2 A, 1.2 V, Slew Rate Controlled Load Switch

DESCRIPTION

The SiP32411 is a slew rate controlled load switch that is designed for 1.1 V to 5.5 V operation.

The device guarantees low switch on-resistance at 1.2 V input. It features a controlled soft-on slew rate of typical 150 μs that limits the inrush current for designs of capacitive load or noise sensitive loads.

The device features a low voltage control logic interface (on/off interface) that can interface with low voltage digital control without extra level shifting circuit. It also integrates an output discharge switch that enables fast shutdown load discharge. When the switch is off, it provides the reverse blocking to prevent high current flowing into the power source.

The SiP32411DN is in TDFN4 package of 1.2 mm by 1.6 mm. It supports over 2 A of continuous current. The SiP32411DR is in SC-70-6 package.

FEATURES

- 1.1 V to 5.5 V operation voltage range
- 62 mΩ typical from 2 V to 5 V for SiP32411DN
- 101 mΩ typical from 2 V to 5 V for SiP32411DR
- Low R_{ON} down to 1.2 V
- Slew rate controlled turn-on: 150 μs at 3.6 V
- Fast shutdown load discharge
- Low quiescent current
  < 1 μA when disabled
  6.7 μA at V_{IN} = 1.2 V
- Switch off reversed blocking
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE Available

APPLICATIONS

- Cellular phones
- Portable media players
- Digital camera
- GPS
- Computers
- Portable instruments and healthcare devices

TYPICAL APPLICATION CIRCUIT

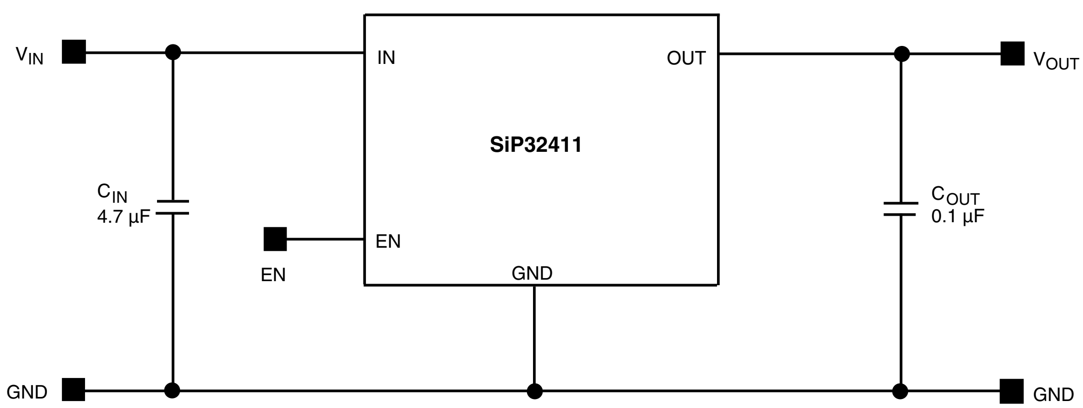

Fig. 1 - SiP32411 Typical Application Circuit

ORDERING INFORMATION			
TEMPERATURE RANGE	**PACKAGE**	**MARKING**	**PART NUMBER**
-40 °C to 85 °C	SC-70-6	MBxx	SiP32411DR-T1-GE3
	TDFN4 1.2 mm x 1.6 mm	Ex	SiP32411DNP-T1-GE4

Notes
- x = lot code
- -GE3 and -GE4 denotes halogen-free and RoHS-compliant

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
Supply input voltage (V_{IN})		-0.3 to 6	V
Enable input voltage (V_{EN})		-0.3 to 6	
Output voltage (V_{OUT})		-0.3 to V_{IN} +0.3	
Maximum continuous switch current ($I_{max.}$)	SC-70-6 package	1.8	A
	TDFN4 1.2 mm x 1.6 mm	2.4	
Maximum pulsed current (I_{DM}) V_{IN} (pulsed at 1 ms, 10 % duty cycle)	SC-70-6 package	2.2	
	TDFN4 1.2 mm x 1.6 mm	3	
ESD rating (HBM)		4000	V
Junction temperature (T_J)		-40 to +125	°C
Thermal tesistance (θ_{JA}) [a]	6 pin SC-70-6 [b]	240	°C/W
	4 pin TDFN4 1.2 mm x 1.6 mm [c]	170	
Power dissipation (P_D) [a]	6 pin SC-70- 6 [b]	230	mW
	4 pin TDFN4 1.2 mm x 1.6 mm [c]	324	

Notes

a. Device mounted with all leads and power pad soldered or welded to PC board, see PCB layout
b. Derate 4.5 mW/°C above T_A = 70 °C, see PCB layout
c. Derate 5.9 mW/°C above T_A = 70 °C, see PCB layout

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE		
PARAMETER	LIMIT	UNIT
Input voltage range (V_{IN})	1.1 to 5.5	V
Operating temperature range	-40 to 85	°C

SPECIFICATIONS							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V_{IN} = 5, T_A = -40 °C to 85 °C (Typical values are at T_A = 25 °C)		LIMITS -40 °C TO 85 °C MIN. [a]	TYP. [b]	MAX. [a]	UNIT
Operating voltage [c]	V_{IN}			1.5	-	5.5	V
Quiescent current	I_Q	V_{IN} = 1.2 V, EN = active		-	6.7	14	µA
		V_{IN} = 1.8 V, EN = active		-	14	24	
		V_{IN} = 2.5 V, EN = active		-	25	40	
		V_{IN} = 3.6 V, EN = active		-	40	60	
		V_{IN} = 4.3 V, EN = active		-	52	75	
		V_{IN} = 5 V, EN = active		-	71	99	
Off supply current	$I_{Q(off)}$	EN = inactive, OUT = open		-	-	1	
Off switch current	$I_{DS(off)}$	EN = inactive, OUT = GND		-	-	1	
Reverse blocking current	I_{RB}	V_{OUT} = 5 V, V_{IN} = 1.2 V, V_{EN} = inactive		-	-	10	
On-resistance	$R_{DS(on)}$	SC-70-6	V_{IN} = 1.2 V, I_L = 100 mA, T_A = 25 °C	-	105	125	mΩ
			V_{IN} = 1.8 V, I_L = 100 mA, T_A = 25 °C	-	101	120	
			V_{IN} = 2.5 V, I_L = 100 mA, T_A = 25 °C	-	101	120	
			V_{IN} = 3.6 V, I_L = 100 mA, T_A = 25 °C	-	101	120	
			V_{IN} = 4.3 V, I_L = 100 mA, T_A = 25 °C	-	101	120	
			V_{IN} = 5 V, I_L = 100 mA, T_A = 25 °C	-	101	120	
		TDFN4 1.2 mm x 1.6 mm	V_{IN} = 1.2 V, I_L = 100 mA, T_A = 25 °C	-	66	76	
			V_{IN} = 1.8 V, I_L = 100 mA, T_A = 25 °C	-	62	72	
			V_{IN} = 2.5 V, I_L = 100 mA, T_A = 25 °C	-	62	72	
			V_{IN} = 3.6 V, I_L = 100 mA, T_A = 25 °C	-	62	72	
			V_{IN} = 4.3 V, I_L = 100 mA, T_A = 25 °C	-	62	72	
			V_{IN} = 5 V, I_L = 100 mA, T_A = 25 °C	-	62	72	
On-resistance temperature coefficient	TC_{RDS}	SC-70-6 package		-	4300	-	ppm/°C
		TDFN4 1.2 mm x 1.6 mm package		-	3400	-	
EN input low voltage [c]	V_{IL}	V_{IN} = 1.2 V		-	-	0.3	V
		V_{IN} = 1.8 V		-	-	0.4 [d]	
		V_{IN} = 2.5 V		-	-	0.5 [d]	
		V_{IN} = 3.6 V		-	-	0.6 [d]	
		V_{IN} = 4.3 V		-	-	0.7 [d]	
		V_{IN} = 5 V		-	-	0.8 [d]	
EN input high voltage [c]	V_{IH}	V_{IN} = 1.2 V		0.9 [d]	-	-	
		V_{IN} = 1.8 V		1.2 [d]	-	-	
		V_{IN} = 2.5 V		1.4 [d]	-	-	
		V_{IN} = 3.6 V		1.6 [d]	-	-	
		V_{IN} = 4.3 V		1.7 [d]	-	-	
		V_{IN} = 5 V		1.8	-	-	
EN Input leakage	I_{SINK}	V_{EN} = 5.5 V		-1	-	1	µA
Output pull-down resistance	R_{PD}	EN = inactive, T_A = 25 °C		-	217	280	Ω
Output turn-on delay time	$t_{d(on)}$	V_{IN} = 3.6 V, R_{load} = 10 Ω, T_A = 25 °C		-	140	210	µs
Output turn-on rise time	$t_{(on)}$			80	150	220	
Output turn-off delay time	$t_{d(off)}$			-	0.27	1	

Notes

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
c. For V_{IN} outside this range consult typical EN threshold curve
d. Not tested, guarantee by design

PIN CONFIGURATION

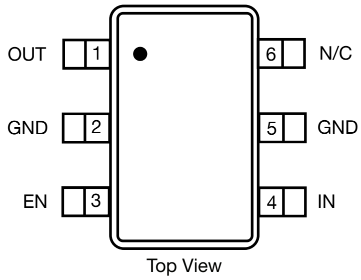

Fig. 2 - SC-70-6 Package

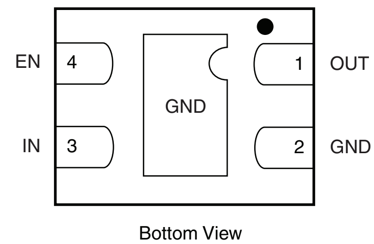

Fig. 3 - TDFN4 1.2 mm x 1.6 mm Package

PIN DESCRIPTION

PIN NUMBER		NAME	FUNCTION
SC-70-6	TDFN4		
4	3	IN	This pin is the n-channel MOSFET drain connection. Bypass to ground through a 2.2 μF capacitor
2, 5	2	GND	Ground connection
3	4	EN	Enable input
1	1	OUT	This pin is the n-channel MOSFET source connection. Bypass to ground through a 0.1 μF capacitor

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

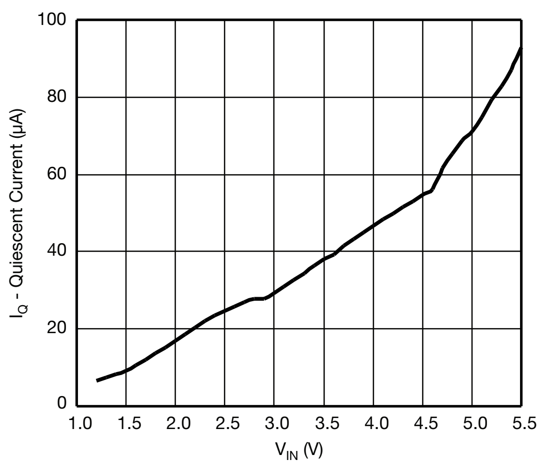

Fig. 4 - Quiescent Current vs. Input Voltage

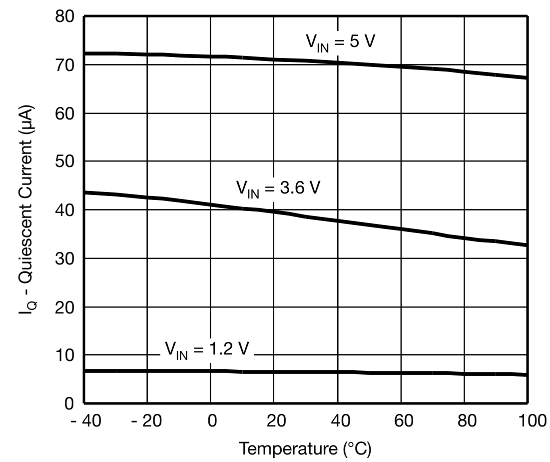

Fig. 6 - Quiescent Current vs. Temperature

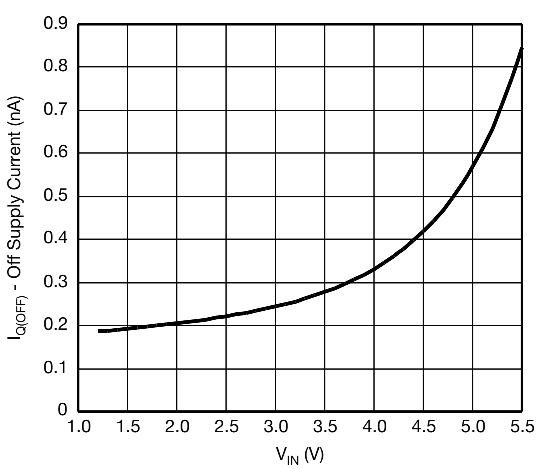

Fig. 5 - Off Supply Current vs. Input Voltage

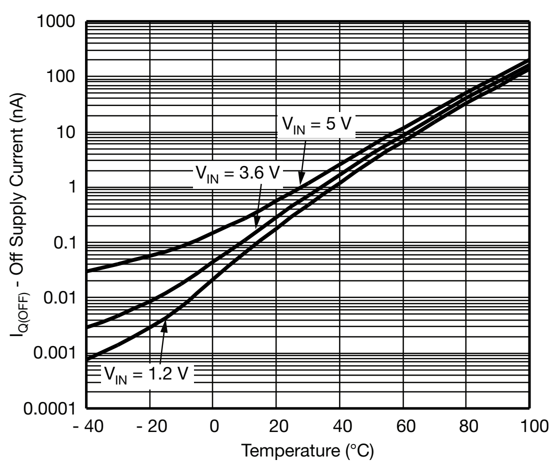

Fig. 7 - Off Supply Current vs. Temperature

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

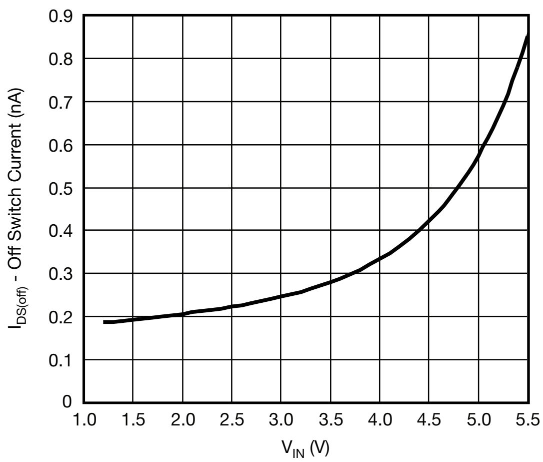

Fig. 8 - Off Switch Current vs. Input Voltage

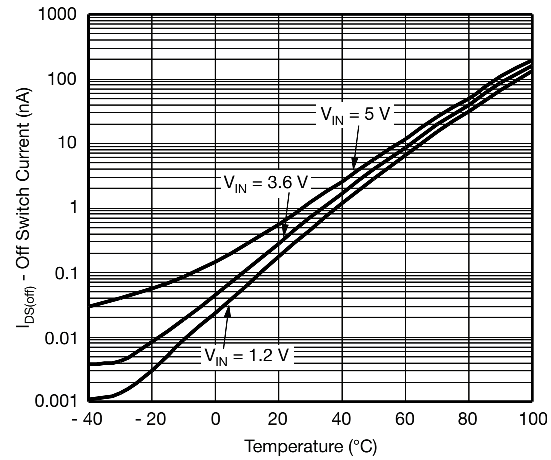

Fig. 11 - Off Switch Current vs. Temperature

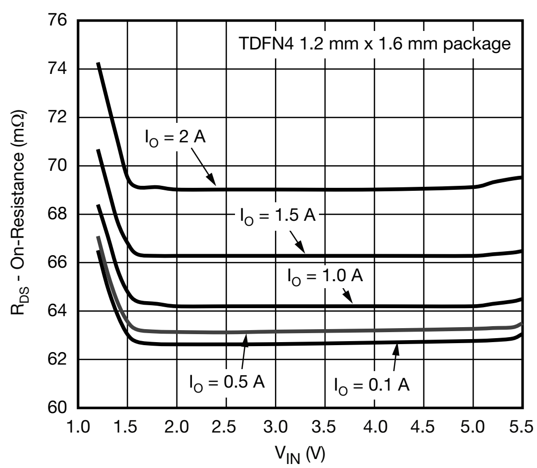

Fig. 9 - $R_{DS(on)}$ vs. V_{IN} for TDFN4 package

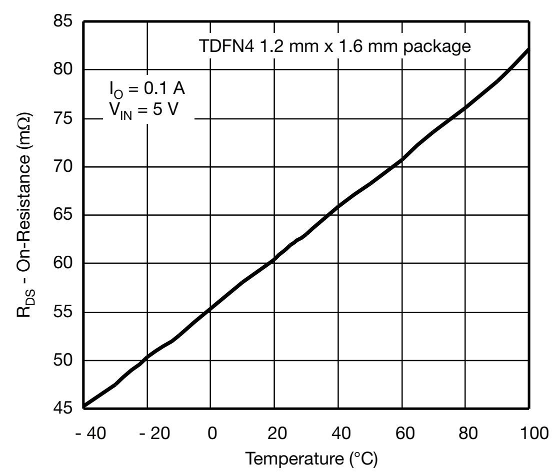

Fig. 12 - $R_{DS(on)}$ vs. Temperature for TDFN4 package

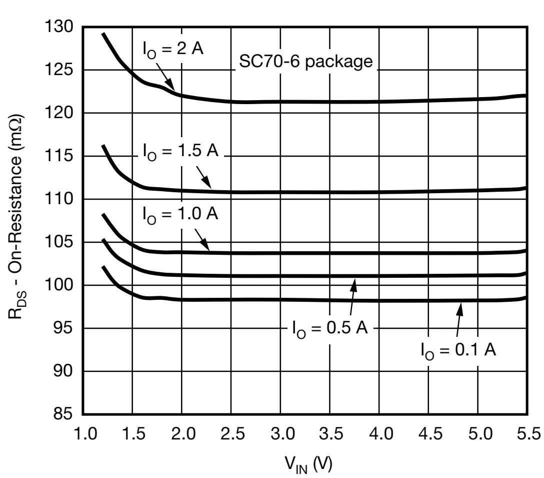

Fig. 10 - $R_{DS(on)}$ vs. V_{IN} for SC-70-6 package

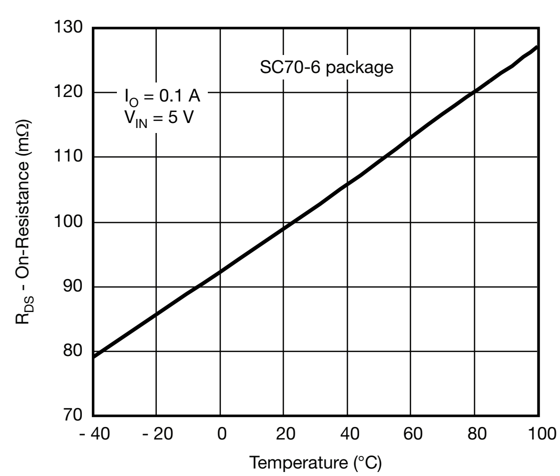

Fig. 13 - $R_{DS(on)}$ vs. Temperature for SC-70-6 package

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

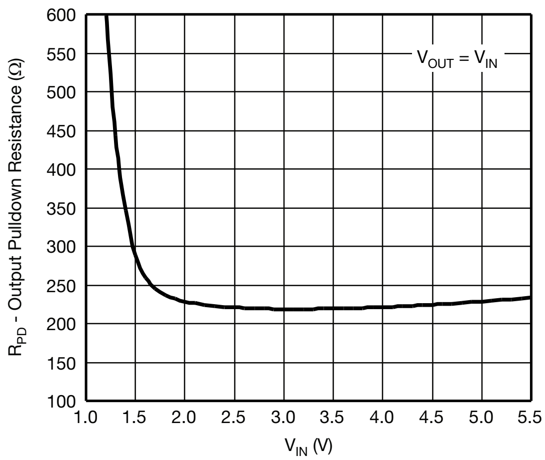

Fig. 14 - Output Pull Down vs. Input Voltage

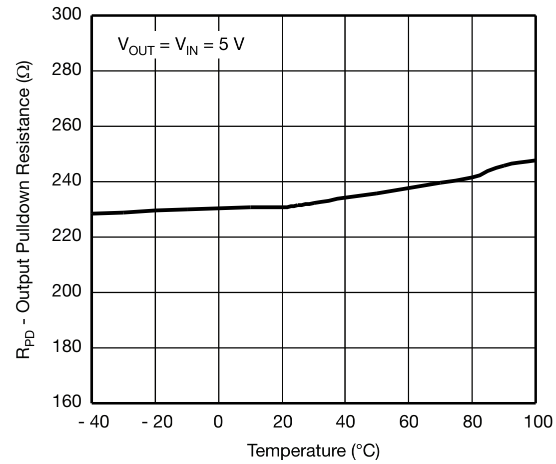

Fig. 17 - Output Pull Down vs. Temperature

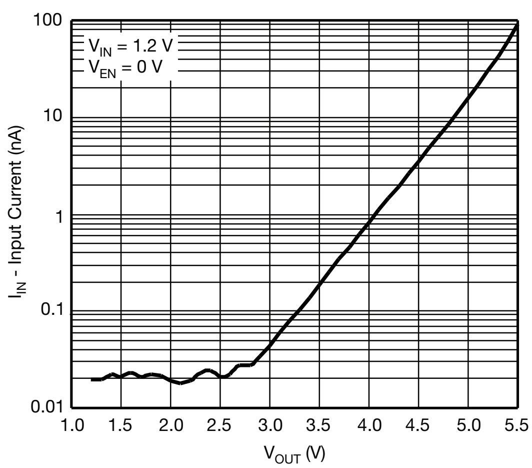

Fig. 15 - Reverse Blocking Current vs. Output Voltage

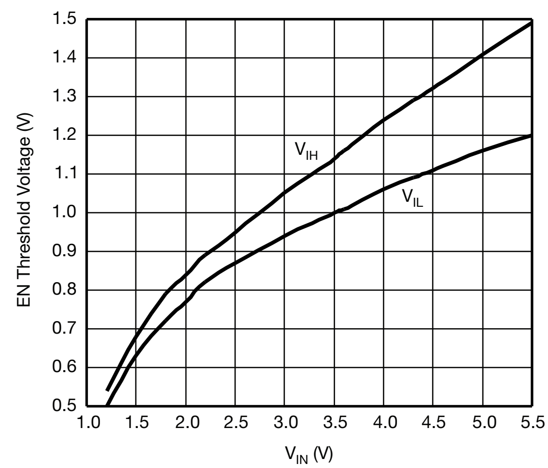

Fig. 18 - EN Threshold Voltage vs. Input Voltage

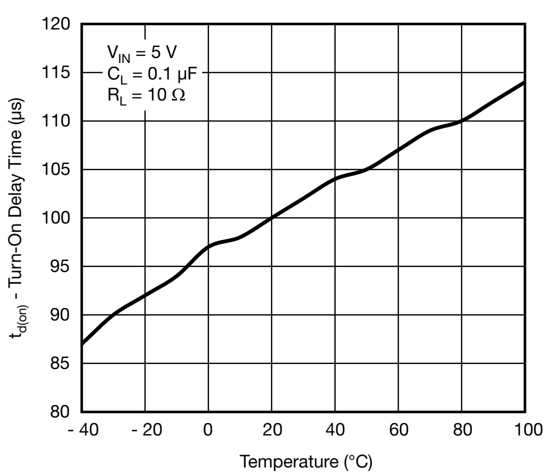

Fig. 16 - Turn-On Delay Time vs. Temperature

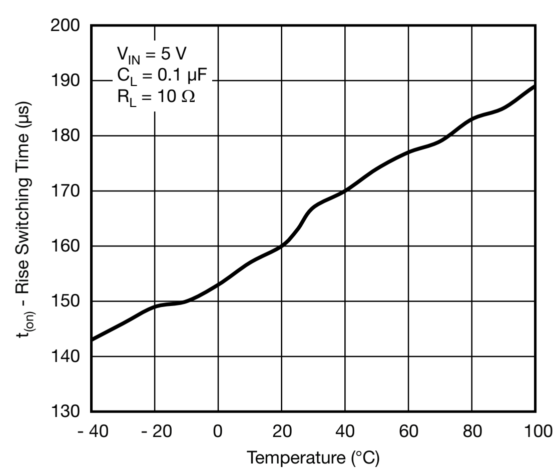

Fig. 19 - Rise Time vs. Temperature

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

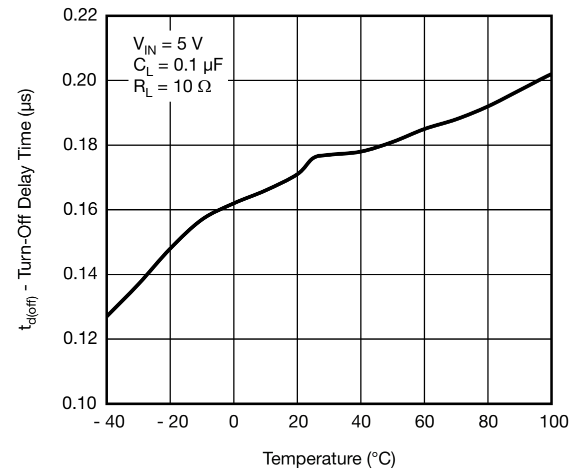

Fig. 20 - Turn-Off Delay Time vs. Temperature

TYPICAL WAVEFORMS

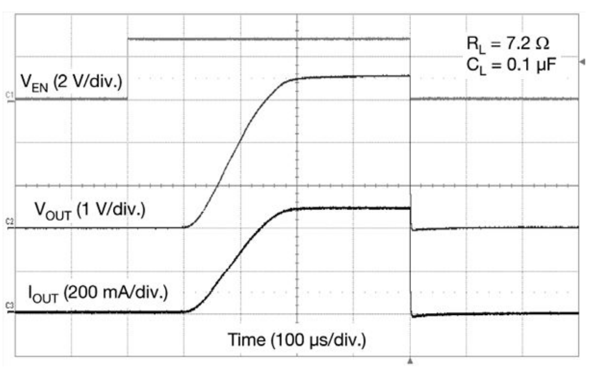

Fig. 21 - Switching (V_{IN} = 3.6 V)

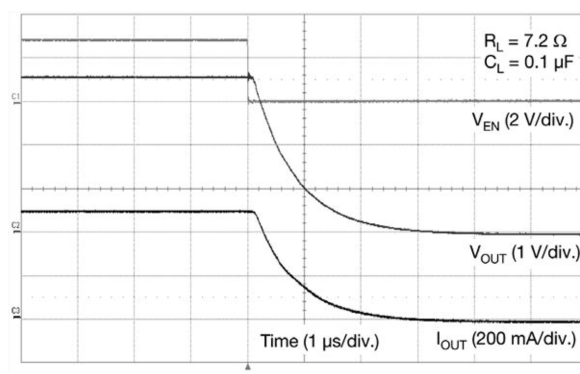

Fig. 23 - Turn-Off (V_{IN} = 3.6 V)

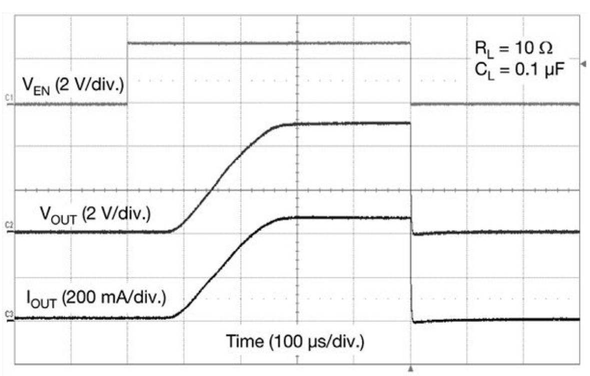

Fig. 22 - Switching (V_{IN} = 5 V)

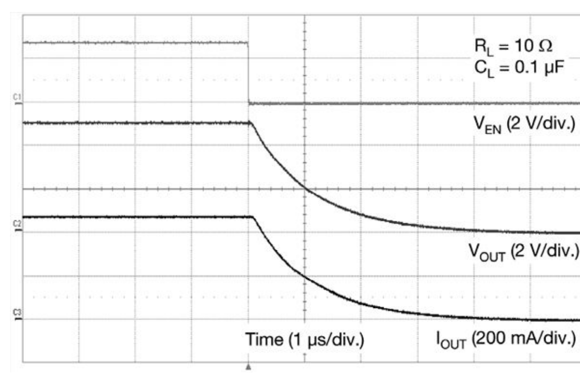

Fig. 24 - Turn-Off (V_{IN} = 5 V)

BLOCK DIAGRAM

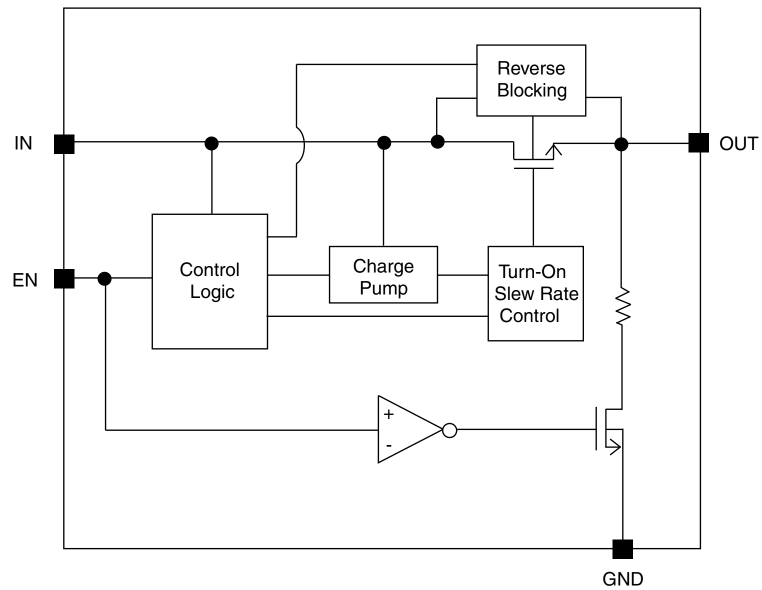

Fig. 25 - Functional Block Diagram

PCB LAYOUT

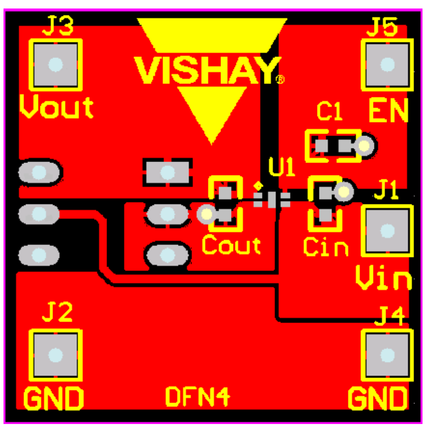

Fig. 26 - Top, PCB Layout for TDFN4 1.2 mm x 1.6 mm (board size: 1" x 1v)

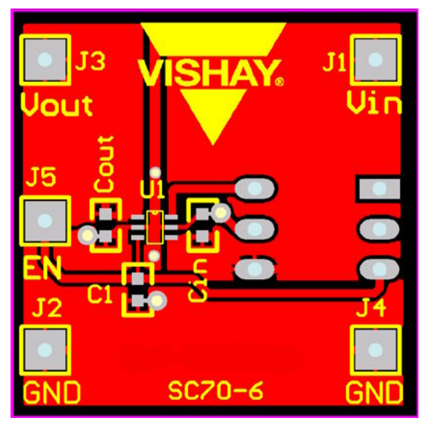

Fig. 28 - Top, PCB Layout for SC-70-6 (board size: 1" x 1")

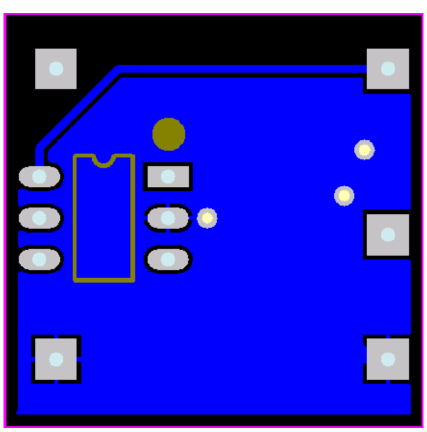

Fig. 27 - Bottom, PCB Layout for TDFN4 1.2 mm x 1.6 mm (board size: 1" x 1")

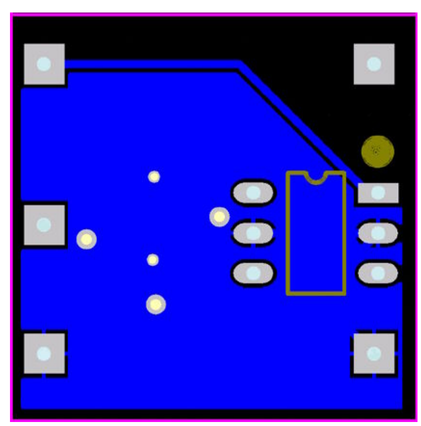

Fig. 29 - Bottom, PCB Layout for SC-70-6 (board size: 1" x 1")

DETAILED DESCRIPTION

SiP32411 is an n-channel power MOSFET designed as high side load switch with slew rate control to prevent in-rush current. Once enable the device charge pumps the gate of the power MOSFET to 5 V gate to source voltage while controlling the slew rate of the turn on time. The mostly constant gate to source voltage keeps the on resistance low through out the input voltage range. When disable, the output discharge circuit turns on to help pull the output voltage to ground more quickly. Also in disable mode, the reverse blocking circuit is activated to prevent current from going back to the input in case the output voltage is higher than the input voltage. Input voltage is needed for the reverse blocking circuit to work properly, it can be as low as $V_{IN(min.)}$.

APPLICATION INFORMATION

Input Capacitor

While a bypass capacitor on the input is not required, a 2.2 µF or larger capacitor for C_{IN} is recommended in almost all applications. The bypass capacitor should be placed as physically close as possible to the SiP32411 to be effective in minimizing transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 0.1 µF capacitor or larger across V_{OUT} and GND is recommended to insure proper slew operation. C_{OUT} may be increased without limit to accommodate any load transient condition with only minimal affect on the SiP32411 turn on slew rate time. There are no ESR or capacitor type requirement.

Enable

The EN pin is compatible with both TTL and CMOS logic voltage levels.

Protection Against Reverse Voltage Condition

The SiP32411 contains a reverse blocking circuitry to protect the current from going to the input from the output in case where the output voltage is higher than the input voltage when the main switch is off. A supply voltage as low as the minimum required input voltage is necessary for this circuitry to work properly.

Thermal Considerations

The SiP32411 is designed to maintain a constant output load current. Due to physical limitations of the layout and assembly of the device the maximum switch current is 1.8 A for SC-70-6 package and 2.4 A for TDFN4 package, as stated in the absolute maximum ratings table. However, another limiting characteristic for the safe operating load current is the thermal power dissipation of the package. To obtain the highest power dissipation (and a thermal resistance of 240 °C/W for SC-70-6 and 170 °C/W for TDFN4) the power pad of the device should be connected to a heat sink on the printed circuit board.

The maximum power dissipation in any application is dependent on the maximum junction temperature, $T_{J(max.)}$ = 125 °C, the junction-to-ambient thermal resistance for the TDFN4 1.2 mm x 1.6 mm package, θ_{J-A} = 170 °C/W, and the ambient temperature, T_A, which may be formulaically expressed as:

$$P\ (\text{max.}) = \frac{T_{J\ (\text{max.})} - T_A}{\theta_{J-A}} = \frac{125 - T_A}{170}$$

It then follows that, assuming an ambient temperature of 70 °C, the maximum power dissipation will be limited to about 324 mW.

So long as the load current is below the 2.4 A limit, the maximum continuous switch current becomes a function two things: the package power dissipation and the $R_{DS(on)}$ at the ambient temperature.

As an example let us calculate the worst case maximum load current at T_A = 70 °C. The worst case $R_{DS(on)}$ at 25 °C occurs at an input voltage of 1.2 V and is equal to 75 mΩ. The $R_{DS(on)}$ at 70 °C can be extrapolated from this data using the following formula

$R_{DS(on)}$ (at 70 °C) = $R_{DS(on)}$ (at 25 °C) x (1 + T_C x ΔT)

Where T_C is 3400 ppm/°C. Continuing with the calculation we have

$R_{DS(on)}$ (at 70 °C) = 75 mΩ x (1 + 0.0034 x (70 °C - 25 °C)) = 86.5 mΩ

The maximum current limit is then determined by

$$I_{LOAD\ (\text{max.})} < \sqrt{\frac{P\ (\text{max.})}{R_{DS(on)}}}$$

which in case is 1.94 A. Under the stated input voltage condition, if the 1.94 A current limit is exceeded the internal die temperature will rise and eventually, possibly damage the device.

PRODUCT SUMMARY		
Part number	SiP32411	SiP32411
Description	1.1 V to 5 V, 62 mΩ, 150 µs rise time, output discharge	1.1 V to 5 V, 101 mΩ, 150 µs rise time, output discharge
Configuration	Single	Single
Slew rate time (µs)	150	150
On delay time (µs)	140	140
Input voltage min. (V)	1.1	1.1
Input voltage max. (V)	5.5	5.5
On-resistance at input voltage min. (mΩ)	66	105
On-resistance at input voltage max. (mΩ)	62	101
Quiescent current at input voltage min. (µA)	6.7	6.7
Quiescent current at input voltage max. (µA)	71	71
Output discharge (yes / no)	Yes	Yes
Reverse blocking (yes / no)	Yes	Yes
Continuous current (A)	2.4	1.8
Package type	TDFN4	SC-70-6
Package size (W, L, H) (mm)	1.2 x 1.6 x 0.5	2.0 x 2.0 x 0.5
Status code	2	2
Product type	Slew rate	Slew rate
Applications	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable

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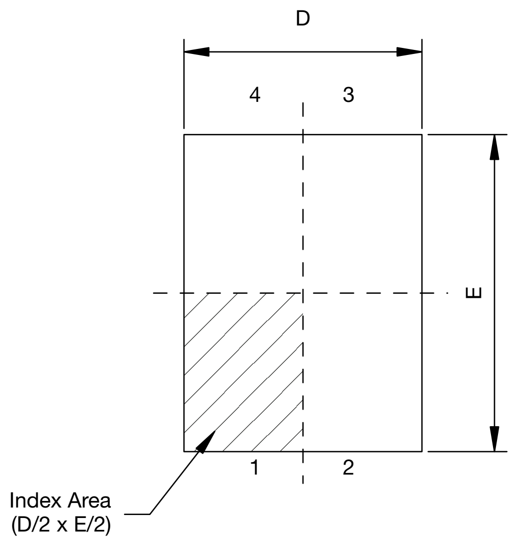
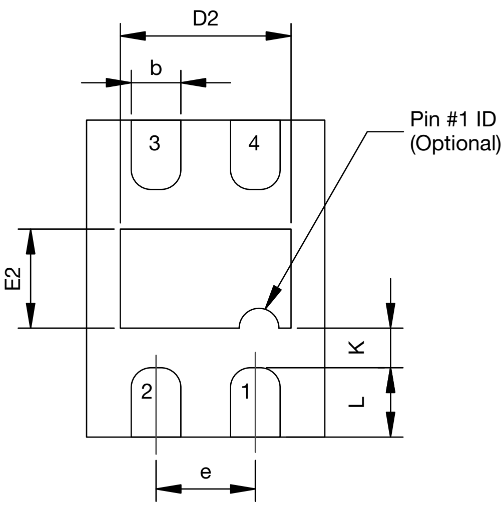
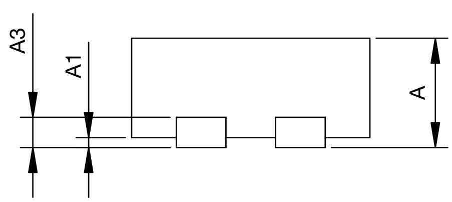
TDFN4 1.2 x 1.6 Case Outline



Top View



Bottom View



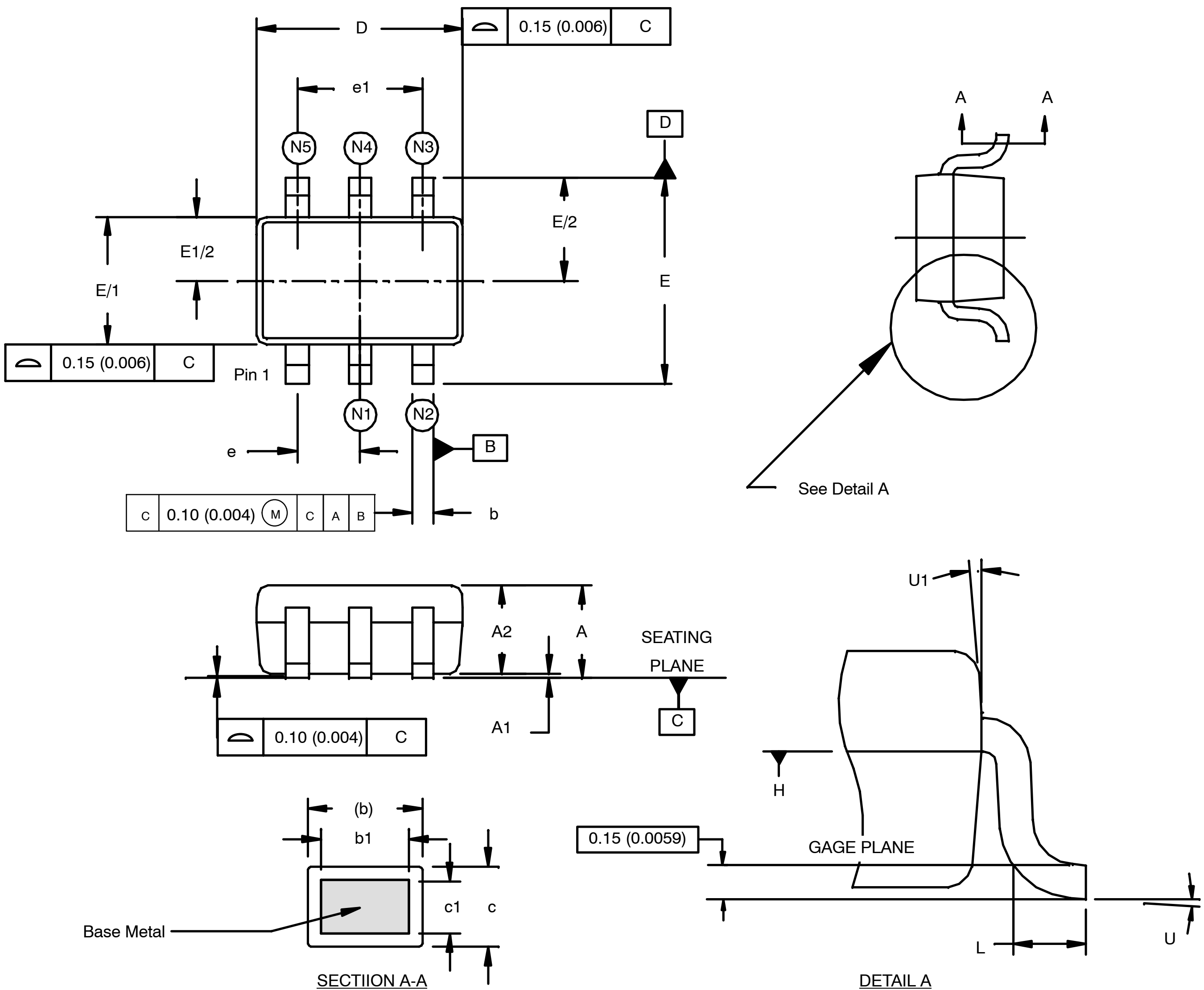
Side View

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.45	0.55	0.60	0.017	0.022	0.024
A1	0.00	-	0.05	0.00	-	0.002
A3	0.15 REF. or 0.127 REF. (1)			0.006 or 0.005 (1)		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.15	1.20	1.25	0.045	0.047	0.049
D2	0.81	0.86	0.91	0.032	0.034	0.036
e	0.50 BSC			0.020		
E	1.55	1.60	1.65	0.061	0.063	0.065
E2	0.45	0.50	0.55	0.018	0.020	0.022
K	0.25 typ.			0.010 typ.		
L	0.25	0.30	0.35	0.010	0.012	0.014
ECN: T16-0143-Rev. C, 18-Apr-16 DWG: 5995						

Note

(1) The dimension depends on the leadframe that assembly house used.

SC-70: 3/4/5/6-LEADS (PIC ONLY)



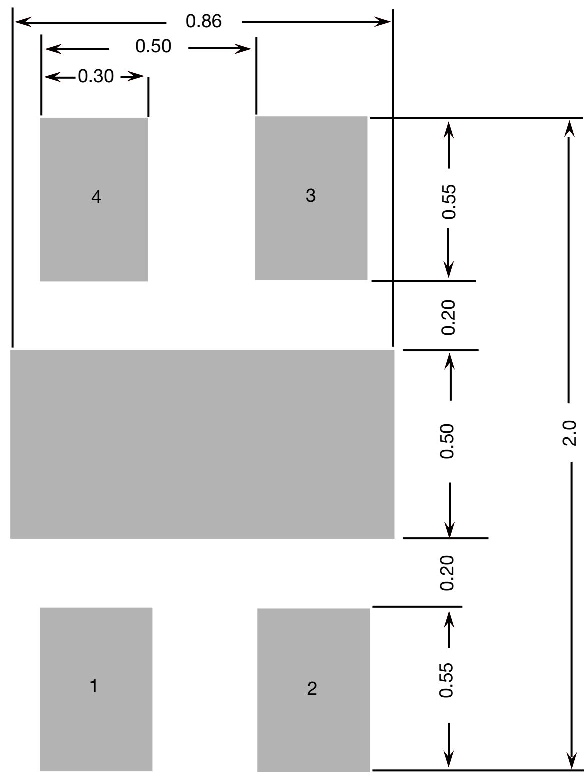
Pin Code	LEAD COUNT			
	3	4	5	6
N1	–	–	2	2
N2	2	2	3	3
N3	–	3	4	4
N4	3	–	–	5
N5	–	4	5	6

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Controlling dimensions: millimeters converted to inch dimensions are not necessarily exact.
3. Dimension “D” does not include mold flash, protrusion or gate burr. Mold flash, protrusion or gate burr shall not exceed 0.15 mm (0.006 inch) per side.
4. The package top shall be smaller than the package bottom. Dimension “D” and “E1” are determined at the outer most extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.80	–	1.10	0.031	–	0.043
A1	0.00	–	0.10	0.000	–	0.004
A2	0.80	0.90	1.00	0.031	0.035	0.040
b	0.15	–	0.30	0.006	–	0.012
b1	0.15	0.20	0.25	0.006	0.008	0.010
c	0.08	–	0.25	0.003	–	0.010
c1	0.08	0.13	0.20	0.003	0.005	0.008
D	1.90	2.10	2.15	0.074	0.082	0.084
E	2.00	2.10	2.20	0.078	0.082	0.086
E_1	1.15	1.25	1.35	0.045	0.050	0.055
e	0.65 BSC			0.0255 BSC		
e_1	1.30 BSC			0.0512 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
U	0°	–	8°	0°	–	8°
U1	4°		10°	4°		10°
ECN: S-42145—Rev. A, 22-Nov-04 DWG: 5941						

RECOMMENDED MINIMUM PADS FOR TDFN4 1.2 x 1.6



Recommended Minimum Pads
Dimensions in mm

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