AN4855
Application note

STEVAL-ISA177V1 5 V/4.25 W non-isolated flyback demo with VIPer01

Introduction

The STEVAL-ISA77V1 is a 5 V/4.25 W power supply set in non-isolated flyback topology using the new and innovative VIPer01 IC for building smart power supplies with green energy management.

The STEVAL-ISA77V1 board features:

- Five-star energy efficiency rating under no load operation ($P_{IN\_no\_load}$ < 10 mW @ 230 V_{AC})
- Compliance with the 10 % load efficiency and 4-point average active-mode efficiency targets prescribed by European CoC ver. 5 Tier 2
- Compliance with IEC55022 Class B conducted EMI, even with reduced EMI filter
- RoHS compliance

The VIPer01 device features:

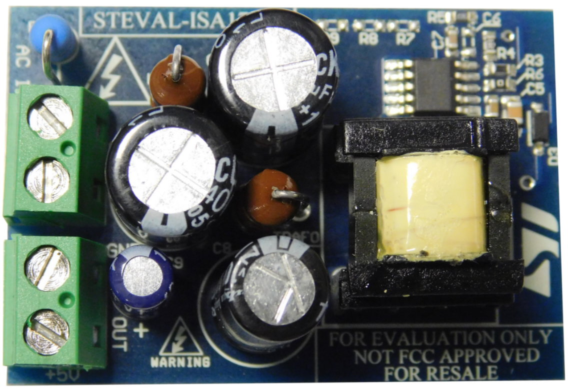
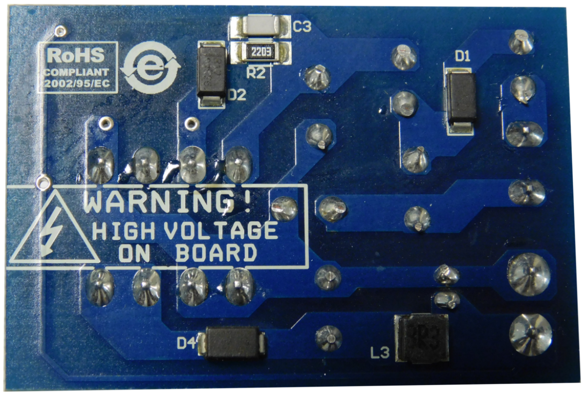
- an 800 V avalanche rugged power MOSFET
- Embedded HV start-up
- Pulse frequency modulation (PFM) and ultra-low stand-by consumption of the internal circuitry under light load condition
- 60 kHz fixed switching frequency with jittering
- On-board transconductance error amplifier internally referenced to 1.2 V ± 2%
- Self-supply option to avoid auxiliary winding and bias components
- Current mode PWM controller with drain current limit protection to facilitate compensation

These features facilitate complete system design with minimum component count.

Enhanced system reliability is ensured by the built-in soft start function and the following protections:

- Pulse skip mode to avoid flux-runaway
- delayed overload protection (OLP)
- max duty cycle counter
- V_{CC} clamp
- Input overvoltage protection
- thermal shutdown

Except for pulse-skip mode, all protections involve auto restart mode.

Figure 1: STEVAL-ISA177V1 top view	Figure 2: STEVAL-ISA177V1 bottom view
	

Contents

List of tables

List of figures

1 Adapter features

Table 1: STEVAL-ISA177V1 electrical specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	85 to 265 V_{AC}
Output voltage	V_{OUT}	5 V
Max output current	I_{OUT}	0.85 A
Output power	P_{OUT}	4.25 W
Precision of output regulation	ΔV_{OUT_LF}	±5 %
High frequency output 1 voltage ripple	ΔV_{OUT_HF}	50 mV
Max ambient operating temperature	T_{AMB}	60 °C
Switching frequency	F_{OSC}	60 kHz

2 Circuit description

The power supply is set in non-isolated flyback topology, as shown in *Figure 5: "Application schematic diagram"*. The input section includes a resistor R1 for inrush current limitation, a diode D1 and a filter (L1, L2, C1, C2) for EMC suppression. The FB pin is the inverting input of an error amplifier and is an accurate 1.2 V voltage reference with respect to GND, which allows the setting and tight regulation of the output voltage through a voltage divider connected directly to the output terminal, according to the following formula:

Equation 1

$$V_{OUT} = 1.2\text{V} \cdot (1 + \frac{R4}{R3})$$

The C-R-C network from COMP (the output of the error amplifier) to GND provides frequency compensation to the feedback loop that regulates the output voltage.

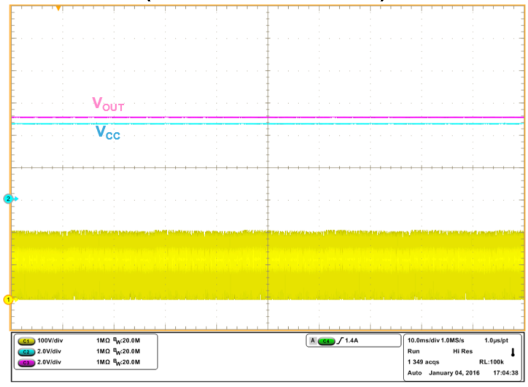
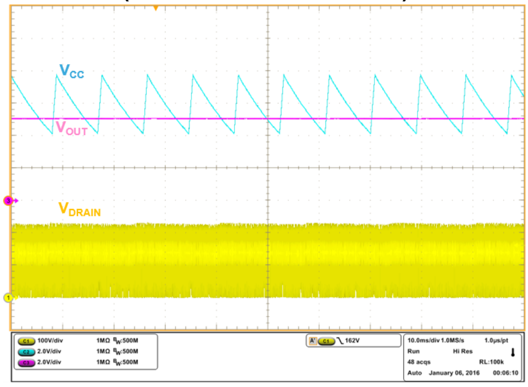
During power-up, as V_{DRAIN} exceeds $V_{HVSTART}$, the internal HV current generator charges the C5 V_{CC} capacitor to V_{CCon}; then the Power MOSFET starts switching, the current generator is turned off and the IC is powered by C5.

Resistors R6, R7, R8 and R9 form a voltage divider from the rectified input mains to DIS voltage, which can be used for input overvoltage protection, as described later. By default, R6 = 0 while R7, R8 and R9 are not mounted in order to minimize input power consumption under no load and light load conditions.

Generally speaking, the VIPer01 can be self-biased or externally biased. The IC is self-biased when V_{CC} can drop to V_{CCson}, which triggers HV source activation until V_{CC} is recharged to V_{CCon}. This results into a sawtooth V_{CC} shape between V_{CCson} and V_{CCon} (see *Figure 4: "V_{CC} waveforms external biasing (diode D3 not connected)"*). Self-supply eliminates the need for a transformer auxiliary winding and auxiliary rectifier (only a capacitor across VCC and GND is needed), at the cost of higher power dissipation and worse stand-by performance.

The IC is externally-biased when V_{CC} does not drop to V_{CCson}. Since the maximum value of V_{CSon} is 4.5V (from the VIPer01 datasheet), this is obtained by simply connecting the small signal diode D3 from the output terminal to VCC. The HV current source is never activated and the V_{CC} shape is constant, just a diode forward drop below V_{OUT} (see *Figure 3: "V_{CC} waveforms external biasing (diode D3 connected)"*). Together with an appropriate design, external biasing allows the achievement of very low input power consumption under no load and light load conditions (less than 10 mW at 230 V_{AC}), thanks to the low consumption of the IC internal blocks.

Only external biasing is considered herein.

Figure 3: V_{CC} waveforms external biasing (diode D3 connected)	Figure 4: V_{CC} waveforms external biasing (diode D3 not connected)
	

3 Schematic diagram and bill of materials

Figure 5: Application schematic diagram

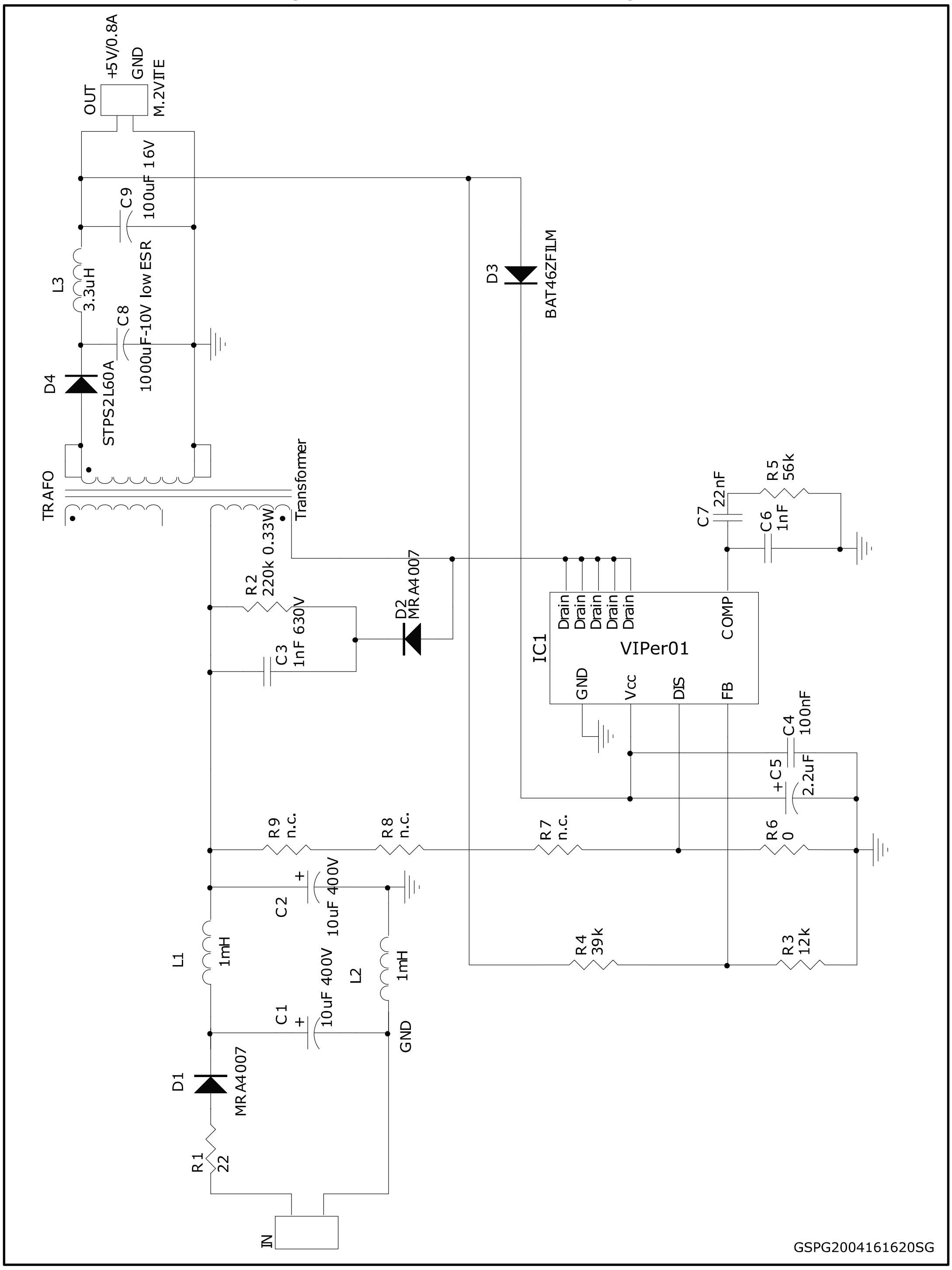


Table 2: Bill of materials

Ref	Part number	Manufacturer	Description	Package
R1	ROX1SJ22R	TE Connectivity	22 Ω 1 W flameproof	Ø3 mm – p 9 mm
R2	ERJ-P08J224V	Panasonic	220 kΩ±5% / 0.66 W / 200 V	1206
R3	ERJP03F2202V	Panasonic	12 kΩ ±1% / 0.2W	0603
R4	ERJP03F3902V	Panasonic	39 kΩ ±1% / 0.2W	0603
R5	ERJP03F5602V	Panasonic	56 kΩ ±1% - 0.2W	0603
R6			0 Ω	0603
R7			not mounted	0603
R8			not mounted	0603
R9			not mounted	0603
C1		RS	Elcap 10 µF-400 V	Ø10 mm – p 5 mm – h 15mm
C2		RS	Elcap 10 µF-400 V	Ø10 mm – p 5 mm – h15 mm
C3	C3216C0G2J102JT	TDK	MLCC capacitor 1 nF-630 V	1206
C4	C1608X7R1H104K080AA	Murata	MLCC capacitor 100 nF - 50 V	0603
C5	GRM21BR61H225KA73L	Murata	MLCC capacitor 2.2µF - 50 V	0805
C6	GCM188R71H102KA37D	Murata	MLCC capacitor 1 nF - 50 V	0603
C7	GRM188R71H223KA01D	Murata	MLCC capacitor 22 nF - 50 V	0603
C8	10ZLH1000MEFC8X16	Rubycon	Elcap 1000 µF-10 V-0.040 Ω - 1330 mA	Ø10 mm – p 5 mm – h12.5 mm
C9	SK016M0100B2F-0511	Yageo	Elcap 100 µF-16 V	Ø 5 mm - P 2 mm – H 11 mm
D1	MRA4007T3G	ON Semiconductor	1 A -1000 V Power rectifier diode	SMA
D2	MRA4007T3G	ON Semiconductor	1 A -1000 V Power rectifier diode	SMA
D3	BAT46ZFILM	STMictroelectronics	Schottky Diode, 0.15 A 100 V	SOD-123
D4	STPS2L60A	STMictroelectronics	2 A - 60 V Power schottky	SMA

Ref	Part number	Manufacturer	Description	Package
L1	B82144A2105J	Epcos	Inductor THT axial LBC 1000 µH 0.2 A	axial
L2	B82144A2105J	Epcos	Inductor THT axial LBC 1000 µH 0.2 A	axial
L3	74404042033	Wurth	Power inducor 3.3 µA	(4x4x1.8) mm
IC1	VIPer01LS	STMicroelectronics	High voltage converter	SSO-10
TF	1921.0054	Magnetica	Flyback transformer	E16

4 Board layout

Figure 6: Board layout (complete)

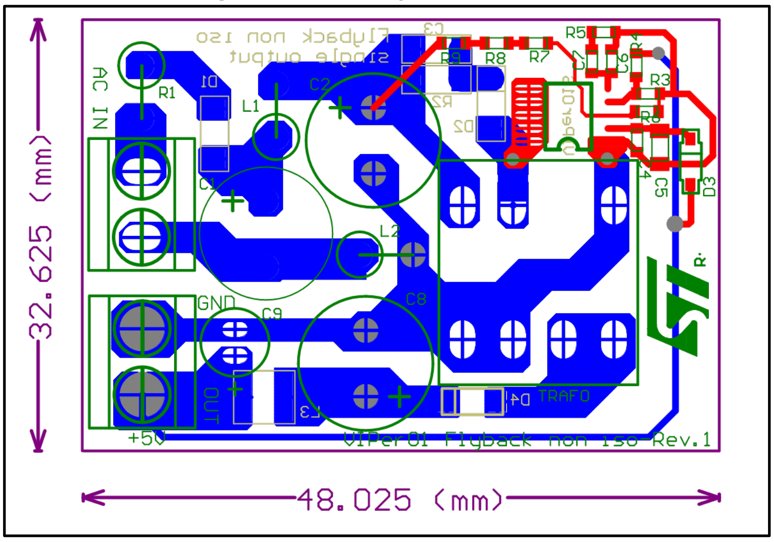


Figure 7: Board layout (top layer)

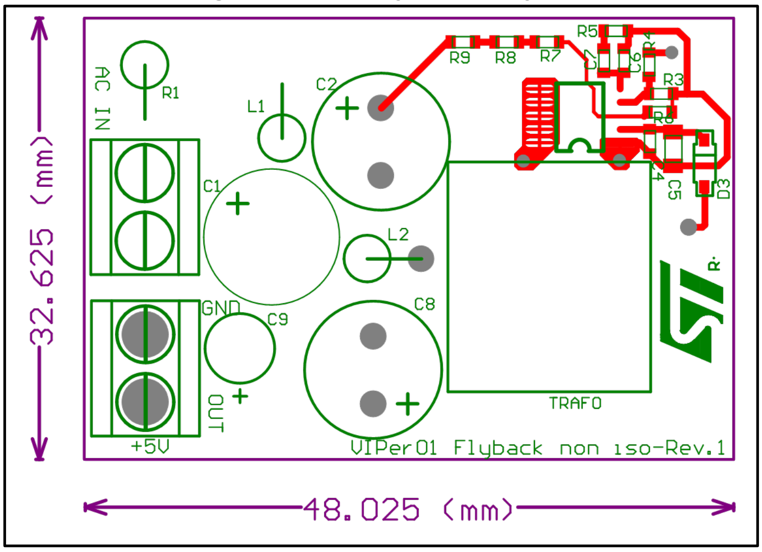
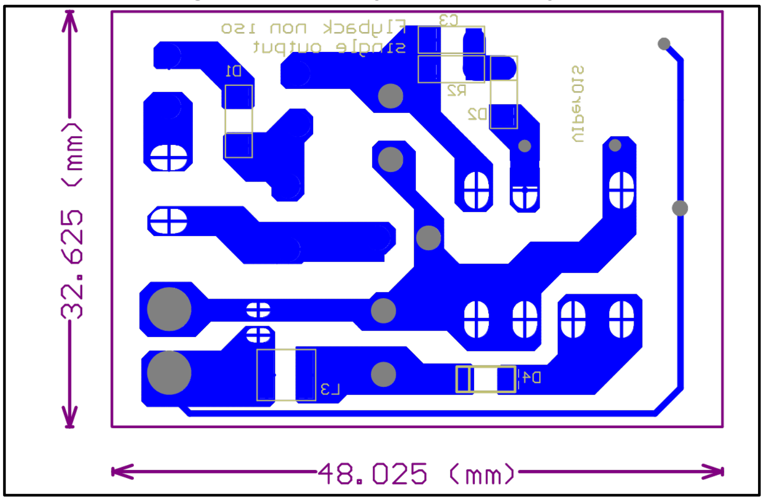


Figure 8: Board layout (bottom layer)



5 Transformer

The electrical and mechanical characteristics of the transformer are shown in the following table and figures.

Table 3: Transformer characteristics

Parameter	Value	Test conditions
Manufacturer	Magnetica	
Part Number	1921.0054	
Primary inductance (pins 3 - 4)	2.0 mH ± 20%	1 kHz, 20 °C
Leakage inductance	90 µH	3-4, 5-6-7-8 s.c. 10 kHz, T_{AMB} 20 °C
Primary to sec. turn ratio (3 - 4)/(7 - 6)	13.93	10 kHz, with tol ±0.5T, T_{AMB} 20 °C
Primary to sec. turn ratio (3 - 4)/(8 - 5)	13.93	10 kHz, with tol ±0.5T, T_{AMB} 20 °C
Saturation current	0.4 A max.	3-4, B_{SAT} 0.32T, T_{AMB} 20 °C
Operating current	0.31 A max.	3-4, P_{MAX} 4 W, 60 kHz, 20 °C
Insulation primary/secondary	500 V	F 50 Hz, time 2”, T_{AMB} 20 °C

Figure 9: Transformer: electrical diagram

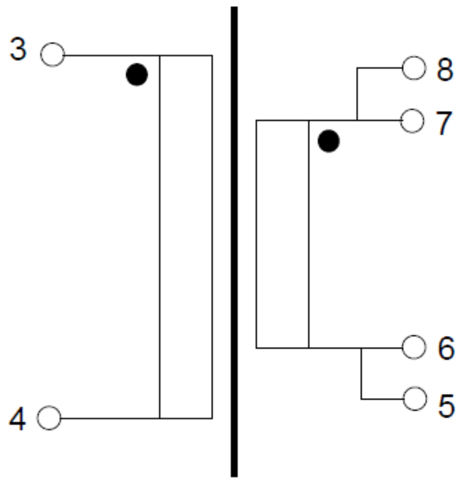


Figure 10: Transformer: pin distances in mm (bottom view)

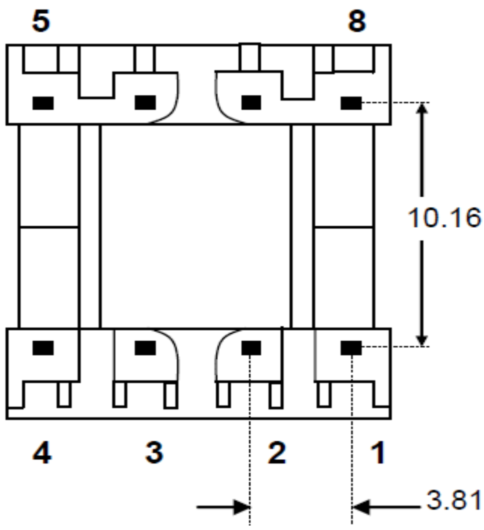


Figure 11: Transformer: front view (mm)

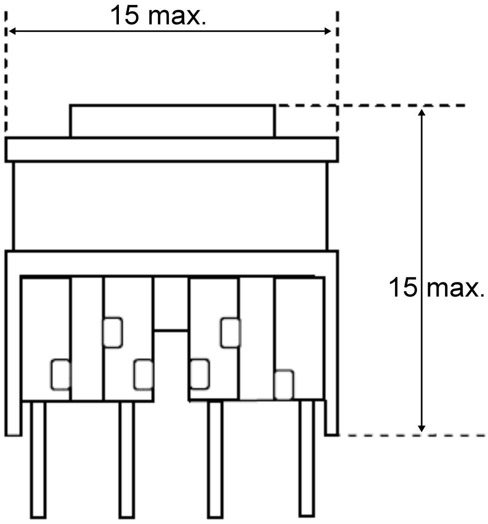
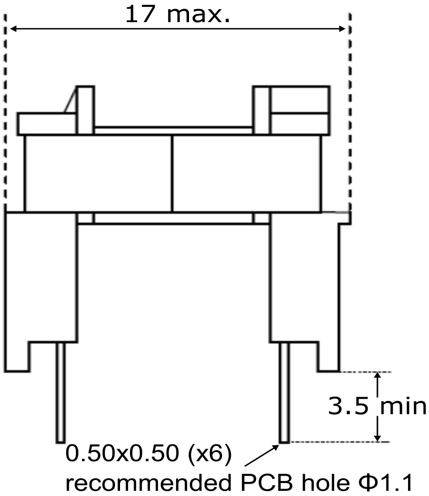


Figure 12: Transformer: side view (mm)



6 Testing the board

6.1 Typical waveforms

Drain voltage and current waveforms under full load condition for the two nominal input voltages are given in *Figure 13: "Drain current/voltage at 115 V_{AC} max. load"* and *Figure 14: "Drain current/voltage at 230 V_{AC} max. load"*, and for minimum and maximum input voltages in *Figure 15: "Drain current/voltage at 90 V_{AC} max. load"* and *Figure 16: "Drain current/voltage at 265 V_{AC} max. load"*, respectively.

Figure 13: Drain current/voltage at 115 V_{AC} max. load

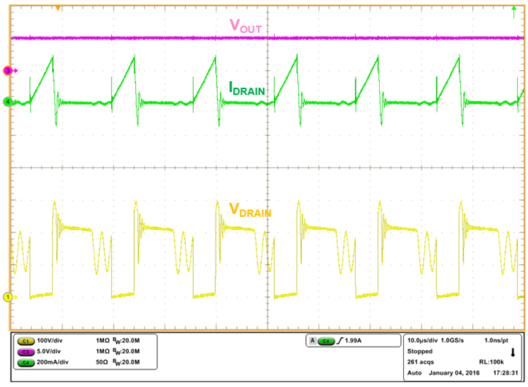


Figure 14: Drain current/voltage at 230 V_{AC} max. load

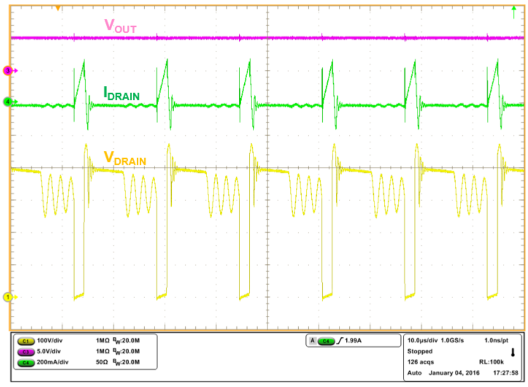


Figure 15: Drain current/voltage at 90 V_{AC} max. load

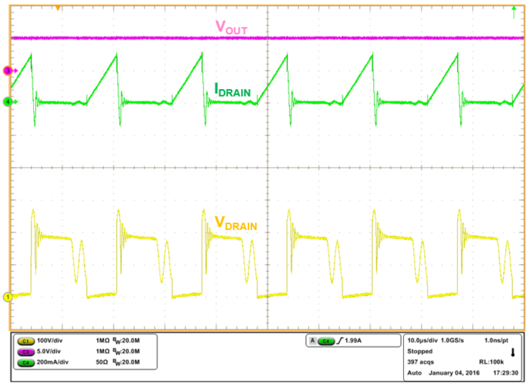


Figure 16: Drain current/voltage at 265 V_{AC} max. load

6.2 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% maximum load at V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC} nominal input voltages.

External power supplies (those housed separately from the end-use devices they are powering) need to comply with the Code of Conduct, version 5 "Active mode efficiency" criterion.

The STEVAL-ISA177V1 is classified under the “Low Voltage external power supply” subclass, for:

- a nameplate output voltage of less than 6 V; and
- a nameplate output current greater than or equal to 550 mA.

For this subclass the Code of Conduct, version 5 states that an SMPS with power throughput of 4.25 W should have an active mode efficiency higher than 72.5% (CoC5 tier2, as of January 2016).

Another applicable standard is the DOE (Department of energy) recommendation of 72.3% active mode efficiency for the same power throughput.

Table 4: "Active mode efficiency" demonstrates the compliance of the STEVAL-ISA177V1 with the above standards.

Table 4: Active mode efficiency

CoC5 req. (P_{OUT} = 4.25 W)		DOE req. (P_{OUT} = 4.25 W)	STEVAL-ISA177V1 performance
Tier 1	Tier2		
69.5%	72.5%	72.3%	74.60% (at V_{IN} =115 V_{AC})
			75.09% (at V_{IN} = 230 V_{AC})

6.3 Light load performance

In version 5 of the Code of Conduct, there are also efficiency requirements when the output load is 10% of the nominal output power. The following table evidences the compliance of the STEVAL-ISA177V1 device with this requirement.

Table 5: CoC5 requirement and STEVAL-ISA177V1 performance at 10% output load

CoC5 efficiency requirements at P_{OUTnom}/10 (P_{OUTnom} = 4.25 W)		STEVAL-ISA177V1 performance
Tier 1	Tier 2	
60.8%	63.7%	72.20% (at V_{IN} = 115 V_{AC})
		65.12% (at V_{IN} = 230 V_{AC})

Power consumption when the power supply is not loaded is also considered in CoC5. The table below evidences the conformance of the STEVAL-ISA177V1 with the criteria for EPS converters with nominal output power below 49 W at nominal input voltages.

Table 6: CoC5 power consumption criteria for no load and STEVAL-ISA177V1 performance

Max no load consumption (49 W > Pno > 0.3 W)		STEVAL-ISA177V1 no load consumption
Tier 1	Tier 2	
150 mW	75 mW	4.4 mW (at V_{IN} = 115 V_{AC})
		8.6 mW (at V_{IN} = 230 V_{AC})

Depending on the equipment supplied, there are several criteria to measure the performance of a converter. In particular, one requirement for light load performance (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW.

The following table shows how the STEVAL-ISA177V1 board satisfies this requirement, along with efficiency figures for P_{OUT} = 25 mW and P_{OUT} = 50 mW light load conditions.

Table 7: Light load performance

V_{IN} [V_{AC}]	efficiency [%]		
	P_{OUT} = 25 mW	P_{OUT} = 50 mW	P_{OUT} = 250 mW
115	51.46	56.15	69.21
230	43.55	49.95	62.73

Another criterion is output power (or efficiency) when the input power is equal to one Watt.

Table 8: Efficiency at P_{IN} = 1 W

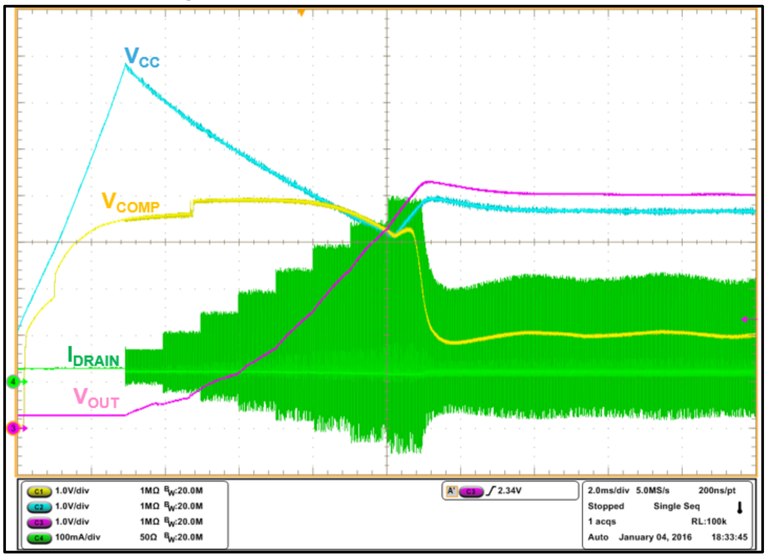
V_{IN} [V_{AC}]	efficiency at P_{IN} = 1 W [%]
115	70.7
230	63.5

7 IC features

7.1 Soft start

The device features an internal soft-start function, which progressively increases the cycle-by-cycle current limitation set point from zero up to I_{DLIM} in eight 50 mA steps. This limits the drain current during the output voltage increase and therefore reduces the stress on the secondary diode. The soft-start time t_{SS} (the time needed for the current limitation set-point to reach its final value) is internally fixed at 8 ms. This function is activated on converter start-up and on restart after a fault event..

Figure 17: STEVAL-ISA177V1 soft start



7.2 Overload protection (OLP)

During an overload or short circuit, the drain current reaches I_{DLIM}. For every cycle that this condition is met, an internal OCP counter is incremented and the protection is tripped if the fault is maintained for time t_{OVL} (50 ms typ., internally fixed), see *Figure 18: "OLP: fault applied during steady state operation; t_{OVL}"*. On protection tripping, the power section is turned off and the converter is disabled for $t_{RESTART}$ (1 s typ.), after which the IC resumes switching and, if the fault persists, continues triggering the protection in the same way (see *Figure 19: "OLP: fault applied during steady state operation; $t_{RESTART}$"*). This lowers the restart attempt rate to ensure safe operation with extremely low power throughput and avoids IC overheating.

Furthermore, every time the protection is tripped, the internal soft-start function is invoked (see *Figure 20: "OLP: fault maintained; t_{SS} and t_{OVL}"*) at restart to reduce the stress on the secondary diode.

Following fault removal, the IC resumes working normally. If the fault is removed during t_{SS} or t_{OVL}, i.e., before protection tripping, the counter counts down each cycle to zero and the protection is not tripped. If the short circuit is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period to elapse before resuming switching (*Figure 21: "OLP: fault removed and autorestart"*).

Figure 18: OLP: fault applied during steady state operation; t_{OVL}

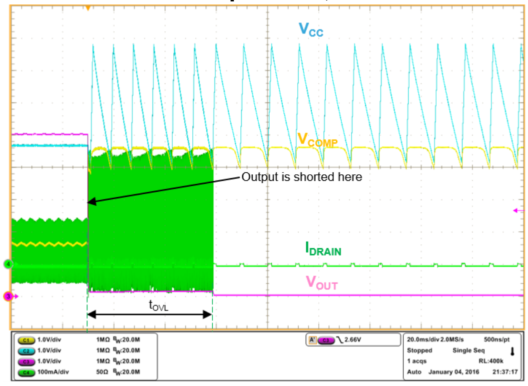


Figure 19: OLP: fault applied during steady state operation; $t_{RESTART}$

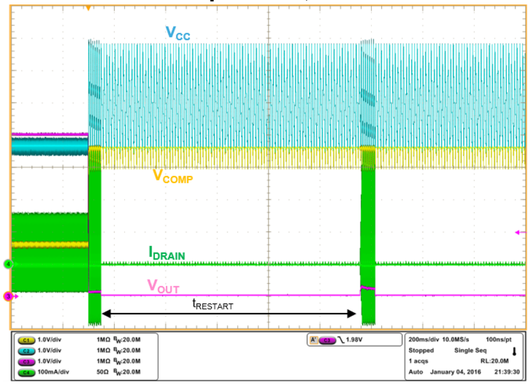


Figure 20: OLP: fault maintained; t_{SS} and t_{OVL}

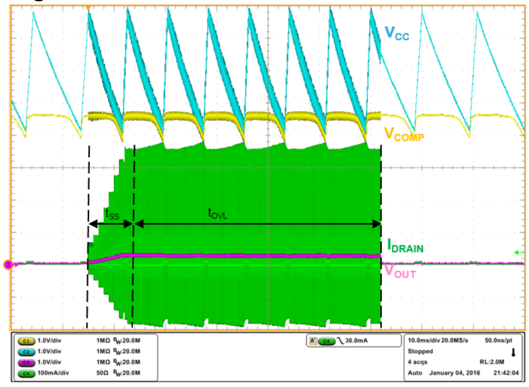
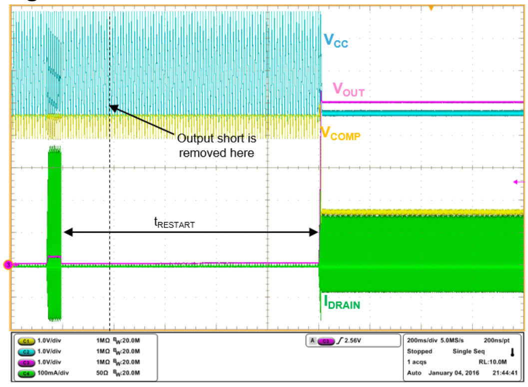


Figure 21: OLP: fault removed and autorestart



7.3 Pulse skip mode

Any time the I_{DRAIN} drain peak current exceeds I_{DLIM} within t_{ON_MIN} minimum on-time, one switching cycle is skipped. The check is performed on a cycle-by-cycle basis, and the cycles can be skipped until the minimum switching frequency F_{OSC_MIN} (15 kHz, typ.) is reached.

If the above condition persists, when the internal OCP counter reaches its end-of-count, the IC is stopped for $t_{RESTART}$ (1s, typ.) and subsequently reactivated via the soft-start phase. Whenever I_{DRAIN} does not exceed I_{DLIM} within t_{ON_MIN}, one switching cycle is restored. The check is made on a cycle-by-cycle basis, and the cycles can be restored until the nominal switching frequency F_{OSC} is reached.

Providing, when needed, an inductor discharge time longer than what would be allowed at nominal switching frequency, the protection helps limit the "flux runaway" effect, often present at converter startup when the primary MOSFET, charged during the minimum on-time through the input voltage, cannot discharge the same amount during off-time because the output voltage is very low. The result is a net increase in average inductor current, which can reach dangerously high values while the output capacitor is not yet sufficiently charged to ensure the inductor discharge rate needed for the volt-second balance.

To check the protection, the secondary diode D4 is shorted while the converter is operating at 265 V_{AC}. In the following two figures, the first part of the protection sequence is captured. From *Figure 23: "V_{IN} = 230 V_{AC}, D4 shorted, steady-state - image 2"*:

1. I_{DLIM} is exceeded at the first cycle, so the next cycle is skipped, resulting in a 30 kHz switching frequency;
2. I_{DLIM} is exceeded again, so the switching frequency is further halved to 15 kHz;
3. I_{DLIM} is exceeded again and the switching frequency is kept at 15 kHz indefinitely.

Figure 22: V_{IN} = 230 V_{AC}, D4 shorted, steady-state - image 1

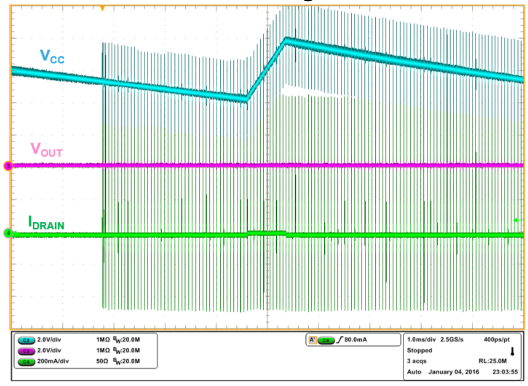
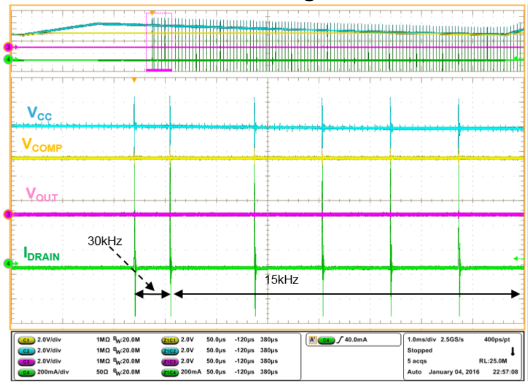


Figure 23: V_{IN} = 230 V_{AC}, D4 shorted, steady-state - image 2



Magnification of one of the switching cycles in *Figure 23: "V_{IN} = 230 V_{AC}, D4 shorted, steady-state - image 2"* shows the DRAIN current rising so quickly that it exceeds I_{DLIM} within t_{ON_MIN} (*Figure 24: "V_{IN} = 230 V_{AC}, D4 shorted, zoom"*). The converter is operated indefinitely at 15 kHz and the OCP internal counter is incremented at every switching cycle. Since it is designed so to reach its end of count (defining t_{OVL}) after 50 ms at 60 kHz operation, the overload time is incremented to 200 ms, as shown in *Figure 25: "V_{IN} = 230 V_{AC}, D4 shorted, steady-state - image 3"*.

Figure 24: V_{IN} = 230 V_{AC}, D4 shorted, zoom

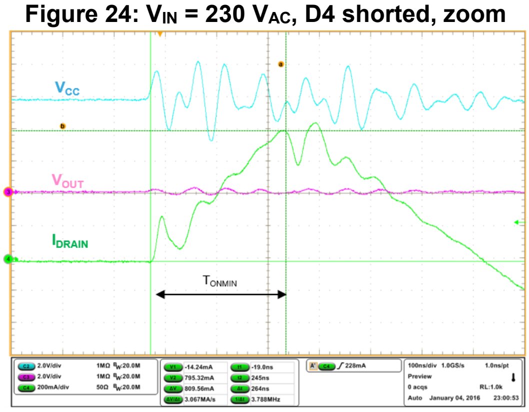
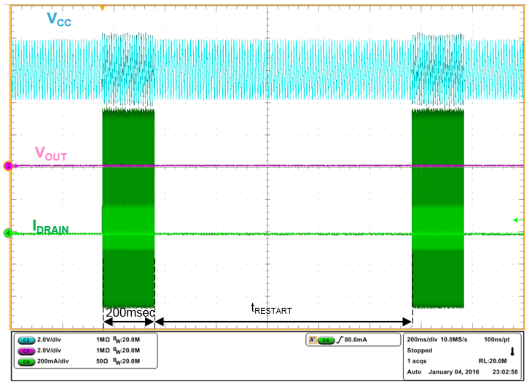


Figure 25: V_{IN} = 230 V_{AC}, D4 shorted, steady-state - image 3



7.4 Maximum duty cycle counter protection

The IC embeds a max. duty-cycle counter which disables the PWM if the MOSFET is turned off by max. duty cycle (70% min., 80% max.) for ten consecutive switching cycles. After protection tripping, the PWM is disabled for $t_{RESTART}$ and subsequently reactivated via the soft-start phase until the fault condition is removed.

In some cases (i.e., breaking of the loop at low input voltage) even if V_{COMP} is saturated high, the OLP cannot be triggered because the PWM is turned off at every switching cycle by maximum duty cycle before the DRAIN peak current can reach I_{DLIM}. This can cause the output voltage V_{OUT} to rise uncontrollably and be maintained well above nominal values indefinitely, placing the output capacitor, the output diode and the IC itself at risk due to the potential breach of the 800 V breakdown threshold. The max duty cycle counter protection prevents this kind of failure.

To test this protection, heavy load and low input voltage are selected.

The IC is protected in autorestart mode for $t_{RESTART}$ (1 s typ.), then continues attempting soft-starts until the fault condition is removed (*Figure 26: "Shut down due to max. duty cycle counter (initial tripping and restart)"* and *Figure 27: "Shut down due to max. duty cycle counter (steady state)"*).

Figure 26: Shut down due to max. duty cycle counter (initial tripping and restart)

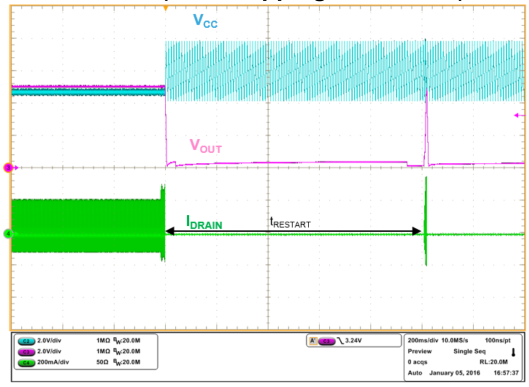


Figure 27: Shut down due to max. duty cycle counter (steady state)

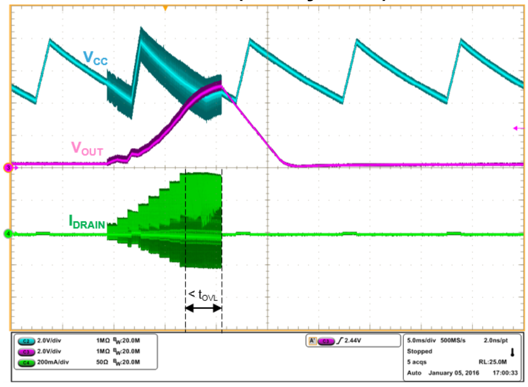


Figure 28: "Shut down due to max. duty cycle counter (steady state) - zoom" shows the ten cycles causing the protection intervention. *Figure 29: "First of ten consecutive switching cycles at max. duty cycle"* magnifies the first cycle and shows the duty cycle measurement: 12/(12 + 4) = 75%.

Figure 28: Shut down due to max. duty cycle counter (steady state) - zoom

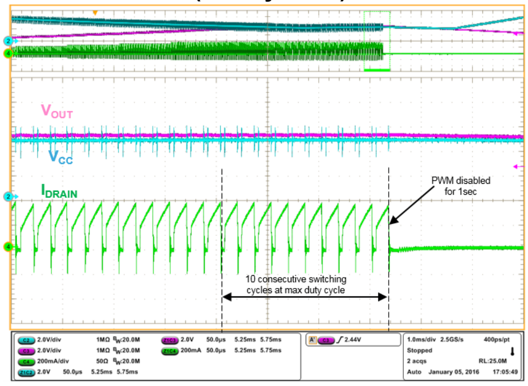
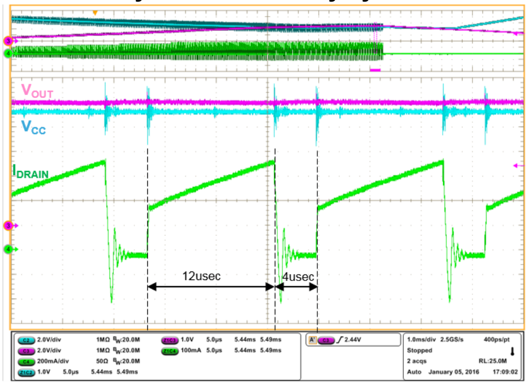


Figure 29: First of ten consecutive switching cycles at max. duty cycle



7.5 Overtemperature protection

If the VIPer01 junction temperature rises higher than the internal threshold T_{SD} (160 °C, typ.), the PWM is disabled for $t_{RESTART}$. A single switching cycle is then performed, in which the temperature sensor embedded in the Power MOSFET section is checked. If a junction temperature above T_{SD} persists, the PWM is maintained disabled for time $t_{RESTART}$ (*Figure 30: "OTP tripping and steady-state"* and *Figure 31: "Turn on for thermal check during OTP"*).

The STEVAL-ISA177V1 is subjected to overheating by air flow from a thermal gun and the IC shuts down when the case temperature measures approximately 152 °C (with a thermal camera). The load is then decreased and the converter resumes with a soft start phase when the case temperature drops to about 120 °C.

Figure 30: OTP tripping and steady-state

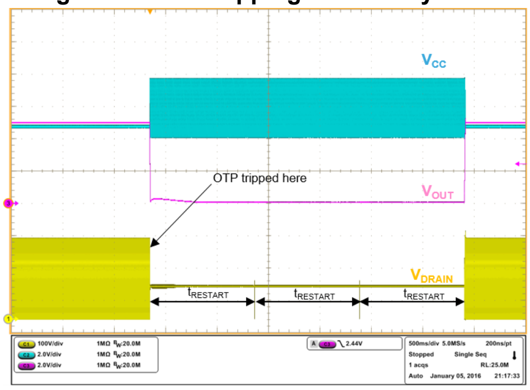
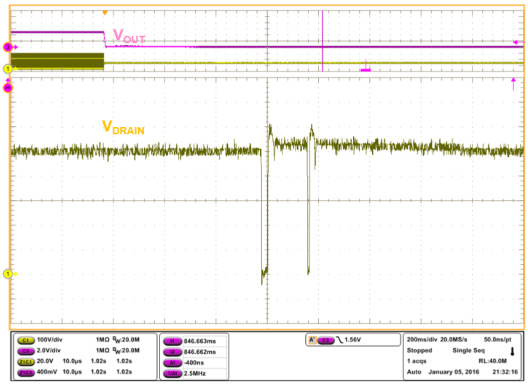


Figure 31: Turn on for thermal check during OTP



7.6 Input overvoltage protection

When the voltage across the DIS pin is externally pulled above the internal threshold V_{DIS_th} (1.2 V typ.) for more than t_{DEB} (for instance by means of a voltage divider connected to some higher voltage), the PWM is disabled in autorestart mode for $t_{DIS\_RESTART}$ (500 ms, typ.). This simplifies the implementation of input overvoltage protection, by simply connecting a voltage divider from the rectified input mains to the DIS pin. Resistors R6, R7, R8 and R9 in *Figure 5: "Application schematic diagram"* can be used for this purpose, with values selected according to the following formula:

Equation 2

$$R7 + R8 + R9 = (\frac{V_{IN\_OVP}}{V_{DIS_{th}}} - 1) \cdot R6$$

where V_{IN_OVP} is the desired input overvoltage threshold.

The additional steady-state power consumption of this network is:

Equation 3

$$P_{DIS}(V_{INdc}) = \frac{(V_{INdc} - V_{DIS})^2}{R7 + R8 + R9} + \frac{{V_{DIS}}^2}{R6}$$

As an example, if R6 = 12 kΩ, R7 = 2 MΩ, R8 = R9 = 1 MΩ, the protection is triggered at V_{IN} = 400 V_{DC}, with an additional steady-state power consumption at 265 V_{AC} of about 35 mW.

As STEVAL-ISA177V1 is in non-isolated topology, an output overvoltage protection can be obtained by connecting the voltage divider to the output terminal, with the additional network power consumption being:

Equation 4

$$P_{DIS}(V_{OUT}) = \frac{(V_{OUT} - V_{DIS})^2}{R7 + R8 + R9} + \frac{{V_{DIS}}^2}{R6}$$

If the disable function is not required, the DIS pin must be soldered to GND (as in the STEVAL-ISA177V1 default setting) to exclude the function.

The following figures show some relevant waveforms for input overvoltage protection implemented through the DIS pin.

Figure 32: Input OVP triggering

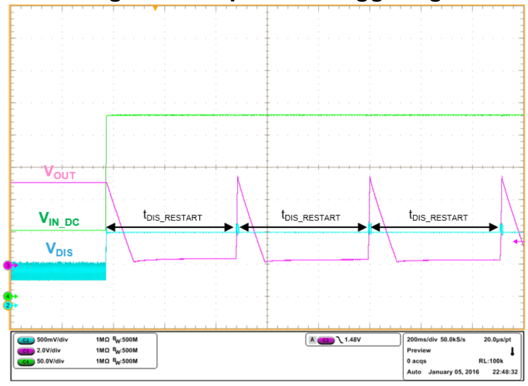


Figure 33: Input OVP triggering (steady state)

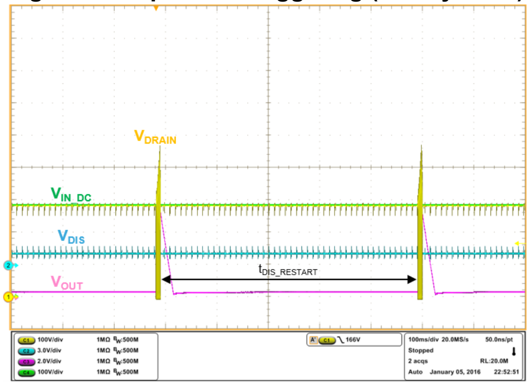


Figure 34: Input OVP triggering (steady state, zoom)

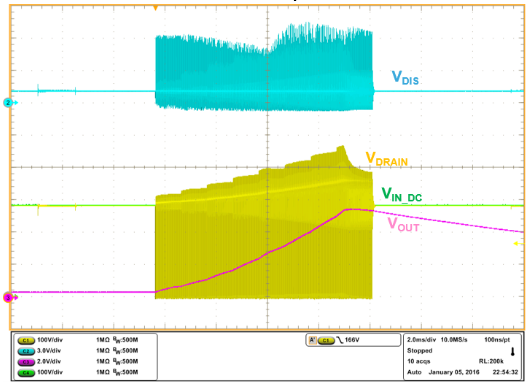
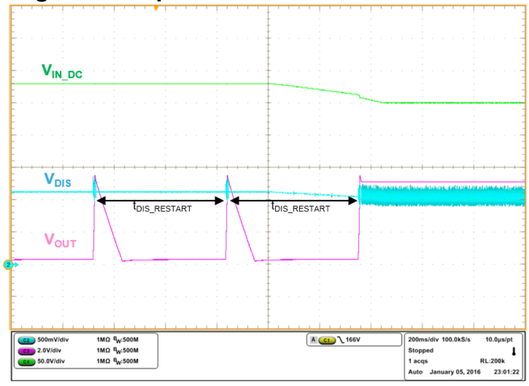


Figure 35: Input OVP removed and IC restart

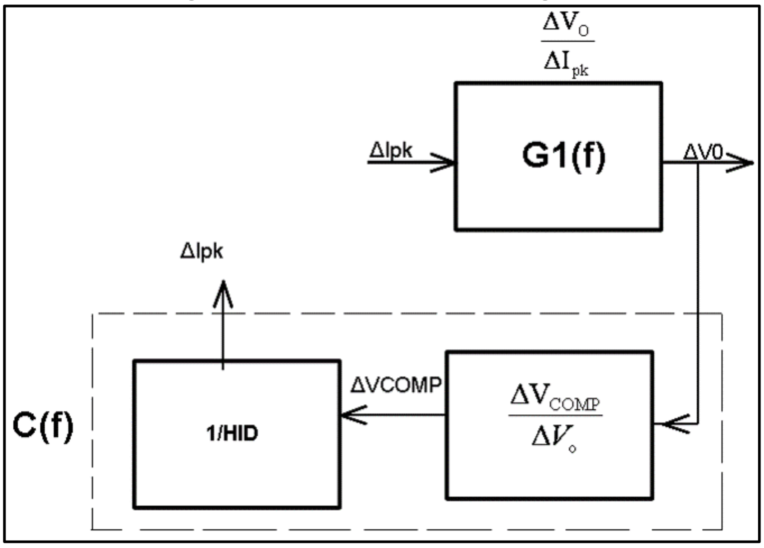


8 Feedback loop calculation guidelines

8.1 Transfer function

In the following figure, G1(f) represents the set PWM modulator plus power stage, while C(f) is the "controller" network which ensures system stability.

Figure 36: Control loop block diagram



The mathematical expression for the power plant G1(f) is:

Equation 5

$$G1(f) = \frac{\Delta V_O}{\Delta I_{pk}} = \frac{V_{OUT} \cdot \left(1 + \frac{j \cdot 2 \cdot \pi \cdot f}{z}\right)}{Ipkp(fsw, Vdc) \cdot \left(1 + \frac{j \cdot 2 \cdot \pi \cdot f}{p}\right)} = \frac{V_{OUT} \cdot \left(1 + \frac{j \cdot f}{fz}\right)}{Ipkp(fsw, Vdc) \cdot \left(1 + \frac{j \cdot f}{fp}\right)}$$

fp is the pole due to the output load and fz is the zero due to the ESR of the output capacitor:

Equation 6

$$fp = \frac{1}{\pi \cdot Cout \cdot (Rout + 2 \cdot ESR)}$$

Equation 7

$$fz = \frac{1}{2 \cdot \pi \cdot Cout \cdot ESR}$$

The mathematical expression of the compensator C(f) is:

Equation 8

$$C(f) = \frac{\Delta I_{pk}}{\Delta V_O} = \frac{C_0}{H_{COMP}} \cdot \frac{1 + \frac{f \cdot j}{fZc}}{2 \cdot \pi \cdot f \cdot j \cdot \left(1 + \frac{f \cdot j}{fPc}\right)}$$

where:

Equation 9

$$C_0 = -\frac{G_M}{C6 + C7} \cdot \frac{R3}{R3 + R4}$$

Equation 10

$$fZc = \frac{1}{2 \cdot \pi \cdot R5 \cdot C7}$$

Equation 11

$$fPc = \frac{1}{2 \cdot \pi \cdot R5} \cdot \frac{C6 + C7}{C7 \cdot C6}$$

are chosen in order to ensure the stability of the overall system.

G_M is the VIPer01 transconductance, H_{COMP} = (V_{COMPH} - V_{COMPL})/(I_{DLIM} - I_{DLIM_PFM}) is the slope of the V_{COMP} vs. I_{DRAIN} characteristic

8.2 Compensation procedure

The first step is to choose the pole and zero of the compensator and the crossing frequency.

Equation 12

$$fZc = x \cdot fp$$

Equation 13

$$fPc = y \cdot fp$$

Equation 14

$$fcross \leq \frac{fsw}{10}$$

where x and y are given arbitrary values. G1(fcross) can be calculated from *Equation 5* and, since by definition │C(fcross)*G1(fcross)│= 1, C_0 is obtained from *Equation 8* as follows:

Equation 15

$$C_0 = \frac{|j \cdot 2 \cdot \pi \cdot fcross| \cdot |1 + \frac{j \cdot fcross}{fPc}|}{|1 + \frac{j \cdot fcross}{fZc}|} \cdot \frac{H_{COMP}}{|G1(fcross)|}$$

At this point the Bode diagram for G1(f)*C(f) can be plotted to check the phase margin for stability.

If the margin is not high enough, choose new fZc, fPc and fcross values and repeat the procedure.

When the stability is ensured, the next step is to find the values of the schematic components:

- R4 is set in the order of tens of kΩ
- R3 is calculated from *Equation 1*:

Equation 16

$$R3 = \frac{R4}{\frac{V_{OUT}}{V_{REF\_FB}} - 1}$$

C6 is calculated from *Equation9*, *Equation10* and *Equation11*:

Equation 17

$$C6 = \frac{fZc}{fPc} \cdot \frac{G_M}{|C_0|} \cdot \frac{R3}{R3 + R4}$$

C7 is calculated from *Equation10* and *Equation11*:

Equation 18

$$C7 = C6 \cdot \left(\frac{fPc}{fZc} - 1\right)$$

Finally, R5 is calculated from *Equation11*:

Equation 19

$$R5 = \frac{1}{2 \cdot \pi \cdot fPc} \cdot \frac{C6 + C7}{C6 \cdot C7}$$

After selecting commercial values for R3, R4, C6, C7 and R5, the actual values of C_0, fZc and fPc should be calculated with *Equation9*, *Equation10* and *Equation11* to obtain C_0_act, fZc_act and fPc_act respectively. Substituting these values in *Equation8*, the actual compensator, C_act(f), is obtained. The Bode diagram of G1(f)*C_act(f) can now be plotted to check whether the phase margin for stability is still guaranteed.

9 Thermal measurements

Thermal analysis of the board was performed using an IR camera at 90 V_{AC}, 115 V_{AC}, 230 V_{AC} and 265 V_{AC} mains input, full load condition and external biasing. The results are shown in the following figures.

Figure 37: Thermal measurements with IR camera at V_{IN} = 90 V_{AC}, I_{OUT} = 0.9 A, T_{AMB} = 25°C

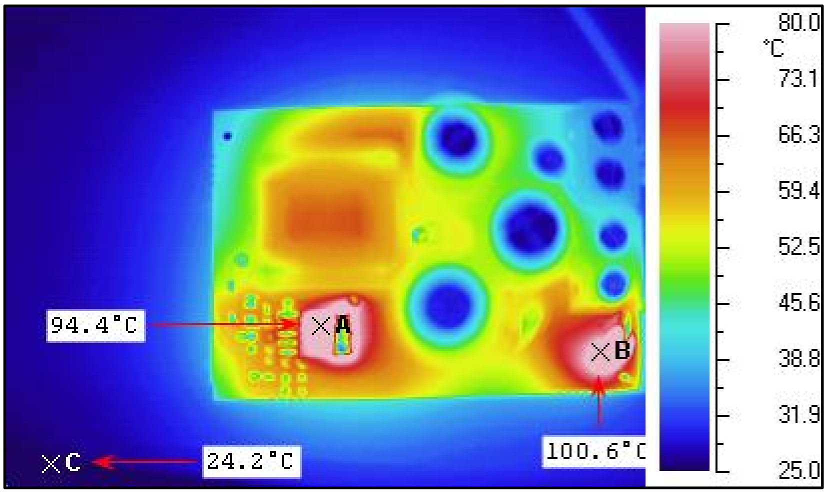


Figure 38: Thermal measurements with IR camera at V_{IN} = 115 V_{AC}, I_{OUT} = 0.9 A, T_{AMB} = 24°C

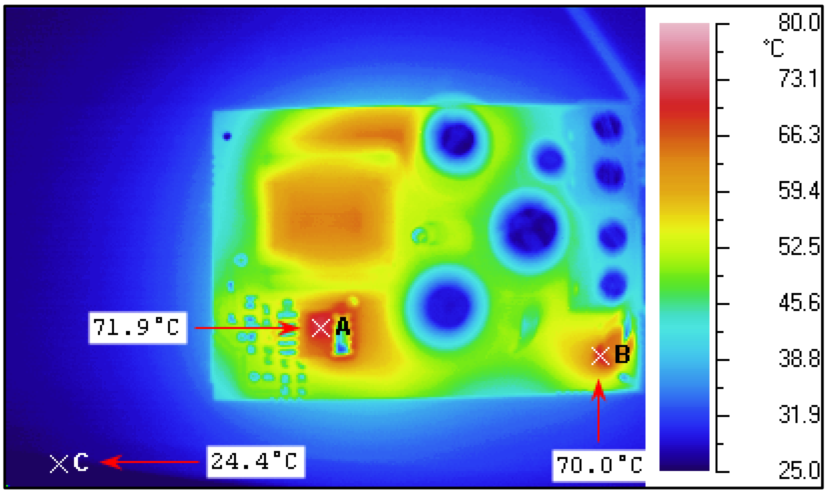


Figure 39: Thermal measurements with IR camera at V_{IN} = 230 V_{AC}, I_{OUT} = 0.9 A, T_{AMB} = 24°C

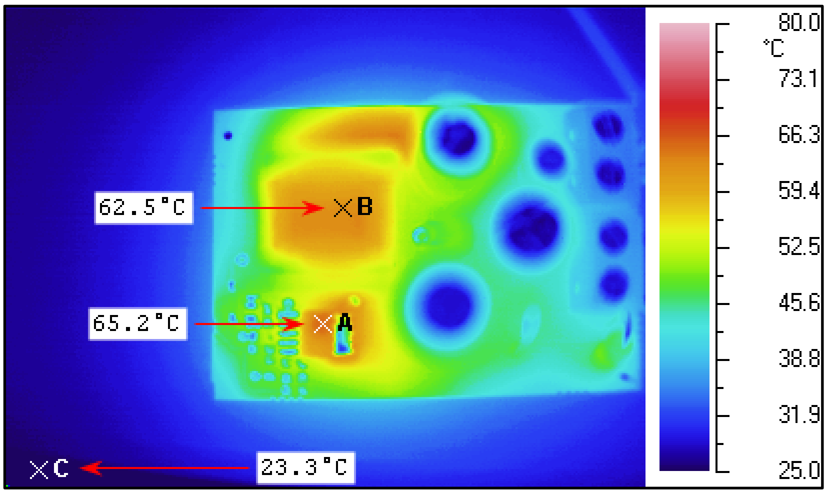
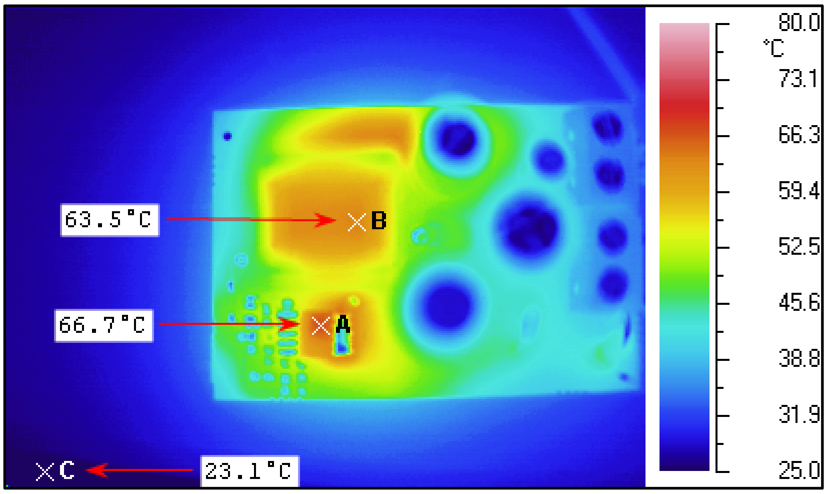


Figure 40: Thermal measurements with IR camera at V_{IN} = 265 V_{AC}, I_{OUT} = 0.9 A, T_{AMB} = 25°C



10 EMI measurements

A pre-compliance test for European normative EN55022 (Class B) was performed using an EMC analyzer with average detector and a line impedance stabilization network (LISN).

Figure 41: EMI measurements with average detector at 115 V_{AC}, full load, supply from output, T_{AMB} = 25°C

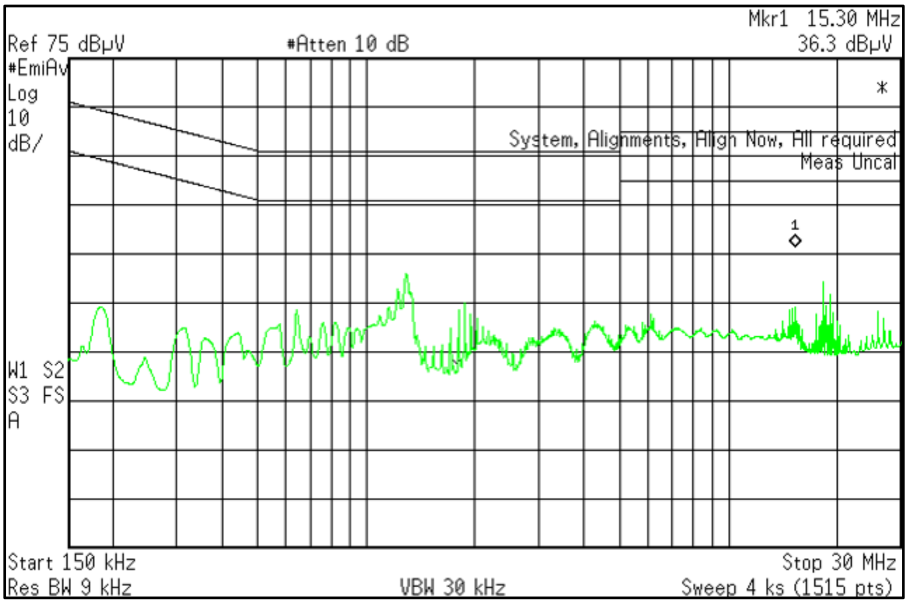
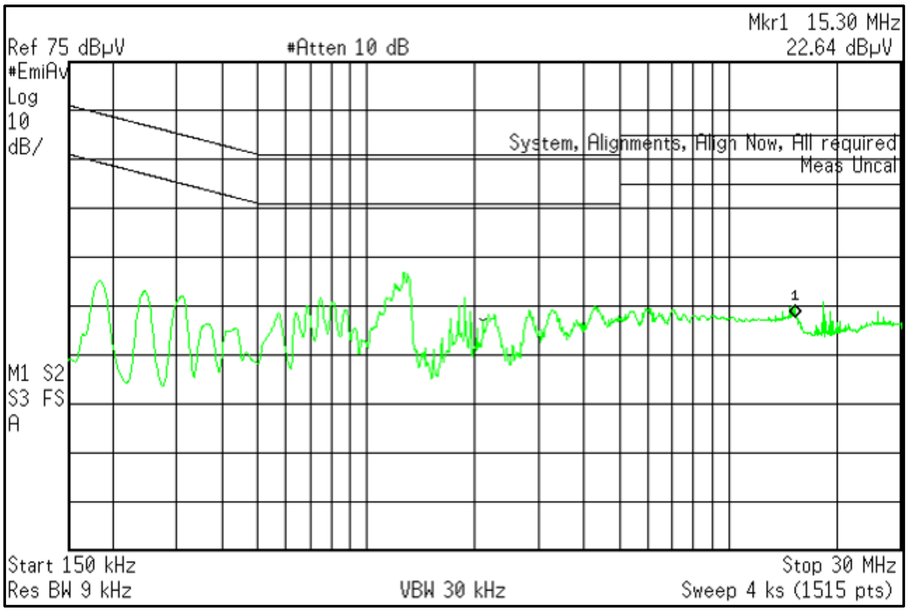


Figure 42: EMI measurements with average detector at 230 V_{AC}, full load, supply from output, T_{AMB} = 25°C



11 Conclusions

The STEVAL-ISA177V1 demonstrates that the VIPer01 facilitates the design of a non-isolated converter that is compliant with the most stringent energy regulations and which requires relatively few external components.

The STEVAL-ISA177V1 in fact consumes less than 10 mW at 230 V_{AC} mains under no load condition and can satisfy both CoC 5 and DOE low voltage external power supplies requirements for active mode and light load efficiency.

The 800 V avalanche rugged Power MOSFET and the embedded protections add reliability to the power converter, rendering the VIPer01 the ideal choice for applications requiring robustness and energy efficient performance.

12 Revision history

Table 9: Document revision history

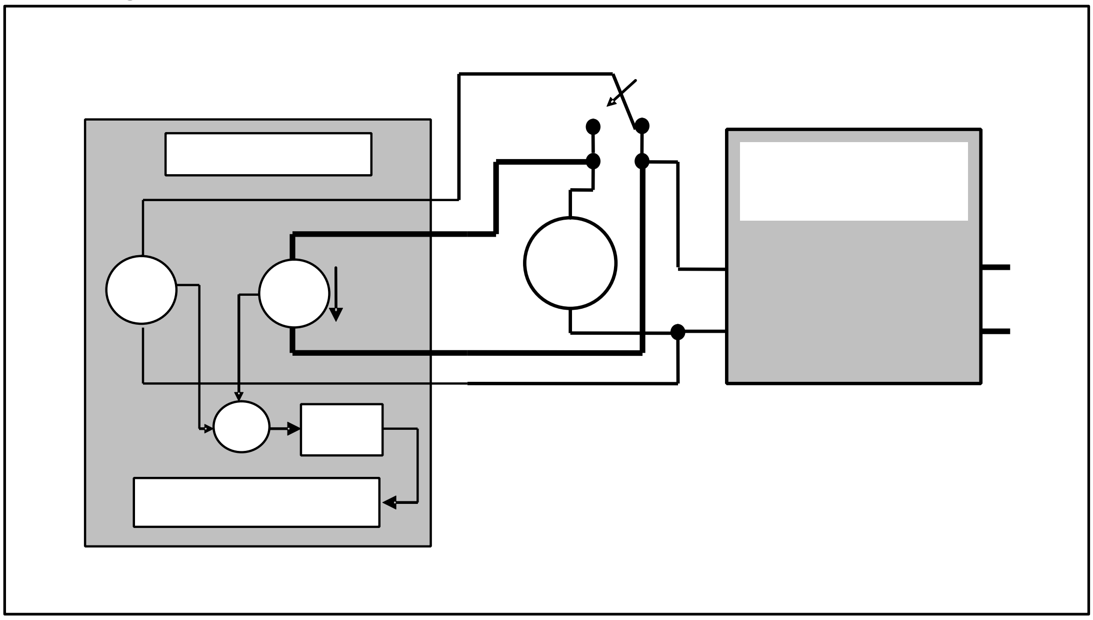
Date	Version	Changes
12-May-2016	1	Initial release.
03-Nov-2016	2	Updated *Table 2: "Bill of materials"*

Appendix A Test equipment and measurement of efficiency and light load performance

The converter input power is measured using a wattmeter. The wattmeter simultaneously measures the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The digital wattmeter samples the current and voltage and converts them in digital formats, which are then multiplied to give the instantaneous measured power. The sampling frequency is in the range of 20 kHz or higher and the average measured power over a short interval (1 s typ.) is displayed.

The following figure shows the wattmeter connection to the UUT (unit under test) and AC source, as well as the wattmeter internal block diagram.

Figure 43: Connections of the UUT to the wattmeter for power measurements



An electronic load is connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage is measured by a voltmeter. The output power is the product between load current and output voltage.

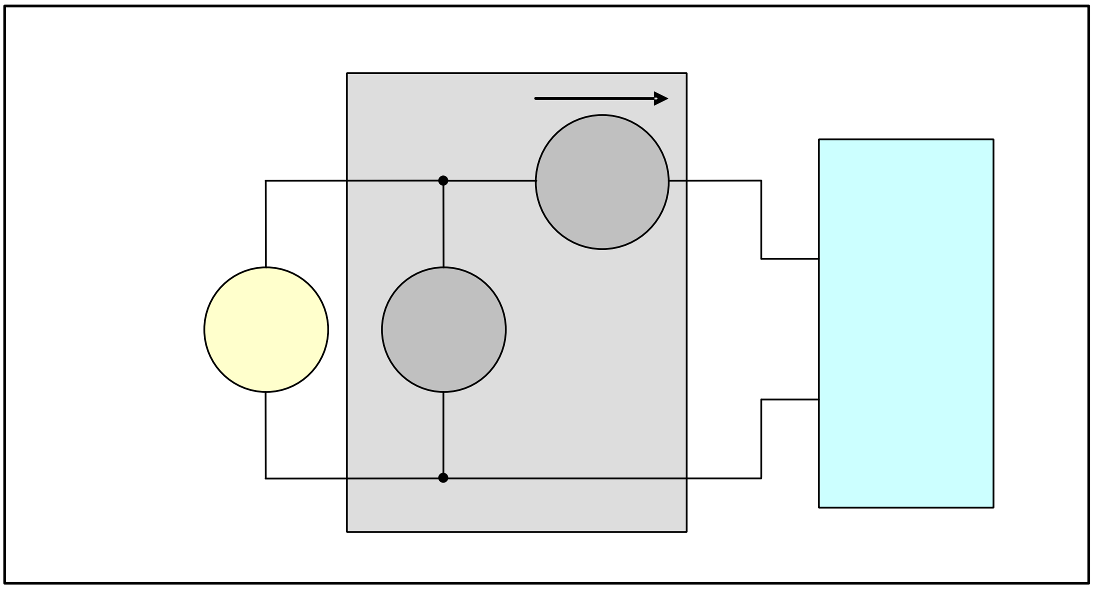
The ratio between the above output power calculation and the input power measured by the wattmeter is the converter's efficiency, measured under different input/output conditions.

Considerations when measuring input power

With reference to *Figure 43: "Connections of the UUT to the wattmeter for power measurements"*, the UUT input current causes a voltage drop across the ammeter internal shunt resistance (the ammeter is not ideal as it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

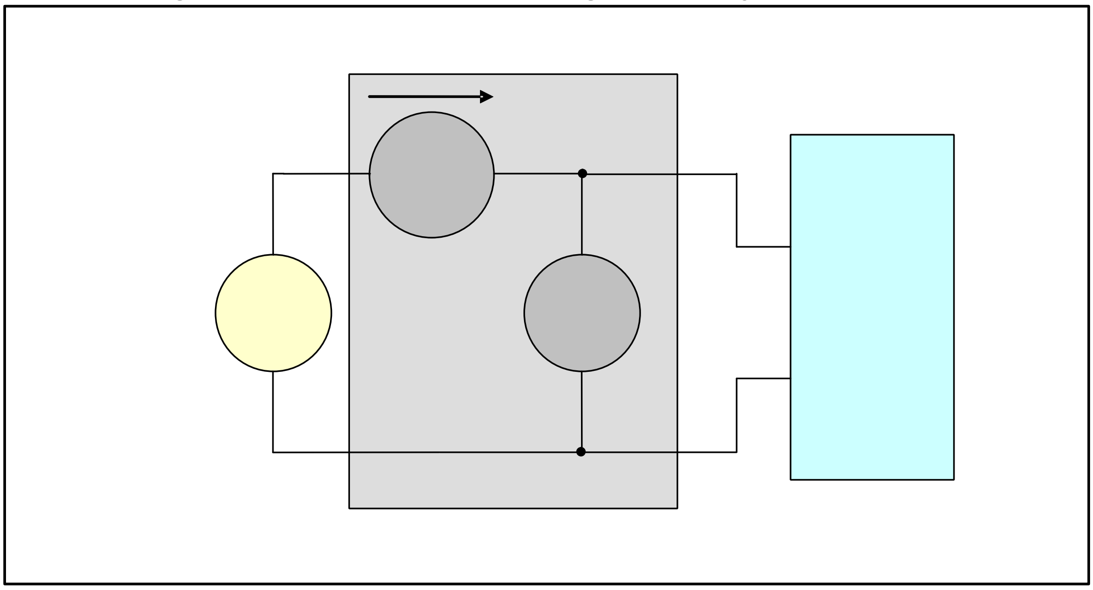
If the switch in *Figure 43: "Connections of the UUT to the wattmeter for power measurements"* is in position 1 (see the simplified schematic below) this voltage drop causes an input measured voltage higher than the input voltage at the UUT input, which of course distorts the measured power. The voltage drop is generally negligible if the UUT input current is low (e.g., the input power of UUT under low load condition).

Figure 44: Switch in position 1 - setting for standby measurements



For high UUT input currents (e.g., heavy load conditions), the voltage drop compared to the UUT real input voltage can become significant. In this case, the switch in *Figure 43: "Connections of the UUT to the wattmeter for power measurements"* should be set to position 2 (see the simplified schematic below), where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

Figure 45: Switch in position 2 - setting for efficiency measurements



On the other hand, the arrangement in *Figure 45: "Switch in position 2 - setting for efficiency measurements"* may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (not having infinite input resistance) is not negligible. This is why it is better to use the *Figure*

44: "Switch in position 1 - setting for standby measurements" arrangement for light load measurements and *Figure 45: "Switch in position 2 - setting for efficiency measurements"* for heavy loads.

If you are not certain which arrangement distorts the result less, try both and record the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT shall be operated at 100% of nameplate output current output for at least 30 minutes (warm up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the AC input power shall be monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5 minute period. If AC input power is not stable over a 5 minute period, the average power or accumulated energy shall be measured over time for both AC input and DC output.

Some wattmeter models allow integrating the measured input power over a time range and measuring the energy absorbed by the UUT during the integration time. Dividing by the integration time itself gives the average input power.