3.0 V to 5.5 V, ±12 kV IEC ESD Protected, 50 Mbps RS-485 Transceiver

Data Sheet

ADM3065E/ADM3066E

FEATURES

TIA/EIA RS-485 compliant over full supply range
3.0 V to 5.5 V operating voltage range on V_{CC}
1.62 V to 5.5 V V_{IO} logic supply
ESD protection on the bus pins
- IEC 61000-4-2 ≥ ±12 kV contact discharge
- IEC 61000-4-2 ≥ ±12 kV air discharge
- HBM ≥ ±30 kV

Full hot swap support (glitch free power-up/power-down)
High speed 50 Mbps data rate
Full receiver short circuit, open circuit, and bus idle fail-safe
Extended temperature range up to 125°C
Profibus compliant at V_{CC} ≥ 4.5 V
Half duplex
Allows connection of up to 128 nodes onto the bus
Space-saving package options
- 10-lead 3 mm × 3 mm LFCSP package
- 8-lead and 10-lead MSOP packages

APPLICATIONS

Industrial fieldbuses
Process control
Building automation
Profibus networks
Motor control servo drives and encoders

FUNCTIONAL BLOCK DIAGRAMS

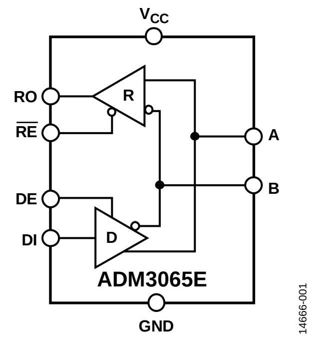

Figure 1. ADM3065E Functional Block Diagram

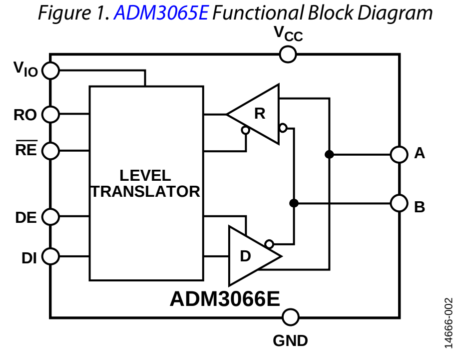

Figure 2. ADM3066E Functional Block Diagram

Table 1. Summary of the ADM3065E/ADM3066E Operating Conditions—Data Rate Capability Across Temperature, Power Supply, and Package

Maximum Data Rate (Mbps)[1]	Maximum V_{CC} (V)	Maximum Temperature	Package Description
50	5.5	−40°C to +125°C	10-lead LFCSP
50	5.5	−40°C to +105°C	8-lead SOIC_N, 8-lead MSOP, and 10-lead MSOP
50	3.6	−40°C to +125°C	8-lead SOIC_N, 8-lead MSOP, and 10-lead MSOP

[1] The ADM3065E data input (DI) is transmitting 50 Mbps clock data, and the ADM3065E driver enable (DE) is enabled for 50% of the DI transmit time.

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REVISION HISTORY

5/2017—Rev. 0 to Rev. A

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3/2017—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADM3065E is a 3.0 V to 5.5 V, IEC electrostatic discharge (ESD) protected RS-485 transceiver, allowing the device to withstand ±12 kV contact discharges on the transceiver bus pins without latch-up or damage. The ADM3066E features a V_{IO} logic supply pin allowing a flexible digital interface capable of operating as low as 1.62 V.

The ADM3065E/ADM3066E are suitable for high speed, 50 Mbps, bidirectional data communication on multipoint bus transmission lines. The ADM3065E/ADM3066E feature a ¼ unit load input impedance, which allows up to 128 transceivers on a bus.

The ADM3065E/ADM3066E are half-duplex RS-485 transceivers, fully compliant to the Profibus® standard with increased 2.1 V bus differential voltage at $V_{CC} \geq 4.5$ V.

The RS-485 transceivers are available in a number of space-saving packages, such as a 10-lead, 3 mm × 3 mm LFCSP package, an 8-lead, 3 mm × 3 mm MSOP package, a 10-lead, 3 mm × 3 mm MSOP package, and an 8-lead, narrow body SOIC package. Models with operating temperature ranges of −40°C to +125°C and −40°C to +85°C are available.

Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. If, during fault conditions, a significant temperature increase is detected in the internal driver circuitry, this feature forces the driver output into a high impedance state.

The ADM3065E/ADM3066E guarantee a logic high receiver output when the receiver inputs are shorted, open, or connected to a terminated transmission line with all drivers disabled.

Table 1 presents an overview of the ADM3065E/ADM3066E data rate capability across temperature, power supply, and package options. Refer to the Ordering Guide for model numbering.

SPECIFICATIONS

V_{CC} = 3.0 V to 5.5 V, V_{IO} = 1.62 V to V_{CC}, T_A = T_{MIN} (−40°C) to T_{MAX} (+125°C), unless otherwise noted. All typical specifications are at T_A = 25°C, V_{IO} = V_{CC} = 3.3 V unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
Supply Current	I_{CC}		2	7.5	mA	No load, DE = V_{CC}, $\overline{RE}$ = 0 V
				7.5	mA	No load, DE = V_{CC}, $\overline{RE}$ = V_{CC}
				4.5	mA	No load, DE = 0 V, $\overline{RE}$ = 0 V
				172	mA	50 Mbps, R_L = 54 Ω, DE = V_{CC}, $\overline{RE}$ = 0 V
			67	75	mA	50 Mbps, R_L = 54 Ω, DE = V_{CC}, $\overline{RE}$ = 0 V (V_{CC} = 3.0 V)
Supply Current in Shutdown Mode	I_{SHDN}			450	µA	DE = 0 V, $\overline{RE}$ = V_{CC}
Supply Current in Shutdown Mode	I_{IOSHDN}			50	µA	DE = 0 V, $\overline{RE}$ = V_{IO}
DRIVER						
Differential Outputs						
Output Voltage, Loaded	$\|V_{OD2}\|$	2.0		V_{CC}	V	V_{CC} ≥ 3.0 V, R = 50 Ω, see Figure 11
	$\|V_{OD2}\|$	1.5		V_{CC}	V	V_{CC} ≥ 3.0 V, R = 27 Ω (RS-485), see Figure 11
	$\|V_{OD2}\|$	2.1		V_{CC}		V_{CC} ≥ 4.5 V, R = 50 Ω, see Figure 11
	$\|V_{OD2}\|$	2.1		V_{CC}	V	V_{CC} ≥ 4.5 V, R = 27 Ω (RS-485), see Figure 11
	$\|V_{OD3}\|$	1.5		V_{CC}	V	V_{CC} ≥ 3.0 V, −7 V ≤ V_{CM} ≤ +12 V, see Figure 12
	$\|V_{OD3}\|$	2.1		V_{CC}	V	V_{CC} ≥ 4.5 V, −7 V ≤ V_{CM} ≤ +12 V, see Figure 12
Δ$\|V_{OD}\|$ for Complementary Output States	Δ$\|V_{OD}\|$			0.2	V	R = 27 Ω or 50 Ω, see Figure 11
Common-Mode Output Voltage	V_{OC}			3.0	V	R = 27 Ω or 50 Ω, see Figure 11
Δ$\|V_{OC}\|$ for Complementary Output States	Δ$\|V_{OC}\|$			0.2	V	R = 27 Ω or 50 Ω, see Figure 11
Output Short-Circuit Current	I_{OS}	−250		250	mA	−7 V < V_{OUT} < +12 V
Logic Inputs (DE, $\overline{RE}$, DI)						
Input Voltage						
Low	V_{IL}			0.33 × V_{IO}	V	DE, $\overline{RE}$, DI, 1.62 V ≤ V_{IO} ≤ 5.5 V
High	V_{IH}	0.67 × V_{IO}			V	DE, $\overline{RE}$, DI, 1.62 V ≤ V_{IO} ≤ 5.5 V
Input Current	I_I	−2		+2	µA	DE, $\overline{RE}$, DI, 1.62 V ≤ V_{IO} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{IO}
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage	V_{TH}	−200	−125	−30	mV	−7 V < V_{CM} < +12 V
Input Voltage Hysteresis	V_{HYS}		30		mV	−7 V < V_{CM} < +12 V
Input Current (A, B)	I_I			0.25	mA	DE = 0 V, V_{CC} = powered/unpowered, V_{IN} = 12 V
		−0.20			mA	DE = 0 V, V_{CC} = powered/unpowered, V_{IN} = −7 V
Line Input Resistance	R_{IN}	48			kΩ	−7 V ≤ V_{TST} ≤ +12 V
Logic Outputs						
Output Voltage						
Low	V_{OL}			0.4	V	V_{IO} = 3.6 V, I_{OUT} = +2 mA, V_{ID} ≤ −0.2 V
				0.4	V	V_{IO} = 2.7 V, I_{OUT} = +1 mA, V_{ID} ≤ −0.2 V
				0.2	V	V_{IO} = 1.95 V, I_{OUT} = +500 µA, V_{ID} ≤ −0.2 V
High	V_{OH}	2.4			V	V_{IO} = 3.0 V, I_{OUT} = −2 mA, V_{ID} ≥ +0.2 V
		2.0			V	V_{IO} = 2.3 V, I_{OUT} = −1 mA, V_{ID} ≥ +0.2 V
		V_{IO} − 0.2			V	V_{IO} = 1.65 V, I_{OUT} = −500 µA, V_{ID} ≥ +0.2 V
Short-Circuit Current				85	mA	V_{OUT} = GND or V_{CC}
Three-State Output Leakage	I_{OZR}			±2	µA	RO = 0 V or V_{CC}

TIMING SPECIFICATIONS

V_{CC} = 3.0 V to 5.5 V, V_{IO} = 1.62 V to V_{CC}, T_A = T_{MIN} (−40°C) to T_{MAX} (+125°C), unless otherwise noted. All typical specifications are at T_A = 25°C, V_{IO} = V_{CC} = 3.3 V unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate[1]		50			Mbps	
Propagation Delay	t_{DPLH}, t_{DPHL}		9	15	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 13
Skew	t_{DSKEW}		1	2	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 13
Rise/Fall Times	t_{DR}, t_{DF}		4	6.7	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 13
Enable to Output High	t_{DZH}		10	30	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 14
Enable to Output Low	t_{DZL}		10	30	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 14
Disable Time from Low	t_{DLZ}		10	30	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 14
Disable Time from High	t_{DHZ}		10	30	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 14
Enable Time from Shutdown to High	$t_{DZH(SHDN)}$			2000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 14
Enable Time from Shutdown to Low	$t_{DZL(SHDN)}$			2000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 14
RECEIVER						
Maximum Data Rate		50			Mbps	
Propagation Delay	t_{RPLH}, t_{RPHL}			35	ns	C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, see Figure 15
Skew/Pulse Width Distortion	t_{RSKEW}			3	ns	C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, V_{CM} = 1.5 V, see Figure 15
Enable to Output High	t_{RZH}		10	35	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, DE high, see Figure 17
Enable to Output Low	t_{RZL}		10	35	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, DE high, see Figure 17
Disable Time from Low	t_{RLZ}		10	35	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, see Figure 17
Disable Time from High	t_{RHZ}		10	35	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, see Figure 17
Enable from Shutdown to High	$t_{RZH(SHDN)}$			2000	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, see Figure 16
Enable from Shutdown to Low	$t_{RZL(SHDN)}$			2000	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, see Figure 16
TIME TO SHUTDOWN	t_{SHDN}	40			ns	

[1] Maximum data rate assumes a ratio of t_{DR}:t_{BIT}:t_{DF} equal to 1:1:1.

Timing Diagrams

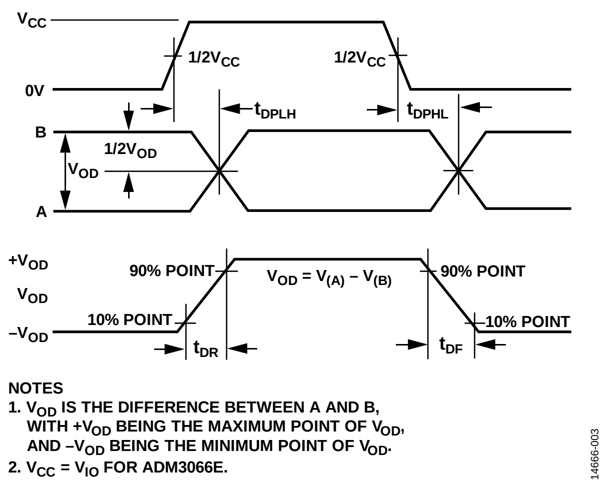

Figure 3. Driver Propagation Delay Rise and Fall Timing Diagram

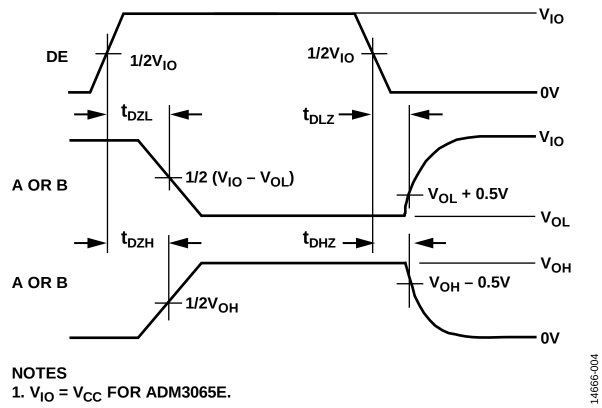

Figure 4. Driver Enable and Disable Timing Diagram

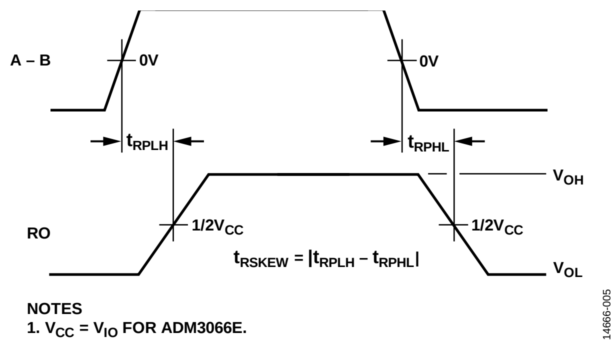

Figure 5. Receiver Propagation Delay Timing Diagram

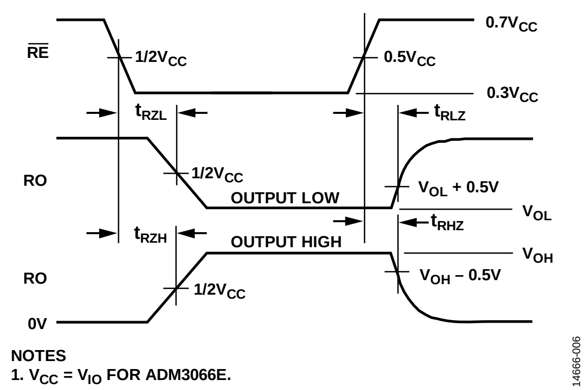

Figure 6. Receiver Enable and Disable Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{CC} to GND	6 V
V_{IO} to GND	−0.3 V to 6 V
Digital Input/Output Voltage (DE, $\overline{RE}$, DI, and RO)	−0.3 V to V_{CC} + 0.3 V
Driver Output/Receiver Input Voltage	−9 V to +14 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to + 150°C
Continuous Total Power Dissipation	
8-Lead SOIC_N	0.225 W
8-Lead MSOP	0.151 W
Maximum Junction Temperature	150°C
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD on the Bus Pins (A and B)	
IEC 61000-4-2 Contact Discharge	±12 kV
IEC 61000-4-2 Air Discharge	
Ten Positive and Ten Negative Discharges	±12 kV
Three Positive or Negative Discharges	±15 kV
ESD Human Body Model (HBM)	
On the Bus Pins (A and B)	>±30 kV
All Other Pins	±8 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
R-8	110.88	58.63	°C/W
RM-8	165.69	49.61	°C/W
RM-10	165.69	49.61	°C/W
CP-10	55.65	33.22	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

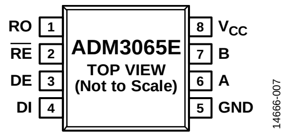

Figure 7. ADM3065E 8-Lead Narrow Body SOIC_N Pin Configuration

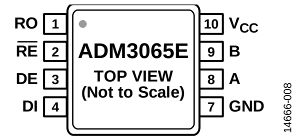

Figure 8. ADM3065E 8-Lead MSOP Pin Configuration

Table 6. ADM3065E Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output Data. This output is high when (A − B) > −30 mV and low when (A − B) < −200 mV. This output is tristated when the receiver is disabled; that is, when $\overline{RE}$ is driven high.
2	$\overline{RE}$	Receiver Enable Input. This is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
3	DE	Driver Output Enable. A high level on this pin enables the driver differential outputs, A and B. A low level places the driver output into a high impedance state.
4	DI	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
5	GND	Ground.
6	A	Noninverting Driver Output/Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
7	B	Inverting Driver Output/Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
8	V_{CC}	3 V to 5.5 V Power Supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.

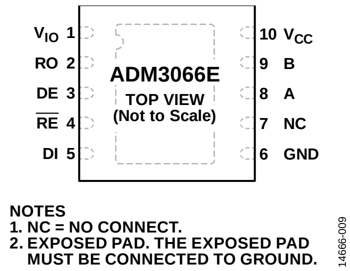

Figure 9. ADM3066E 10-Lead LFCSP Pin Configuration

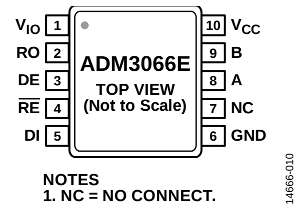

Figure 10. ADM3066E 10-Lead MSOP Pin Configuration

Table 7. ADM3066E Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{IO}	1.62 V to 5.5 V Logic Supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.
2	RO	Receiver Output Data. This output is high when (A − B) > −30 mV and low when (A − B) < −200 mV. This output is tristated when the receiver is disabled; that is, when $\overline{RE}$ is driven high.
3	DE	Driver Output Enable. A high level on this pin enables the driver differential outputs, A and B. A low level places the driver output into a high impedance state.
4	$\overline{RE}$	Receiver Enable Input. This is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
5	DI	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
6	GND	Ground.
7	NC	No Connect. Do not connect to this pin.
8	A	Noninverting Driver Output/Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
9	B	Inverting Driver Output/Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
10	V_{CC}	3 V to 5.5 V Power Supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.
	EPAD	Exposed Pad. The exposed pad must be connected to ground.

TEST CIRCUITS

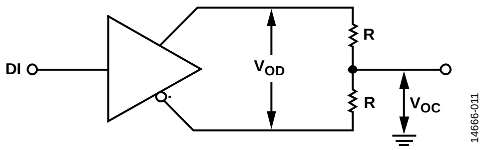

Figure 11. Driver Voltage Measurements

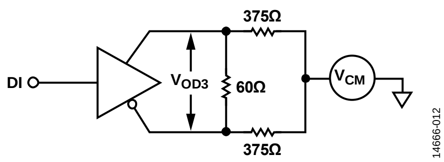

Figure 12. Driver Voltage Measurements over Common-Mode Range

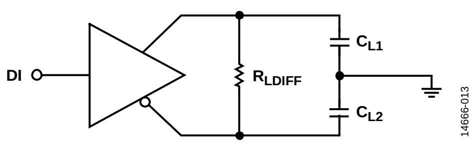

Figure 13. Driver Propagation Delay

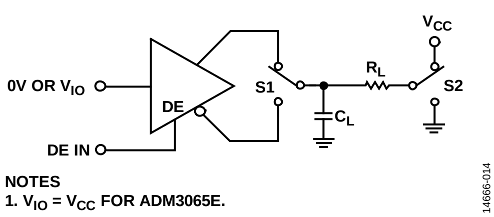

Figure 14. Driver Enable/Disable

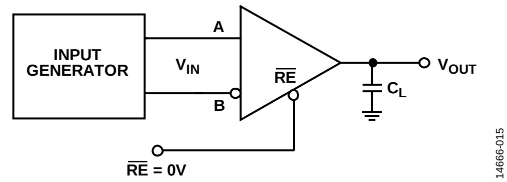

Figure 15. Receiver Propagation Delay/Skew

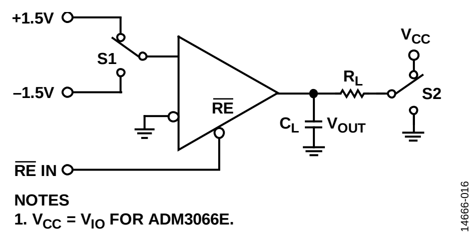

Figure 16. Receiver Enable/Disable from Shutdown

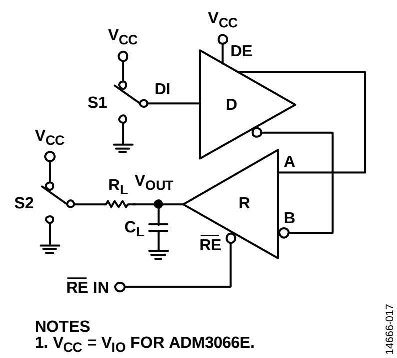

Figure 17. Receiver Enable/Disable

TYPICAL PERFORMANCE CHARACTERISTICS

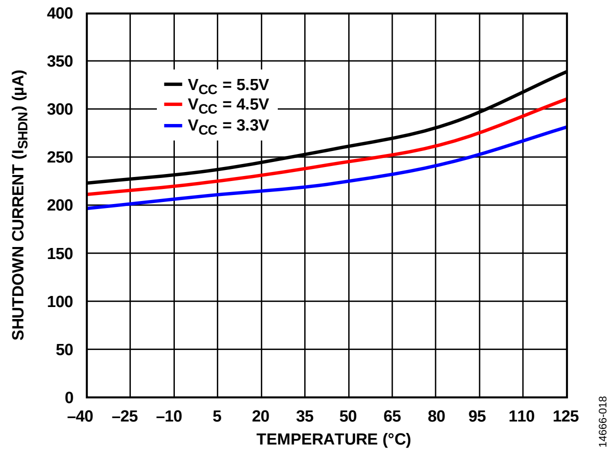

Figure 18. Shutdown Current (I_{SHDN}) vs. Temperature

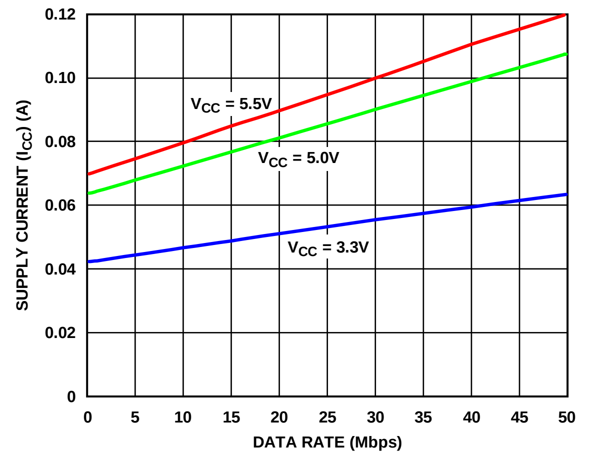

Figure 21. Supply Current (I_{CC}) vs. Data Rate with 54 Ω Load Resistance

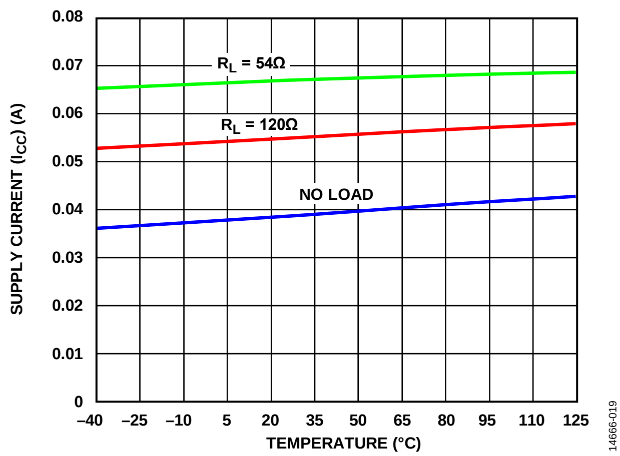

Figure 19. Supply Current (I_{CC}) vs. Temperature, Data Rate = 50 Mbps, V_{CC} = 3.3 V

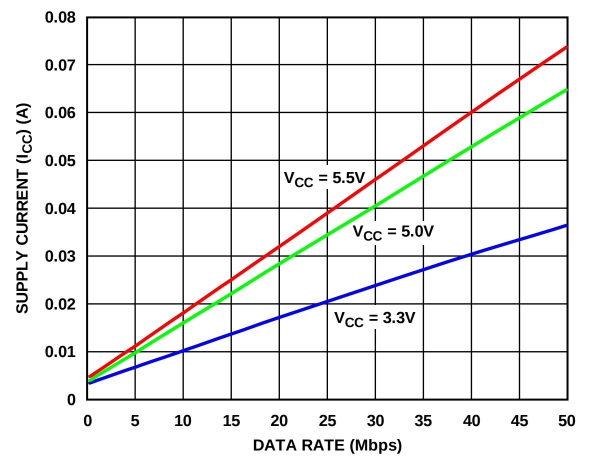

Figure 22. Supply Current (I_{CC}) vs. Data Rate with No Load Resistance

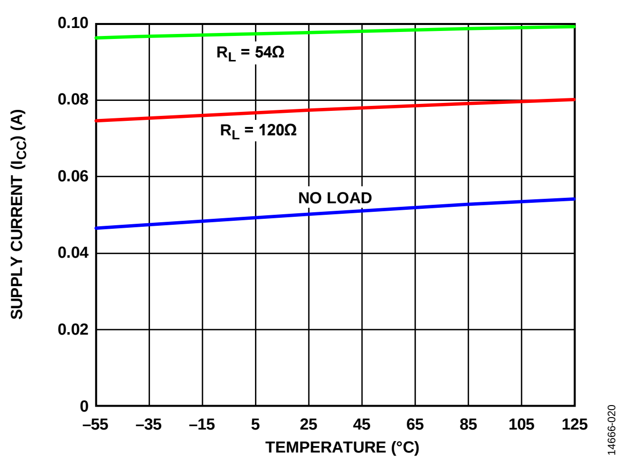

Figure 20. Supply Current (I_{CC}) vs. Temperature, Data Rate = 50 Mbps, V_{CC} = 5.0 V

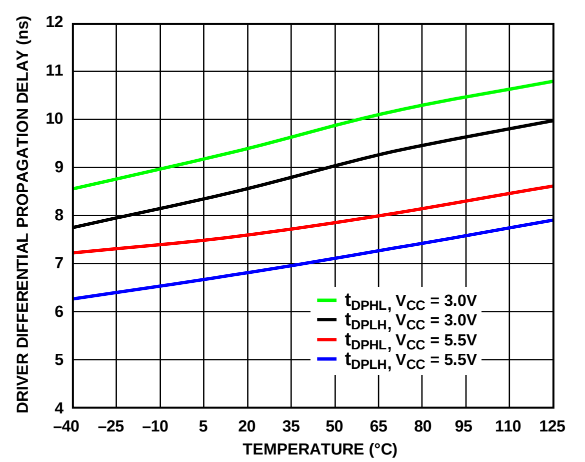

Figure 23. Driver Differential Propagation Delay vs. Temperature, 50 Mbps

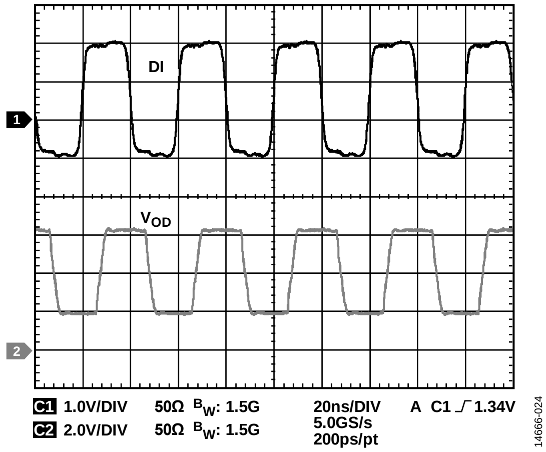

Figure 24. Driver Propagation Delay at 50 Mbps

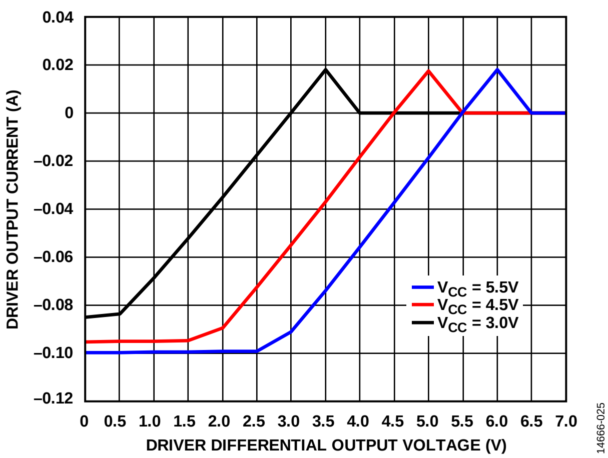

Figure 25. Driver Output Current vs. Driver Differential Output Voltage

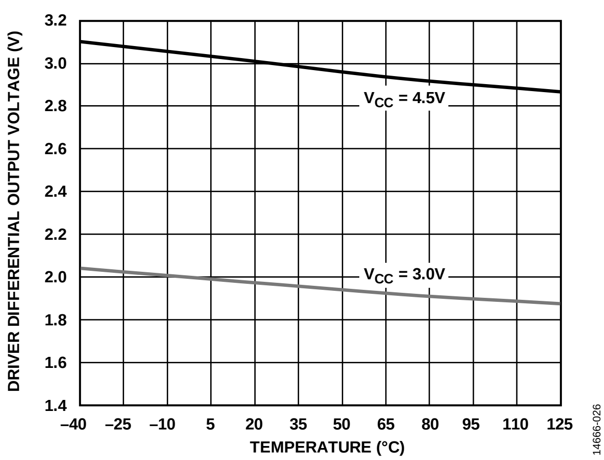

Figure 26. Driver Differential Output Voltage vs. Temperature

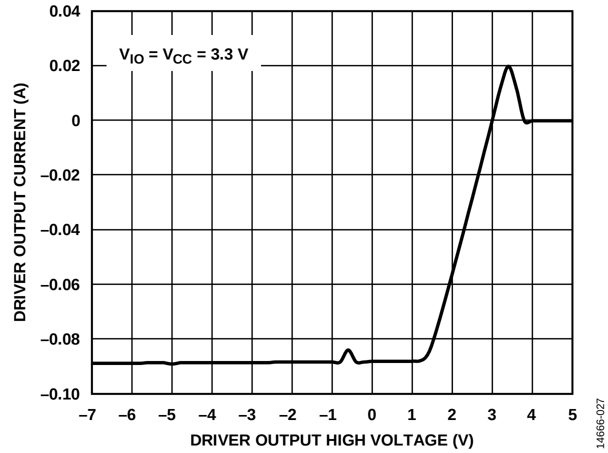

Figure 27. Driver Output Current vs. Driver Output High Voltage

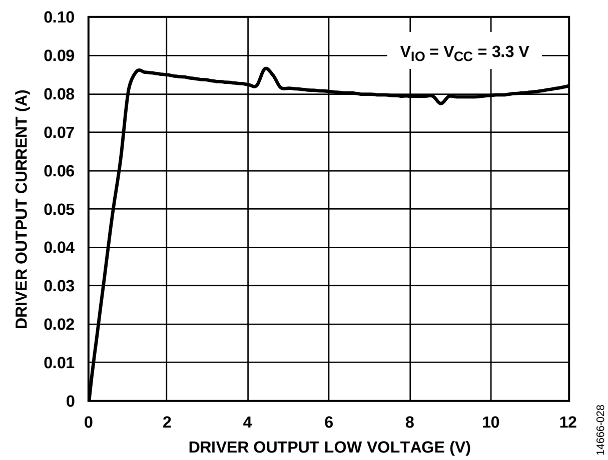

Figure 28. Driver Output Current vs. Driver Output Low Voltage

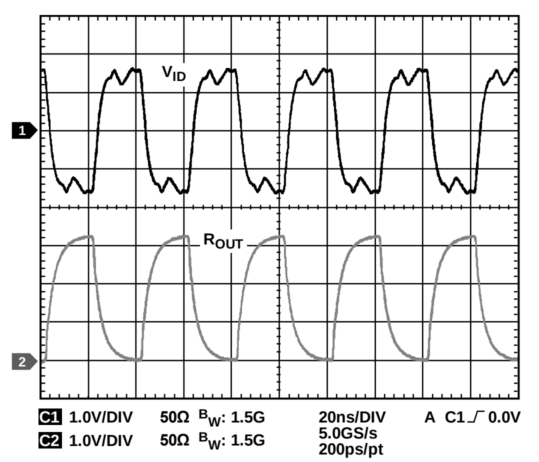

Figure 29. Receiver Propagation Delay at 50 Mbps, $|V_{ID}| \geq 1.5$ V

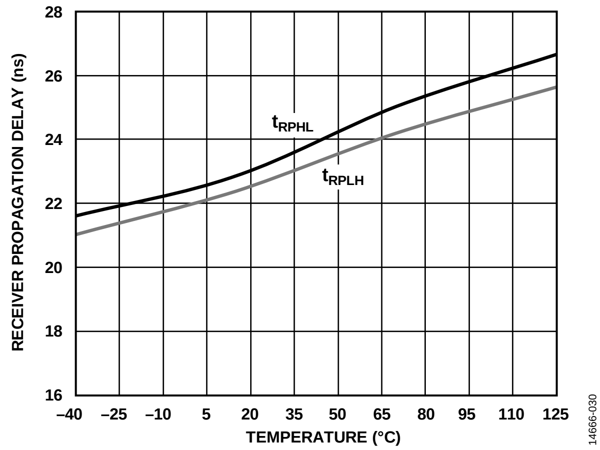

Figure 30. Receiver Propagation Delay vs. Temperature, 50 Mbps

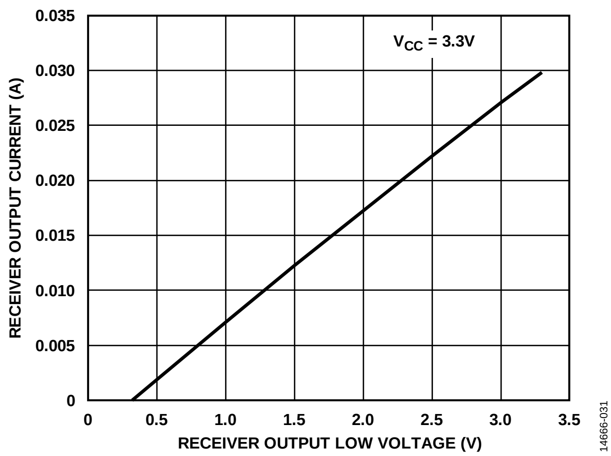

Figure 31. Receiver Output Current vs. Receiver Output Low Voltage (V_{CC} = 3.3 V)

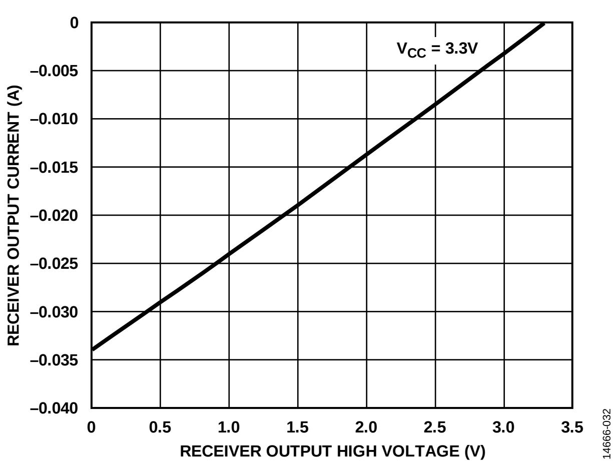

Figure 32. Receiver Output Current vs. Receiver Output High Voltage (V_{CC} = 3.3 V)

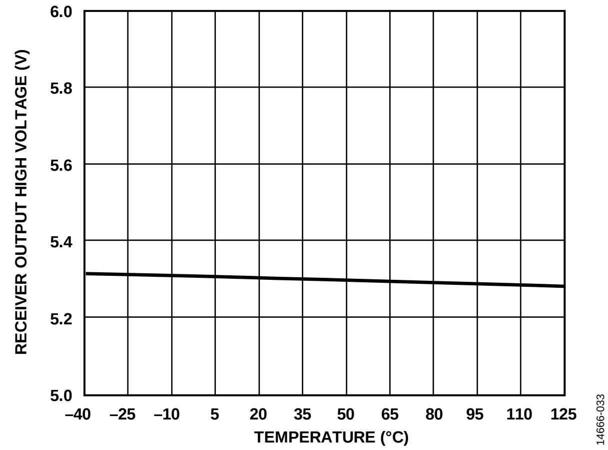

Figure 33. Receiver Output High Voltage vs. Temperature

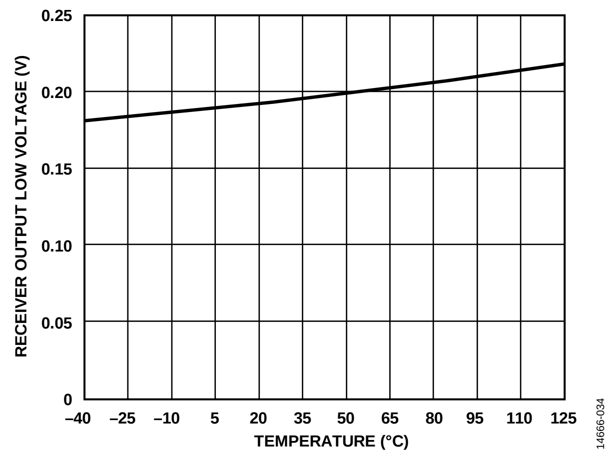

Figure 34. Receiver Output Low Voltage vs. Temperature

THEORY OF OPERATION

HIGH SPEED IEC ESD PROTECTED RS-485

The ADM3065E/ADM3066E are 3.0 V to 5.5 V, 50 Mbps RS-485 transceivers with IEC 61000-4-2 Level 4 ESD protection on the bus pins. The ADM3065E/ADM3066E can withstand up to ±12 kV contact discharge on transceiver bus pins (A and B) without latch-up or damage.

HIGH DRIVER DIFFERENTIAL OUTPUT VOLTAGE

The ADM3065E/ADM3066E have characteristics optimized for use in Profibus applications. When powered at $V_{CC} \geq 4.5$ V, the ADM3065E/ADM3066E driver output differential voltage meets or exceeds the Profibus requirements of 2.1 V with a 54 Ω load.

IEC 61000-4-2 ESD PROTECTION

ESD is the sudden transfer of electrostatic charge between bodies at different potentials caused by near contact or induced by an electric field. It has the characteristics of high current in a short time period. The primary purpose of the IEC 61000-4-2 test is to determine the immunity of systems to external ESD events outside the system during operation. IEC 61000-4-2 describes testing using two coupling methods: contact discharge and air discharge. Contact discharge implies a direct contact between the discharge gun and the equipment under test (EUT). During air discharge testing, the charged electrode of the discharge gun is moved toward the EUT until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the EUT. A number of factors affect the results and repeatability of the air discharge test, including humidity, temperature, barometric pressure, distance, and rate of approach to the EUT. This method is a better representation of an actual ESD event but is not as repeatable. Therefore, contact discharge is the preferred test method.

During testing, the data port is subjected to at least 10 positive and 10 negative single discharges. Selection of the test voltage is dependent on the system end environment.

Figure 35 shows the 8 kV contact discharge current waveform as described in the IEC 61000-4-2 specification. Some of the key waveform parameters are rise times of less than 1 ns and pulse widths of approximately 60 ns.

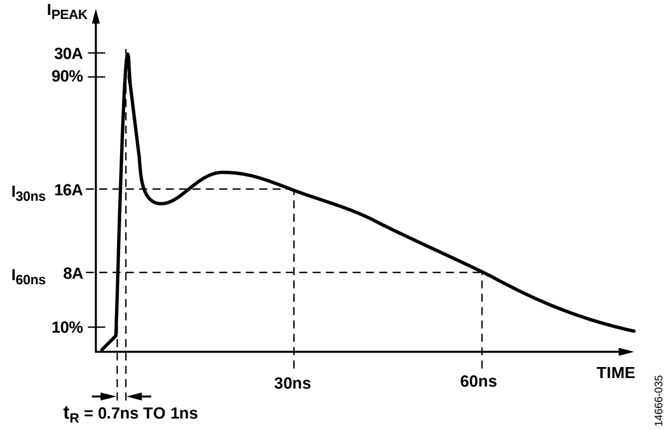

Figure 35. IEC 61000-4-2 ESD Waveform (8 kV)

Figure 36 shows the 8 kV contact discharge current waveform from the IEC 61000-4-2 standard compared to the human body model (HBM) ESD 8 kV waveform. Figure 36 shows that the two standards specify a different waveform shape and peak current. The peak current associated with an IEC 61000-4-2 8 kV pulse is 30 A, whereas the corresponding peak current for HBM ESD is more than five times less, at 5.33 A. The other difference is the rise time of the initial voltage spike, with the IEC 61000-4-2 ESD waveform having a much faster rise time of 1 ns, compared to the 10 ns associated with the HBM ESD waveform. The amount of power associated with an IEC ESD waveform is much greater than that of an HBM ESD waveform. The HBM ESD standard requires the EUT to be subjected to three positive and three negative discharges, while in comparison, the IEC ESD standard requires 10 positive and 10 negative discharge tests.

The ADM3065E/ADM3066E with IEC 61000-4-2 ESD ratings is better suited for operation in harsh environments compared to other RS-485 transceivers that state varying levels of HBM ESD protection.

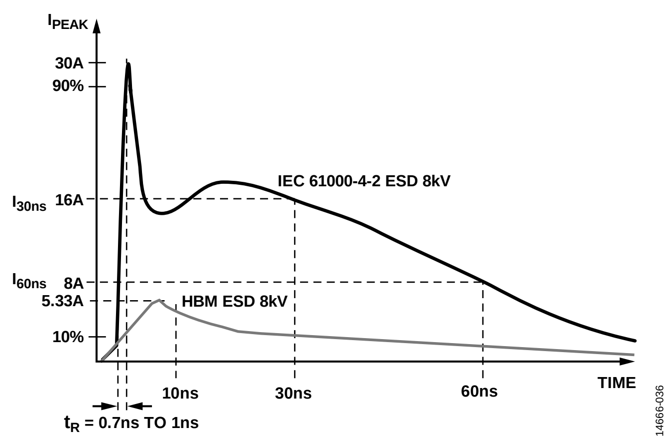

Figure 36. IEC 61000-4-2 ESD Waveform 8 kV Compared to HBM ESD Waveform 8 kV

TRUTH TABLES

Table 8. Transmitting Truth Table

Supply Status		Inputs			Outputs	
V_{IO}	V_{CC}	$\overline{RE}$	DE	DI	A	B
On	On	X[1]	1	1	1	0
On	On	X[1]	1	0	0	1
On	On	0	0	X[1]	High-Z[2]	High-Z[2]
On	On	1	0	X[1]	High-Z[2]	High-Z[2]
On	Off	X[1]	1	1	I[3]	I[3]
On	Off	X[1]	1	0	I[3]	I[3]
On	Off	X[1]	0	X[1]	I[3]	I[3]
Off	On	X[1]	X[1]	X[1]	High-Z[2]	High-Z[2]
Off	Off	X[1]	X[1]	X[1]	High-Z[2]	High-Z[2]

[1] X means don't care.
[2] High-Z means high impedance.
[3] I means indeterminate

Table 9. Receiving Truth Table

Supply Status		Inputs			Outputs
V_{IO}	V_{CC}	A – B	$\overline{RE}$	DE	RO
On	On	>−0.03 V	0	X[1]	1
On	On	<−0.2 V	0	X[1]	0
Off	On	>−0.03 V	0	X[1]	I[3]
Off	On	<−0.2 V	0	X[1]	I[3]
On	On	−0.2 V<A – B<−0.03 V	0	X[1]	I[3]
Off	On	−0.2 V<A – B<−0.03 V	0	X[1]	I[3]
On	On	Inputs open/shorted	0	X[1]	1
Off	On	Inputs open/shorted	0	X[1]	High-Z[2]
On	On	X[1]	1	X[1]	High-Z[2]
On	On	X[1]	1	0	Shutdown
Off	On	X[1]	1	X[1]	I[3]
Off	Off	X[1]	X[1]	X[1]	High-Z[2]

[1] X means don't care.
[2] High-Z means high impedance.
[3] I means indeterminate

RECEIVER FAIL-SAFE

The ADM3065E/ADM3066E guarantee a logic high receiver output when the receiver inputs are shorted, open, or connected to a terminated transmission line with all drivers disabled; set the receiver input threshold between −30 mV and −200 mV. If the differential receiver input voltage (A – B) is greater than or equal to −30 mV, the RO pin is logic high.

If the A – B input is less than or equal to −200 mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver differential input voltage is pulled to 0 V by the termination, resulting in a logic high with a 30 mV minimum noise margin.

HOT SWAP CAPABILITY

Hot Swap Inputs

When a circuit board is inserted into a powered (or hot) backplane, differential disturbances to the data bus can lead to data errors. During this period, processor logic output drivers are high impedance and are unable to drive the DE and $\overline{RE}$ inputs of the RS-485 transceivers to a defined logic level. Leakage currents up to ±10 µA from the high impedance state of the processor logic drivers can cause standard CMOS enable inputs of a transceiver to drift to an incorrect logic level. Additionally, parasitic circuit board capacitance can cause coupling of V_{CC} or GND to the enable inputs. Without the hot swap capability, these factors can improperly enable the driver or receiver of the transceiver. When V_{CC} or V_{IO} rises, an internal pull-down circuit holds DE low and $\overline{RE}$ high. After the initial power-up sequence, the pull-down circuit becomes transparent resetting the hot swap tolerable input.

128 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12 kΩ (1 unit load), and the standard driver can drive up to 32 unit loads. The ADM3065E/ADM3066E transceivers have a ¼ unit load receiver input impedance (48 kΩ), allowing up to 128 transceivers to be connected in parallel on one communication line. Any combination of these devices and other RS-485 transceivers with a total of 32 unit loads or fewer can be connected to the line.

DRIVER OUTPUT PROTECTION

The ADM3065E/ADM3066E features two methods to prevent excessive output current and power dissipation caused by faults or by bus contention. Current limit protection on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. In addition, a thermal shutdown circuit forces the driver outputs into a high impedance state if the die temperature rises excessively. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are reenabled at a temperature of 140°C.

APPLICATIONS INFORMATION

The ADM3065E transceiver is designed for bidirectional data communications on multipoint bus transmission lines. Figure 37 shows a typical network applications circuit.

To minimize reflections, terminate the line at both ends with a termination resistor (the value of the termination resistor must be equal to the characteristic impedance of the cable used) and keep stub lengths off the main line as short as possible.

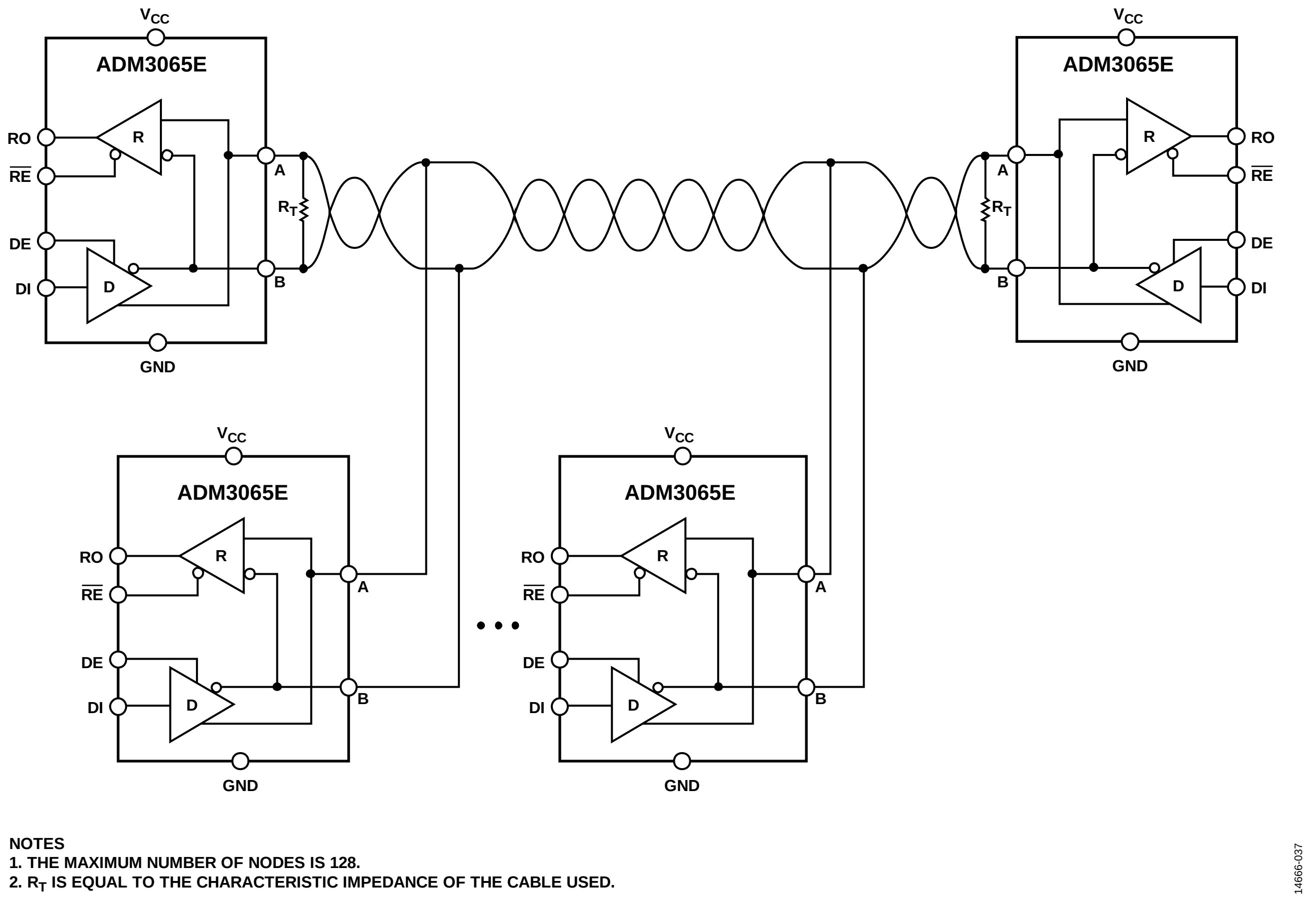

Figure 37. ADM3065E Typical Half-Duplex RS-485 Communications Network

ISOLATED HIGH SPEED RS-485 NODE

Galvanic isolation, with reinforced insulation and 5 kV rms transient withstand voltage, can be added to the ADM3065E using Analog Devices, Inc., *i*Coupler® and *iso*Power® technology. The ADuM6401 provides the required four channels of 5 kV rms signal isolation, operating at rates up to 25 Mbps, together with an integrated dc-to-dc converter. The ADuM6401 combines with the ADM3065E shown in Figure 38, with the V_{ISO} pin configured for 3.3 V by connecting the V_{SEL} pin to GND_{ISO} and a 5 V supply connected to V_{DD1}. Operation at 3.3 V ensures the ADM3065E remains within the load capability of ADuM6401 even at 25 Mbps.

Operation at 50 Mbps data rates with isolation of the ADM3065E can be implemented using the ADuM241D quad-channel digital isolator and the ADuM6000 isolated dc-to-dc converter, as shown in Figure 39. The ADuM241D can operate at a data rate of up to 150 Mbps, offering the precise timing required to fully support the ADM3065E at 50 Mbps.

Operation of ADM3065E at 3.3 V allows operation at the 50 Mbps data rate.

If 5 V operation is desired, V_{SEL} on ADuM6000 can be tied to V_{ISO}, and the maximum supported data rate becomes lower (for example, <10 Mbps). Refer to the Typical Performance Characteristics section, ADuM241D data sheet, and the ADuM6000 data sheet.

The dc-to-dc converters in the ADuM6401 and ADuM6000 *iso*Power devices provide regulated, isolated power to the ADM3065E (and the ADuM241D). These *iso*Power devices use high frequency switching elements to transfer power through their transformers. Take care during printed circuit board (PCB) layout to meet emissions standards. See the AN-0971 Application Note for PCB layout recommendations.

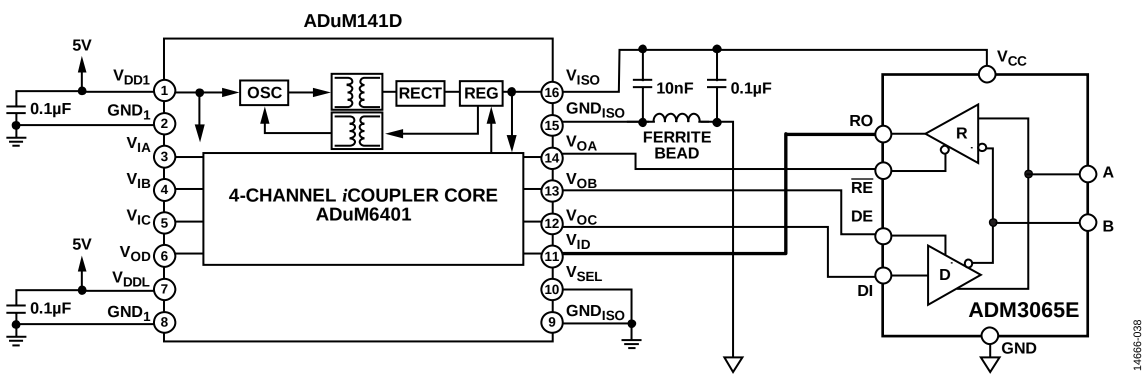

Figure 38. Signal and Power Isolated 50 Mbps RS-485 Solution (Simplified Diagram—All Connections Not Shown)

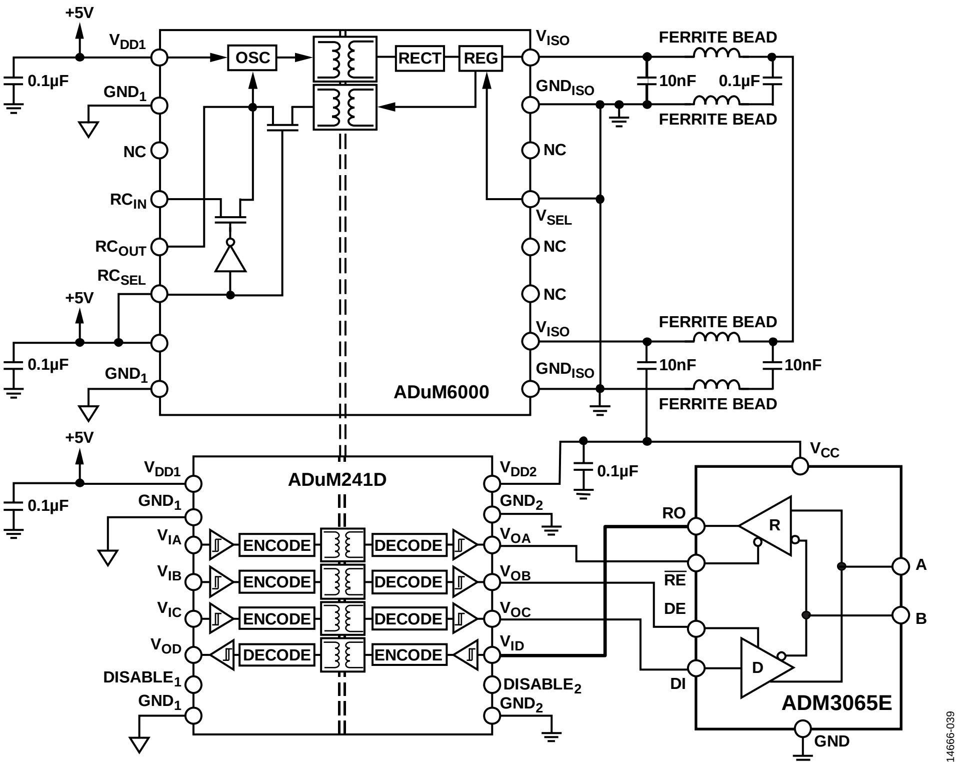

Figure 39. Signal and Power Isolated 25 Mbps RS-485 Solution (Simplified Diagram—All Connections Not Shown)

OUTLINE DIMENSIONS

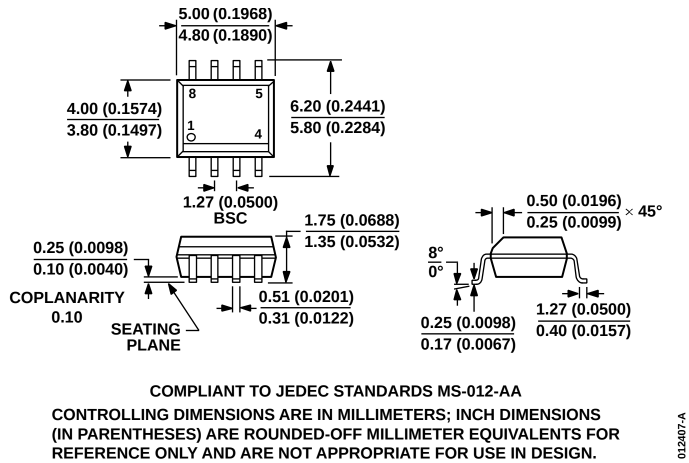

Figure 40. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

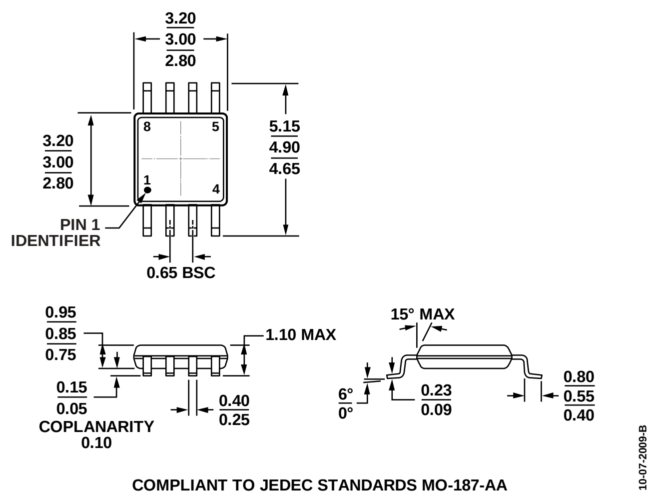

Figure 41. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

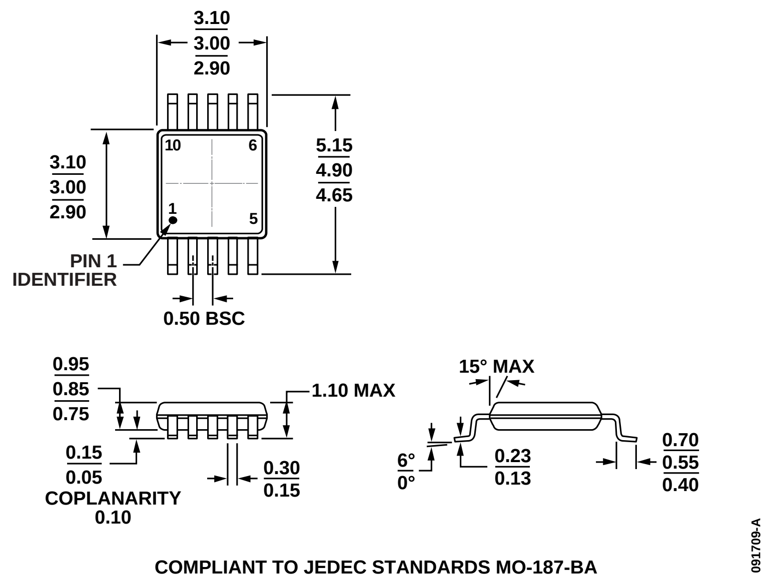

Figure 42. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

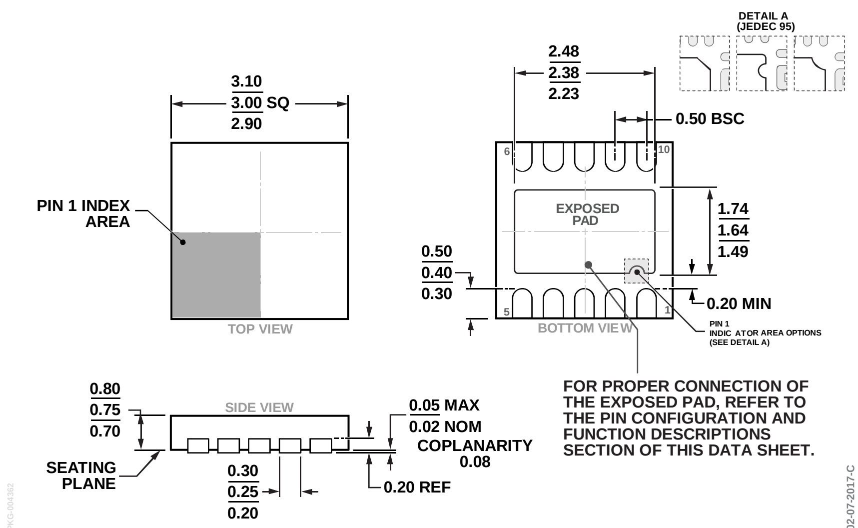

Figure 43. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 Package Height]
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM3065EARZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM3065EARZ-R7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM3065EBRZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM3065EBRZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM3065EARMZ	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8
ADM3065EARMZ-R7	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8
ADM3065EBRMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8
ADM3065EBRMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8
ADM3066EACPZ	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-9
ADM3066EACPZ-R7	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-9
ADM3066EBCPZ	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-9
ADM3066EBCPZ-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-9
ADM3066EARMZ	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10
ADM3066EARMZ-R7	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10
ADM3066EBRMZ	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10
ADM3066EBRMZ-R7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10
EVAL-ADM3065EEBZ		8-Lead SOIC Evaluation Board	
EVAL-ADM3065EEB1Z		8-Lead MSOP Evaluation Board	
EVAL-ADM3066EEBZ		10-Lead MSOP Evaluation Board	
EVAL-ADM3066EEB1Z		10-Lead LFCSP Evaluation Board	

[1] Z = RoHS Compliant Part.

D14666-0-5/17(A)