

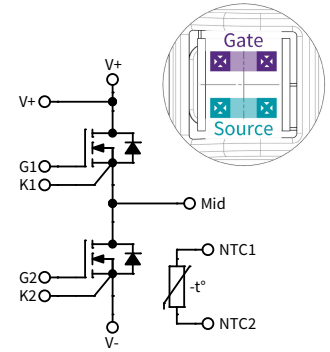
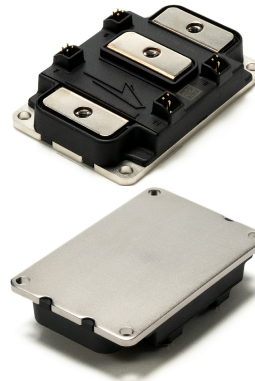
CAB450M12XM3

1200 V, 2.6 mΩ, Silicon Carbide, Half-Bridge Module

V_{DS}	1200 V
I_{DS}	450 A

Technical Features

- High Power Density Footprint
- High Junction Temperature (175 °C) Operation
- Low-Inductance (6.7 nH) Design
- Implements Conduction-Optimized Third Generation SiC MOSFET Technology
- Silicon Nitride Insulator and Copper Baseplate
- 1200 V Drain-Source Voltage



Typical Applications

- Motor & Motion Control
- Vehicle Fast Chargers
- Uninterruptible Power Supplies
- Smart-Grid / Grid-Tied Distributed Generation
- Traction Drives
- E-mobility

System Benefits

- Terminal layout allows for direct bus bar connection without bends or bushings enabling a simple, low inductance design.
- Isolated, integrated temperature sensing enables high-level temperature protection.
- Dedicated high-side Kelvin-drain pin enables direct voltage sensing for gate driver overcurrent protection.

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Drain-Source Voltage	V_{DS}			1200		$T_c = 25\text{ °C}$	
Maximum Gate-Source Voltage	$V_{GS\ max}$	-8		+19	V	Transient	Note 1 Fig. 33
Operational Gate-Source Voltage	$V_{GS\ op}$		-4/+15			Static	
DC Continuous Drain Current ($T_{vj} \leq 175\text{ °C}$)	I_D			450	A	$V_{GS} = 15\text{ V}, T_c = 25\text{ °C}, T_{vj} \leq 175\text{ °C}$	Notes 2, 3, 4 Fig. 20
			438			$V_{GS} = 15\text{ V}, T_c = 90\text{ °C}, T_{vj} \leq 175\text{ °C}$	
Pulsed Drain Current	I_{DM}		900			t_{pmax} limited by $T_{j\ max}$ $V_{GS} = 15\text{ V}, T_c = 25\text{ °C}$	
Power Dissipation	P_D		1670		W	$T_c = 25\text{ °C}, T_{vj} \leq 175\text{ °C}$	Note 5 Fig. 21
Operational Virtual Junction Temperature	$T_{vj\ op}$	-40		175	°C		

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance

Note (2): Current limit $T_c = 25\text{ °C}$ imposed by package

Note (3): Current Limit $T_c = 90\text{ °C}$ calculated by $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)}(T_{vj(max)}, I_{D(max)}))}$

Note (4): Verified by design

Note (5): $P_D = (T_{vj} - T_c) / R_{TH(jc, typ)}$


MOSFET Characteristics (Per Position) ($T_{VJ} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200			V	$V_{GS} = 0\text{ V}, T_{VJ} = -40\text{ }^{\circ}\text{C}$	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6		$V_{DS} = V_{GS}, I_{DS} = 132\text{ mA}$	
			2.0			$V_{DS} = V_{GS}, I_{DS} = 132\text{ mA}, T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}		5	200	μA	$V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$	
Gate-Source Leakage Current	I_{GSS}		50	1300	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance (MOSFET Only)	$R_{DS(on)}$		2.6	3.4	m Ω	$V_{GS} = 15\text{ V}, I_D = 450\text{ A}$	Fig. 2 Fig. 3
			4.7			$V_{GS} = 15\text{ V}, I_D = 450\text{ A}, T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Transconductance	g_{fs}		348		S	$V_{DS} = 20\text{ V}, I_D = 450\text{ A}$	Fig. 4
			333			$V_{DS} = 20\text{ V}, I_D = 450\text{ A}, T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Turn-On Switching Energy, $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 175\text{ }^{\circ}\text{C}$	E_{On}		25.4 24.0 24.4		mJ	$V_{DD} = 600\text{ V},$ $I_D = 450\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V},$ $R_{G-ON(ext)} = 4.0\text{ }\Omega, R_{G-OFF(ext)} = 0.0\text{ }\Omega,$ $L_{\sigma} = 10.2\text{ nH}$	Fig. 11 Fig. 13
Turn-Off Switching Energy, $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 175\text{ }^{\circ}\text{C}$	E_{Off}		7.51 8.10 8.35				
Internal Gate Resistance	$R_{G(int)}$		2.5		Ω	$f = 100\text{ kHz}$	
Input Capacitance	C_{iss}		38.0		nF	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V},$ $V_{AC} = 25\text{ mV}, f = 100\text{ kHz}$	Fig. 9
Output Capacitance	C_{oss}		1.5				
Reverse Transfer Capacitance	C_{rss}		35		pF		
Gate to Source Charge	Q_{GS}		385		nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V},$ $I_D = 450\text{ A},$ Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		475				
Total Gate Charge	Q_G		1300				
FET Thermal Resistance, Junction to Case	R_{thJC}		0.094		$^{\circ}\text{C}/\text{W}$		Fig. 17

Diode Characteristics (Per Position) ($T_{VJ} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Body Diode Forward Voltage	V_{SD}		4.7		V	$V_{GS} = -4\text{ V}, I_{SD} = 450\text{ A}$	Fig. 7
			4.2			$V_{GS} = -4\text{ V}, I_{SD} = 450\text{ A}, T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Reverse Recovery Time	t_{RR}		78		ns	$V_{GS} = -4\text{ V}, I_{SD} = 450\text{ A}, V_R = 600\text{ V},$ $di/dt = 5.1\text{ A/ns}, R_{G-ON(ext)} = 4.0\text{ }\Omega,$ $T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Reverse Recovery Charge	Q_{RR}		7.2		μC		
Peak Reverse Recovery Current	I_{RRM}		169		A		
Reverse Recovery Energy, $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 175\text{ }^{\circ}\text{C}$	E_{RR}		0.2 0.9 1.1		mJ	$V_{DD} = 600\text{ V}, I_D = 450\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V}, R_{G-ON(ext)} = 4.0\text{ }\Omega,$ $L_{\sigma} = 10.2\text{ nH}$	Fig. 14



Temperature Sensor (NTC) Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resistance at 25°C	R ₂₅		4700		Ω	T _{NTC} = 25 °C
Tolerance of R ₂₅				±1	%	
Beta Value for 25 °C to 85 °C	B _{25/85}		3435		K	
Beta Value for 0 °C to 100 °C	B _{0/100}		3399		K	
Tolerance of B _{25/85}				±1	%	
Maximum Power Dissipation	P ₂₅			50	mW	

Steinhart & Hart Coefficients for NTC Resistance & NTC Temperature Computation (T in K)

$$\ln\left(\frac{R}{R_{25}}\right) = A + \frac{B}{T} + \frac{C}{T^2} + \frac{D}{T^3}$$

A	B	C	D
-1.289E+01	4.245E+03	-8.749E+04	-9.588E+06

$$\frac{1}{T} = A_1 + B_1 \ln\left(\frac{R}{R_{25}}\right) + C_1 \ln^2\left(\frac{R}{R_{25}}\right) + D_1 \ln^3\left(\frac{R}{R_{25}}\right)$$

A ₁	B ₁	C ₁	D ₁
3.354E-03	3.001E-04	5.085E-06	2.188E-07

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Package Resistance, M1 (High-Side)	R ₃₋₁		0.72		mΩ	T _c = 125 °C, Note 6 & 7
Package Resistance, M2 (Low-Side)	R ₁₋₂		0.63			T _c = 125 °C, Note 6 & 7
Stray Inductance	L _{Stray}		6.7		nH	Between terminals 2 & 3, f = 10 MHz
Case Temperature	T _c	-40		125	°C	
Mounting Torque	M _s	2.0	3.0	4.0	N-m	Baseplate, M4 bolts
		2.0	4.0	5.0		Power Terminals, M5 bolts
Weight	W		175		g	
Case Isolation Voltage	V _{isol}	4.0			kV	AC, 50 Hz, 1 minute
Comparative Tracking Index	CTI	600				
Clearance Distance		12.5			mm	From 2 to 3, Note 7
		11.5				From 1 to Baseplate, Note 7
		5.7				From 2 to 5, Note 7
		13.7				From 5 to Baseplate, Note 7
Creepage Distance		14.7				From 2 to 3, Note 7
		14.0				From 1 to Baseplate, Note 7
		14.7				From 2 to 5, Note 7
		14.3				From 5 to Baseplate, Note 7

Note (6): Total Effective Resistance (Per Switch Position) = MOSFET R_{DS(ON)} + Switch Position Package Resistance
Note (7): Numbers reference the connections from the Schematics and Pin Out section of this document

Typical Performance

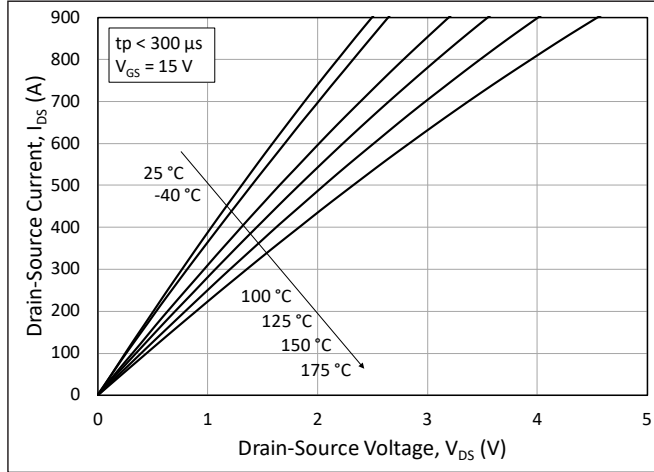


Figure 1. Output Characteristics for Various Junction Temperatures

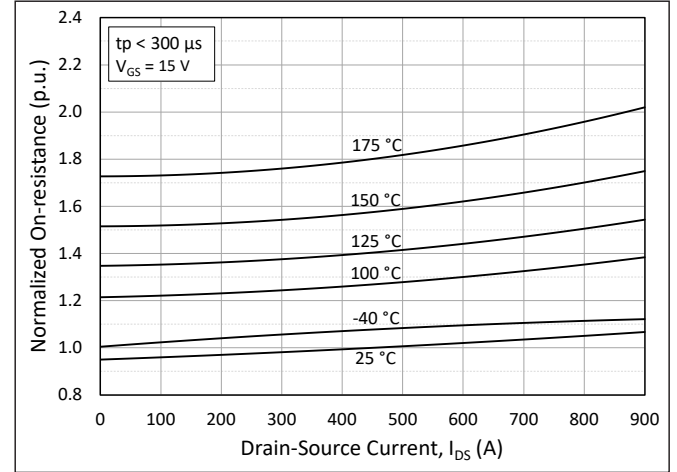


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

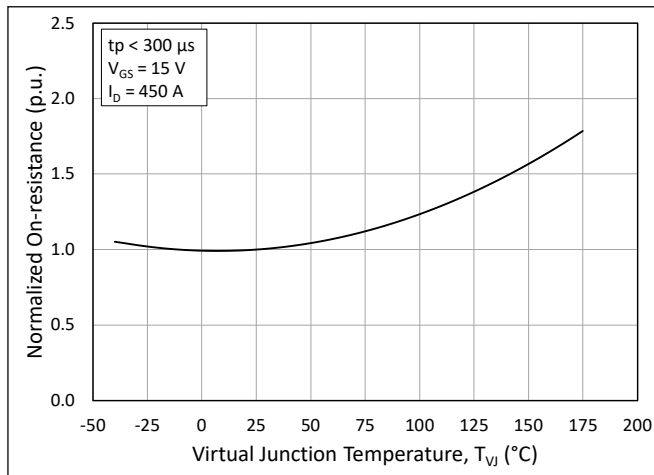


Figure 3. Normalized On-State Resistance vs. Junction Temperature

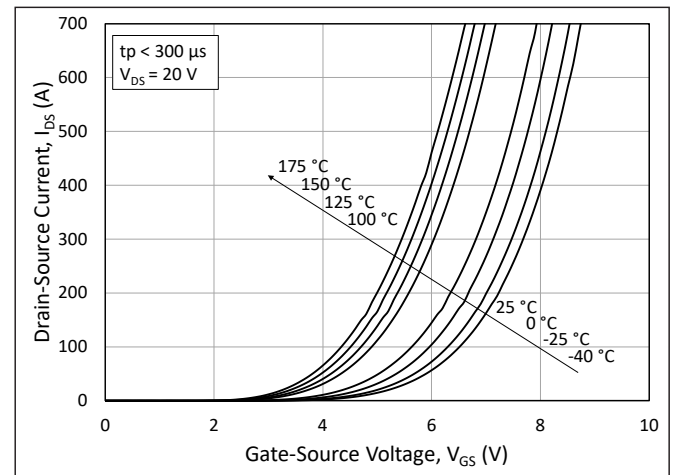


Figure 4. Transfer Characteristic for Various Junction Temperatures

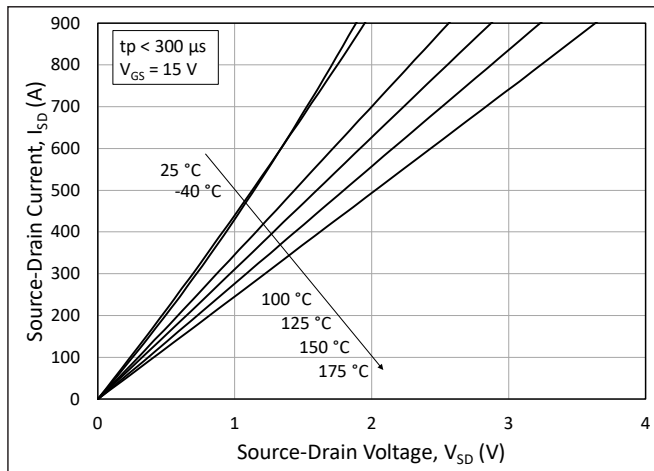


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 15\text{ V}$

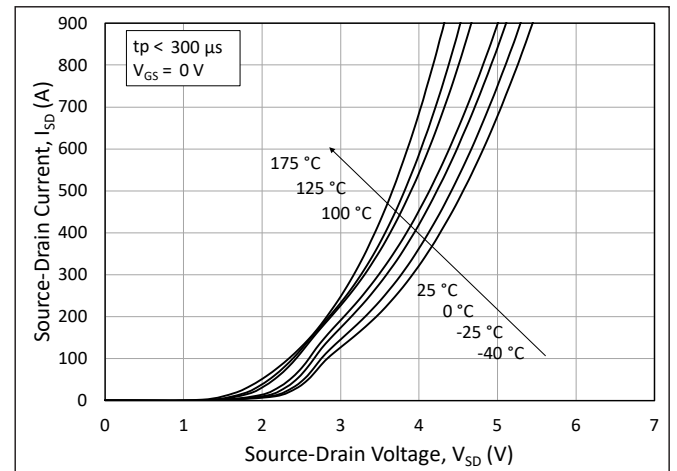


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 0\text{ V}$

Typical Performance

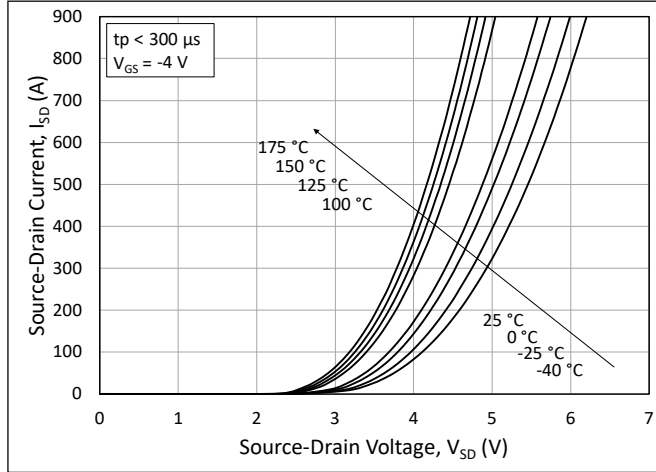


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = -4$ V (Body Diode)

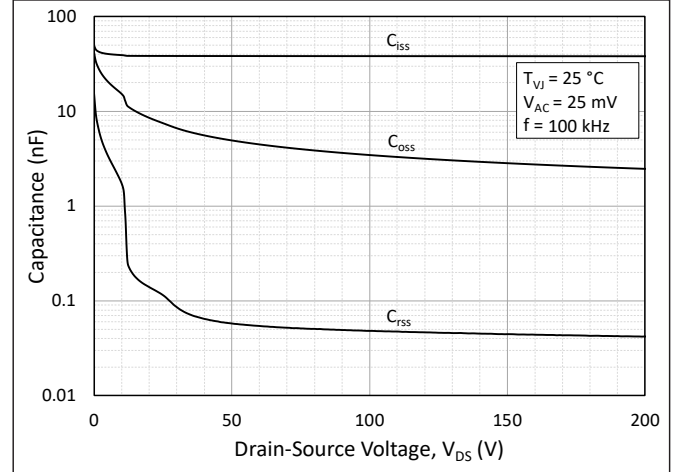


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200 V)

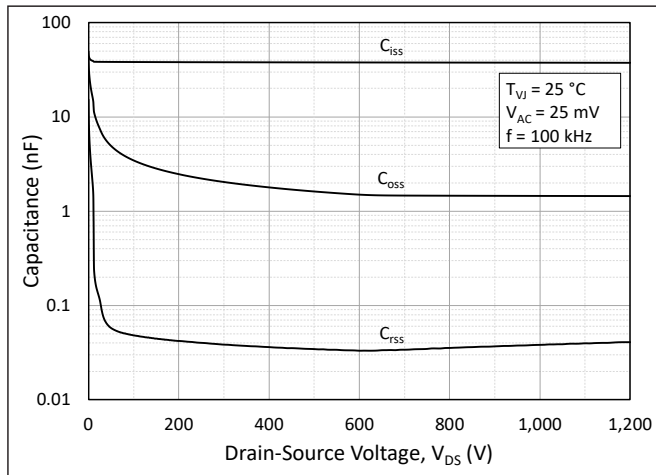


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200 V)

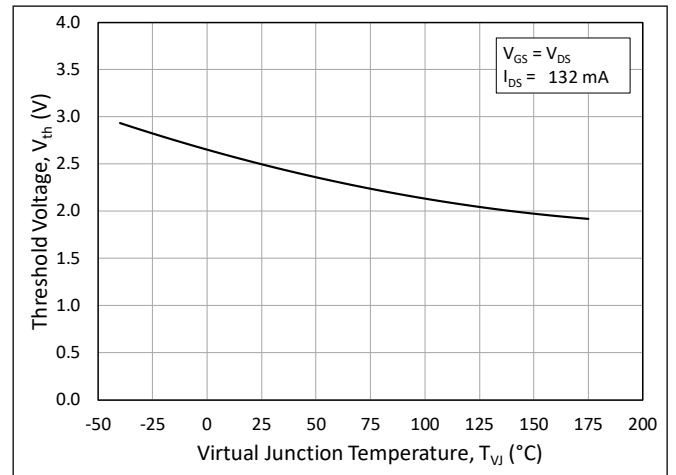


Figure 10. Threshold Voltage vs. Junction Temperature

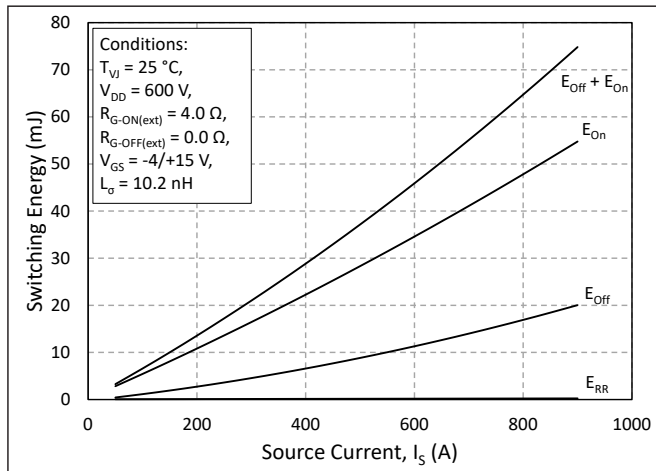


Figure 11. Switching Energy vs. Drain Current ($V_{DD} = 600$ V)

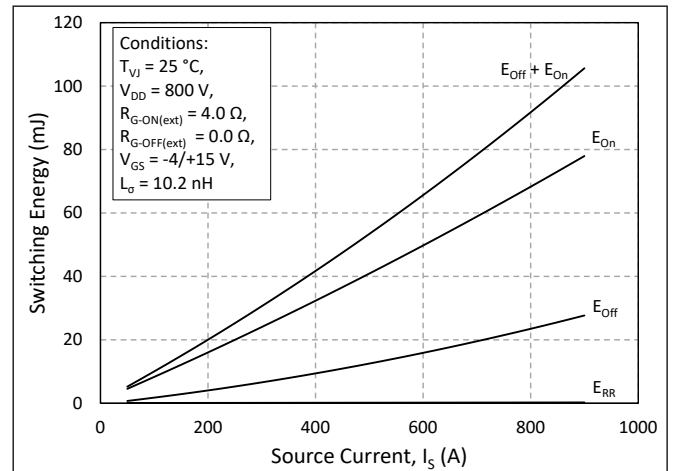


Figure 12. Switching Energy vs. Drain Current ($V_{DD} = 800$ V)

Typical Performance

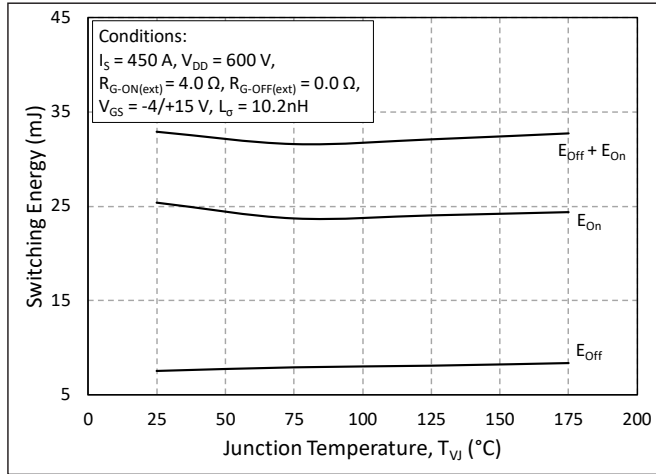


Figure 13. MOSFET Switching Energy vs. Junction Temperature

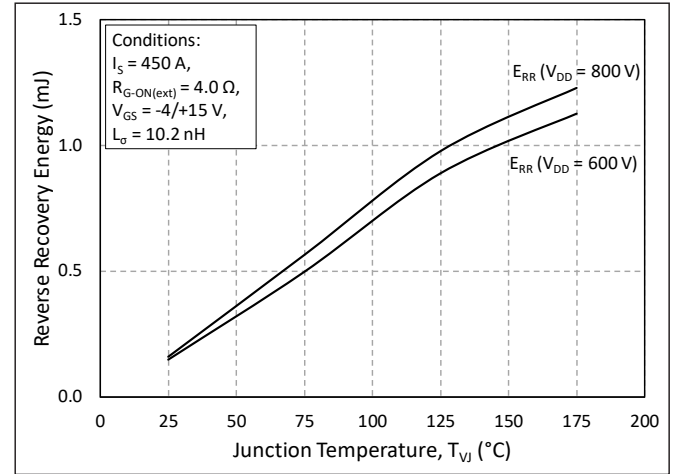


Figure 14. Reverse Recovery Energy vs. Junction Temperature

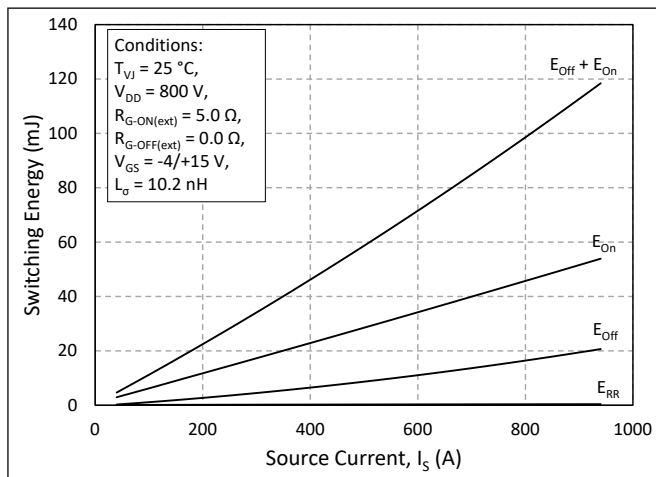


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

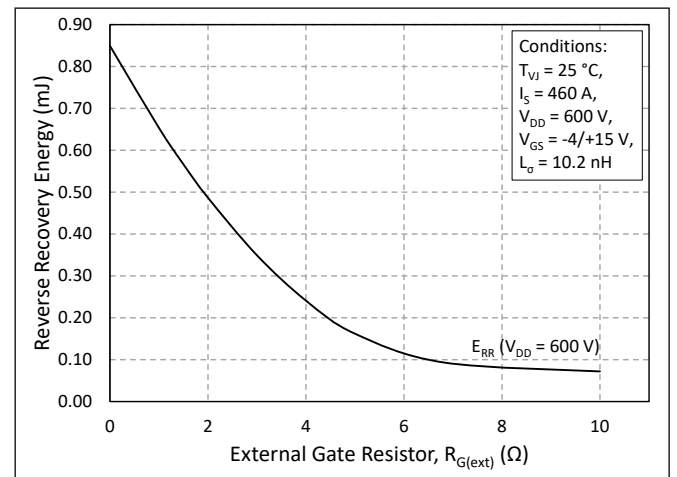


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

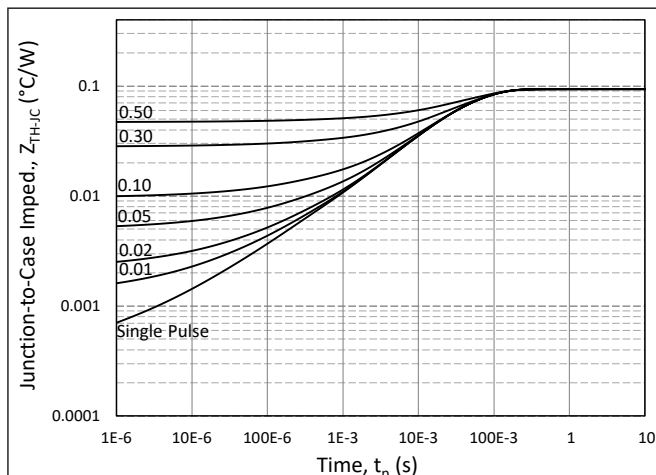


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, Z_{thJC} ($^\circ\text{C/W}$)

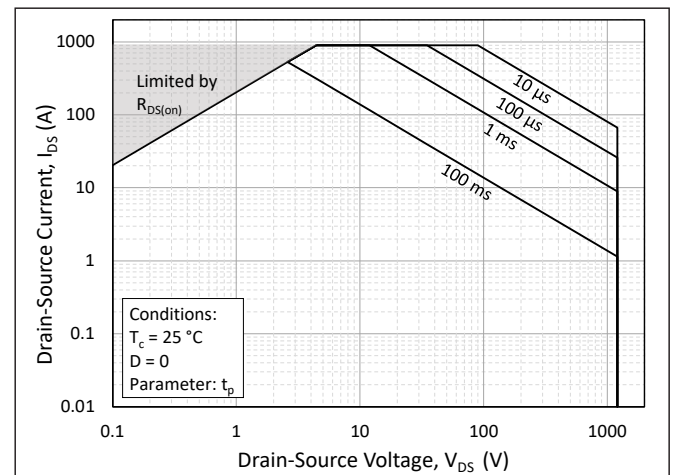


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

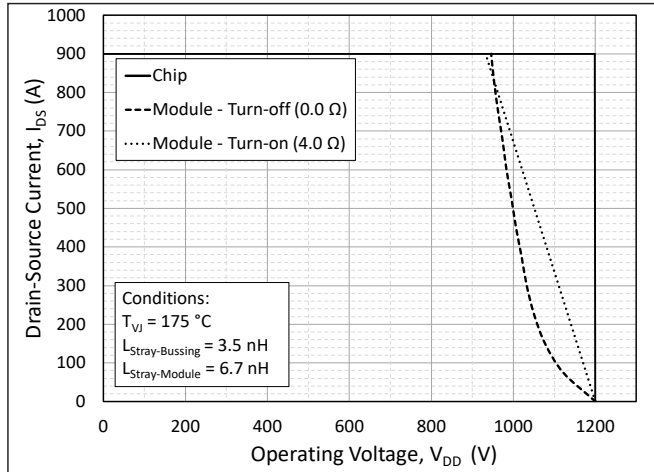


Figure 19. Switching Safe Operating Area

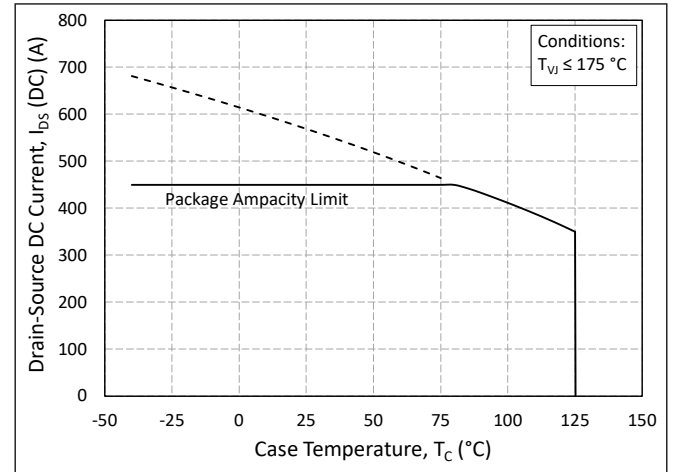


Figure 20. Continuous Drain Current Derating vs. Case Temperature

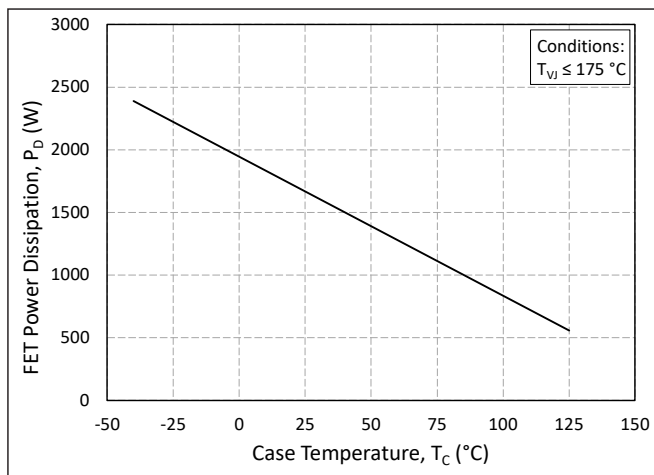


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

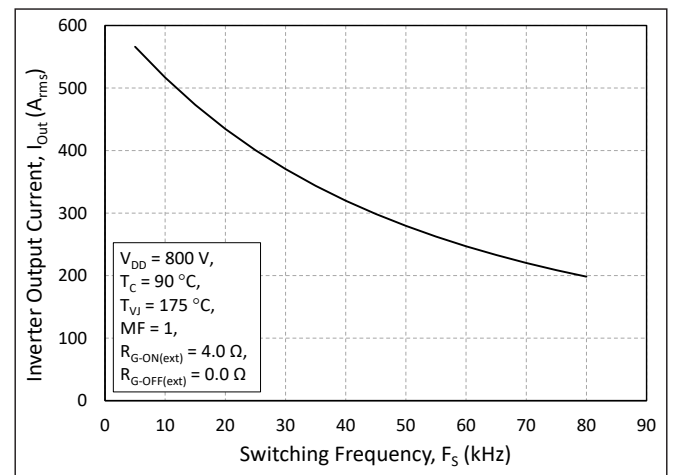


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

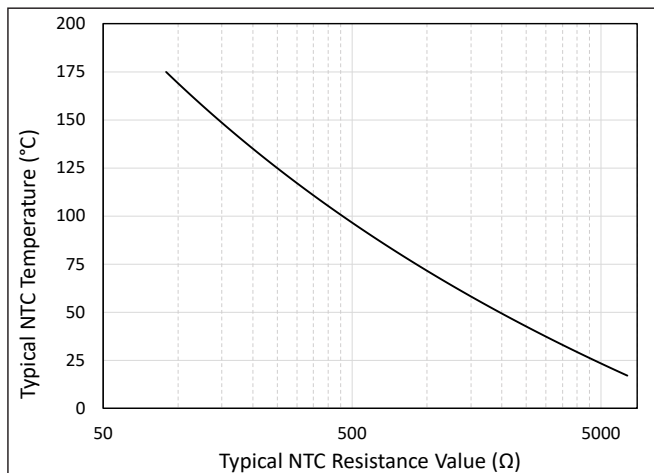


Figure 23. NTC Resistance vs. NTC Temperature

Timing Characteristics

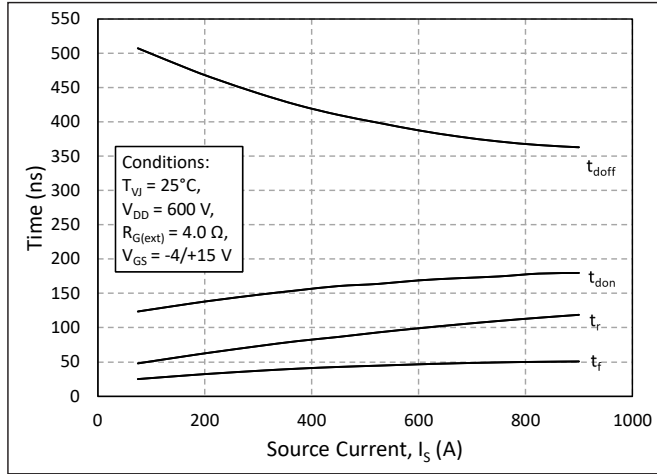


Figure 24. Timing vs. Source Current

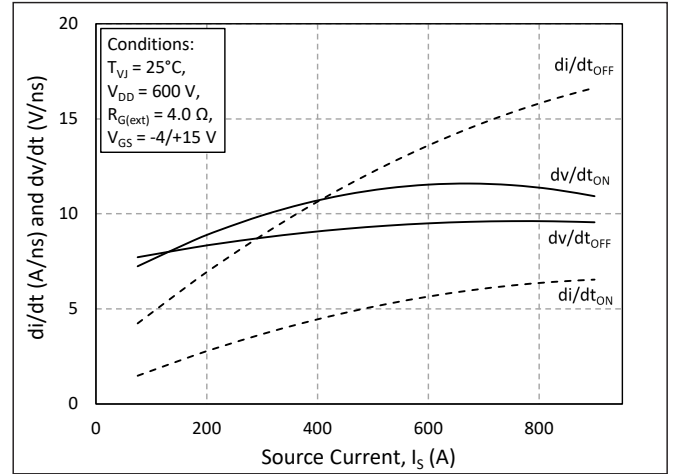


Figure 25. dv/dt and di/dt vs. Source Current

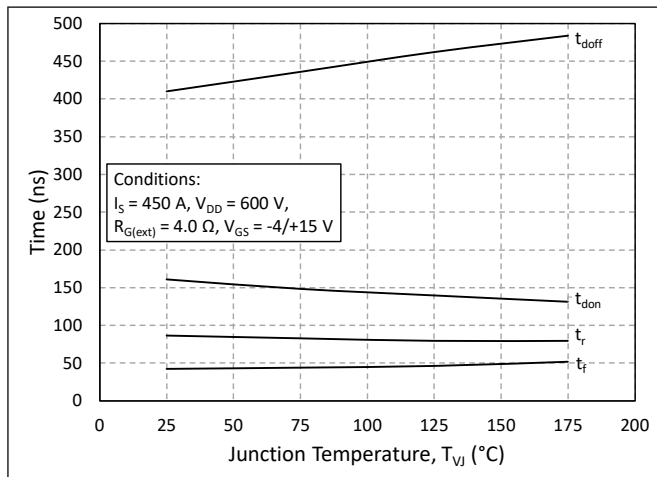


Figure 26. Timing vs. Junction Temperature

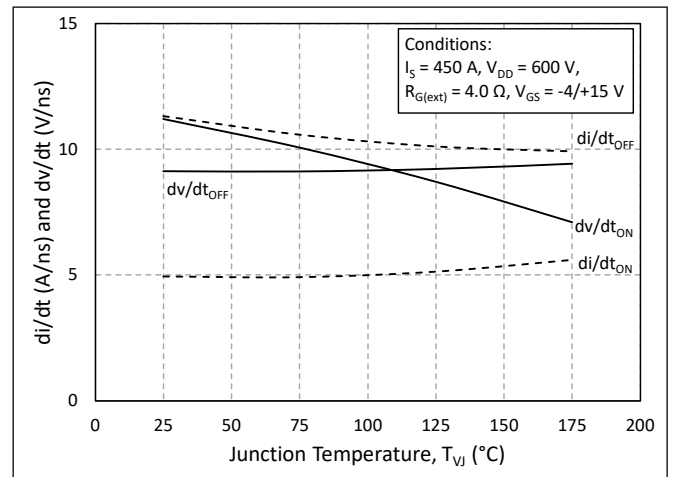


Figure 27. dv/dt and di/dt vs. Junction Temperature

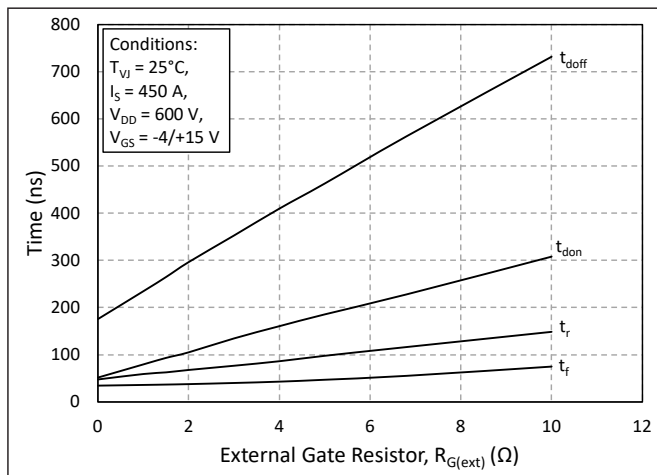


Figure 28. Timing vs. External Gate Resistance

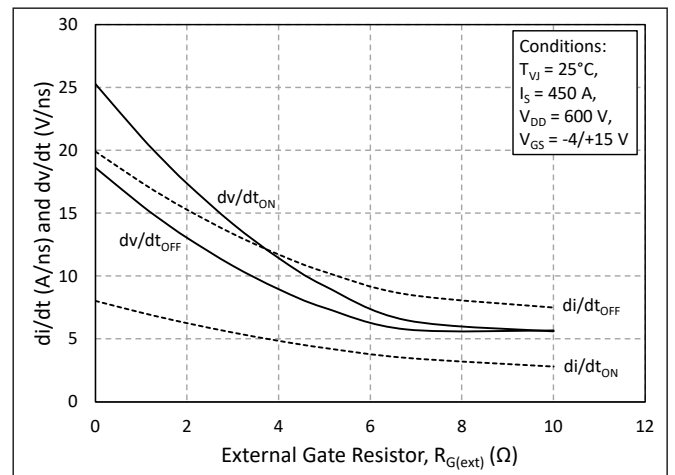


Figure 29. dv/dt and di/dt vs. External Gate Resistance

Definitions

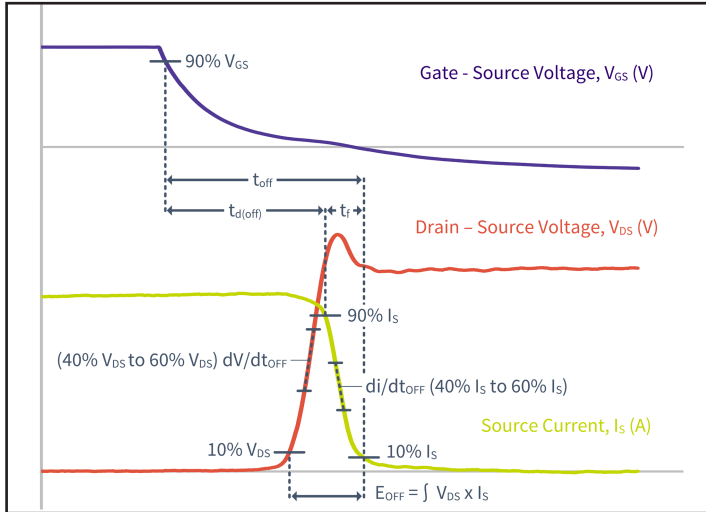


Figure 30. Turn-off Transient Definitions

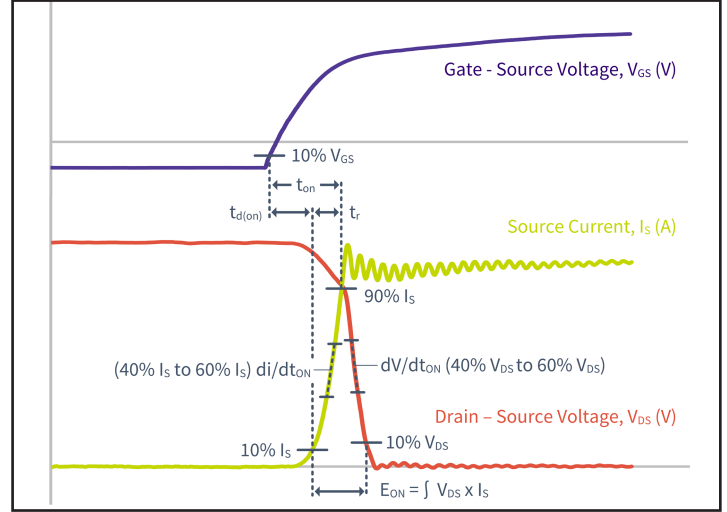


Figure 31. Turn-on Transient Definitions

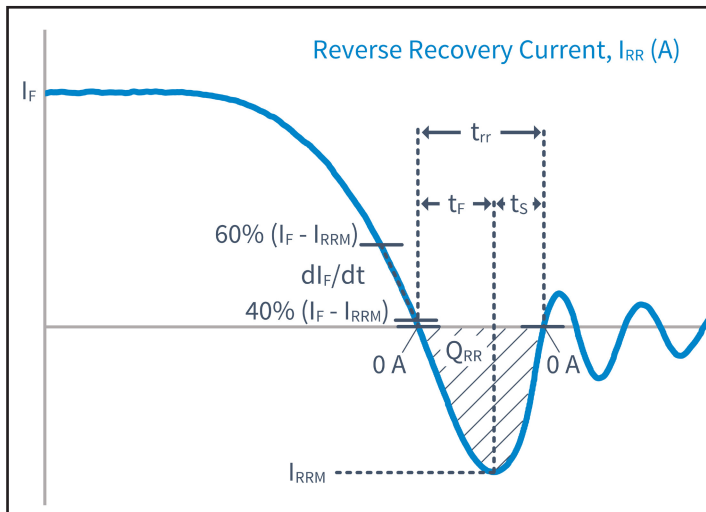


Figure 32. Reverse Recovery Definitions

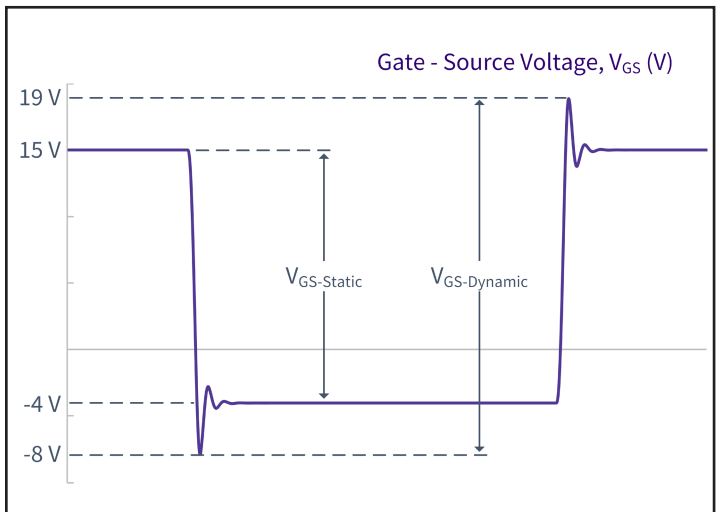
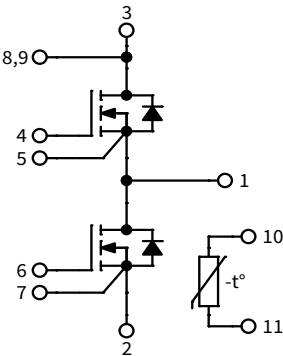
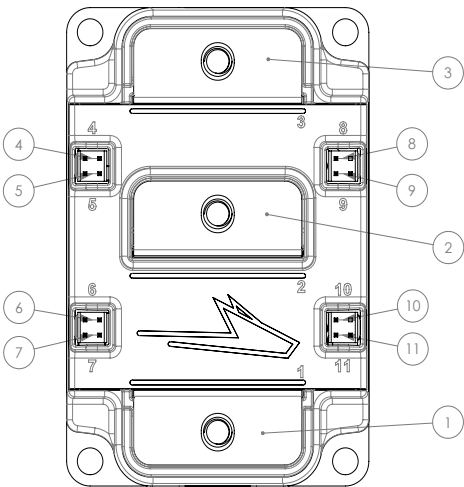
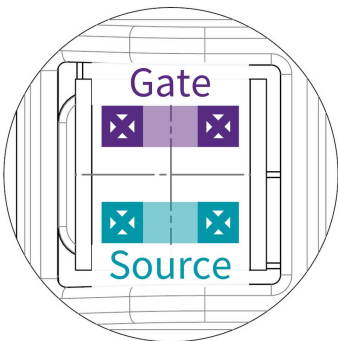


Figure 33. V_{GS} Transient Definitions

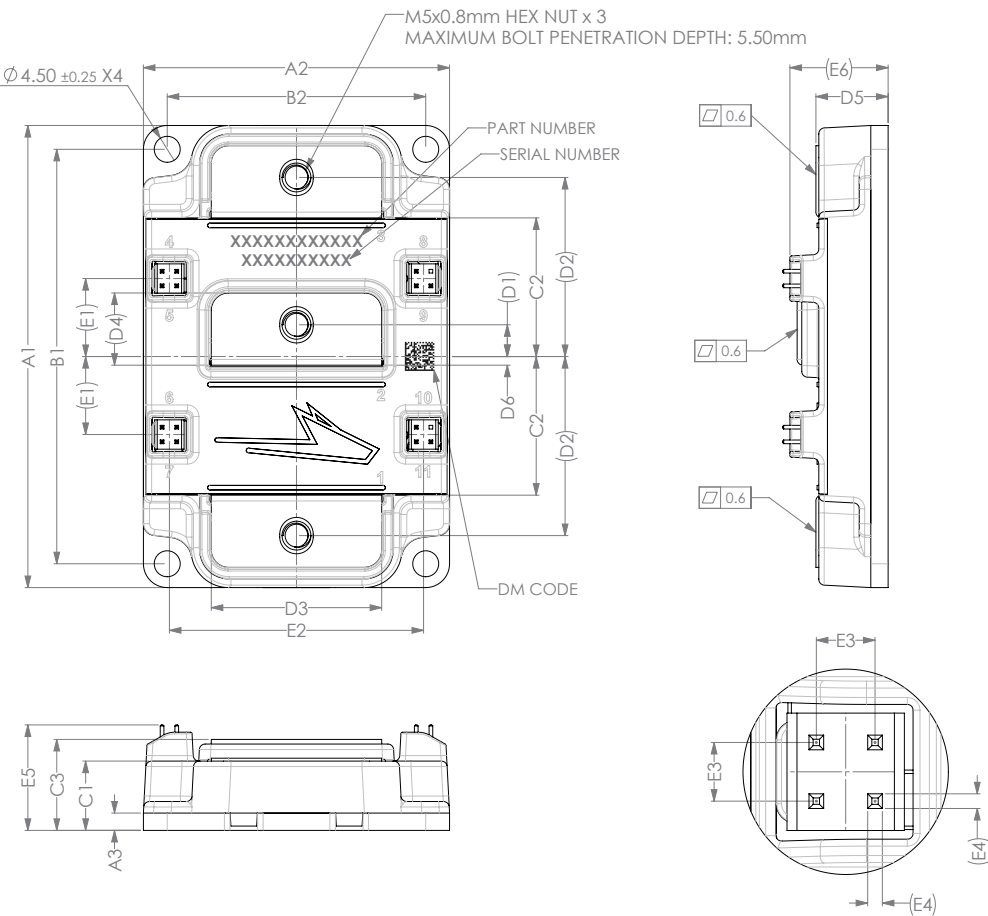
Schematic and Pinout



Zoom View of Signal Pinout



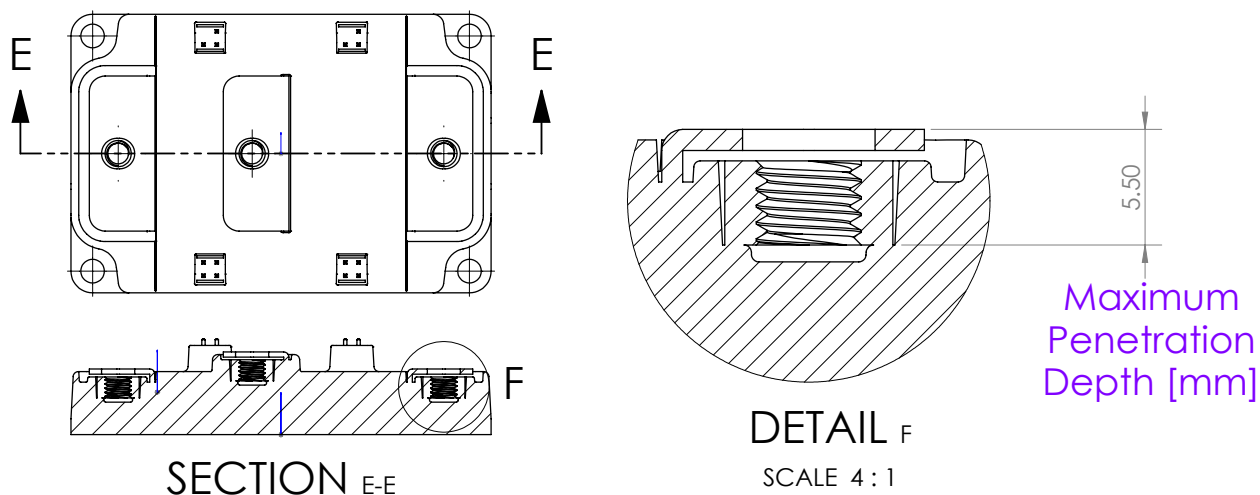
Package Dimension (mm)



DIMENSION TABLE		
SYMBOL	DIMENSION (mm)	TOLERANCE (mm)
A1	80.00	±0.30
A2	53.00	±0.30
A3	3.00	±0.30
B1	71.75	±0.30
B2	44.75	±0.30
C1	12.00	±0.50
C2	24.00	±0.50
C3	15.75	±0.40
D1	(5.50)	REF.
D2	(31.00)	REF.
D3	29.50	±0.30
D4	(12.50) TYP	REF.
D5	12.50	±0.30
D6	1.50	±0.30
E1	(13.50)	REF.
E2	44.00	±0.30
E3	2.54	±0.50
E4	(0.64)	REF.
E5	18.26	±0.30
E6	(17.00)	REF.



Package Dimensions (mm)



Supporting Links & Tools

Evaluation Tools & Support

- [All SiC Module PLECS Models](#)
- [All SiC Module LTspice Models](#)
- [KIT-CRD-CIL12N-XM3: Dynamic Performance Evaluation Board for the XM3 Module](#)
- [SpeedFit 2.0 Design Simulator™](#)
- [Technical Support Forum](#)

Dual-Channel Gate Driver Board

- [CGD12HBXMP: XM3 Evaluation Gate Driver](#)
- [CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers](#)
- [FRDMGD3160XM3EVM: GD3160 XM3 Half-Bridge Evaluation Kit](#)
- [UCC5880QEVM-057 Evaluating Gate Driver for Wolfspeed XM3 Modules](#)
- [UCC5880INVERTEREVM Evaluating Board for Wolfspeed XM3 Modules](#)
- [Si828x Gate Driver Boards for Wolfspeed XM3 Modules](#)

Application Notes

- [XM Module Signal Pinout Clarification Guide](#)
- [XM Mounting Guide](#)
- [XM3 Thermal Interface Material Guide](#)
- [Thermal Characterization Methods and Applications](#)
- [PRD-06832: Design Options for Wolfspeed® Silicon Carbide MOSFET Gate Bias Power Supplies](#)



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Contact info:

4600 Silicon Drive
Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfsped.com/power