RP2350

PCN 28 – A4 stepping

Colophon

Release	2
Build date	29/07/2025
Build version	4e2074f7acf9-dirty

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Document version history

Release	Date	Description
1	1 Jun 2025	Initial release
2	29 Jul 2025	Update to errata section

Product Change Notification

Notification ID

28

Notification date

1 June 2025

Title

Update of RP2350 silicon to A4 stepping.

Products Affected

RP2350A, RP2350B.

Reason for Change

Mass production variant of RP2350A/B moving to A4 stepping including fixes for various errata.

Stepping history

A0

Internal development

A1

Internal development

A2

Early production

A3

Internal development, fixes for various errata, limited production

A4

Some small user-invisible changes to the boot ROM for further security hardening

Change Description

Please refer to the RP2350 datasheet (Appendix C), available on the Raspberry Pi website, for full descriptions of these errata.

The following errata are fixed/mitigated.

Errata	Status	Step	Notes
3	Fixed	A3	In the QFN-60 package, `GPIO_NSMASK` controls the wrong PADS registers.
9	Fixed	A3	Increased leakage current on Bank 0 GPIO when pad input is enabled.
10	Fixed	A3	UF2 drag-and-drop doesn't work with partition tables.

Errata	Status	Step	Notes
12	Mitigated	A3	Inadequate synchronisation of USB status signals.
13	Fixed	A3	A binary containing an explicitly invalid IMAGE_DEF followed by a valid IMAGE_DEF (in that order) fails to boot.
14	Fixed	A3	The bootrom `connect_internal_flash()` function always uses pin 0, ignoring any configured FLASH_DEVINFO CS1 chip select n.
15	Fixed	A3	The `bootrom otp_access()` function applies incorrect access permission to pages 62 and 63.
16	Mitigated	A3	`USB_OTP_VDD` disruption can cause corrupt OTP row read data.
18	Fixed	A4	The RP2350 forever fails to boot if FLASH_PARTITION_SLOT_SIZE contains an invalid ECC bit pattern.
19	Fixed	A3	RP2350 reboot halts if certain bits are set in `FRCE_OFF` when rebooting.
20	Mitigated	A3	An attacker with physical access to the chip and the ability to physically “glitch” the CPU at precise times, could use unsigned code execution on a secured RP2350 by targeting legitimate non-Secure calls to the `bootrom reboot()` function.
21	Mitigated	A3	An attacker with physical access to the chip, and the ability to physically “glitch” the CPU at precise times, could potentially extract sensitive data from OTP on a RP2350 in BOOTSEL mode.
22	Fixed	A3	Parsing a malformed lollipop block loop causes the system to halt rather than fail.
23	Fixed	A3	`PICOBOOT GET_INFO` command always returns zero for `PACKAGE_SEL` .
24	Mitigated	A4	An attacker with physical access to the chip, moderate hardware, and the ability to physically “glitch” the CPU at precise times, could cause unsigned code execution on a secured RP2350.
25	Fixed	A4	`LOAD_MAP` that uses non-word sizes previously didn’t cause an error. The bootrom now correctly rejects these structures.
26	Mitigated	A3	RCP random delays can create a side-channel. These delays are disabled in the bootrom.

The following features have been updated:

- The reset state of the following clock configuration registers have been updated:
  - `ROSC` : `FREQA.DS0_RANDOM` and `FREQA.DS1_RANDOM` from 0 to 1, enabling randomisation of first two drive stages.
  - `CLOCKS` : `CLK_SYS_CTRL.SRC` from 0 to 1 (select `AUX` source).
  - `CLOCKS` : `CLK_SYS_CTRL.AUXSRC` from 0 to 2 (select `ROSC` as `AUX` source).
- Update the early boot path to change the clk_ref divider from 1 to 5, and the `ROSC` divider from 8 to 2.
  - Together with the register reset state changes, this increases the boot `clk_sys` frequency by a factor of 4, to approximately 48 MHz.
  - These changes reduce boot time and fault injection susceptibility.
  - These changes apply for all boot outcomes, including watchdog and `POWMAN` vector boot.

Mechanical (Form, Fit, Function) Changes

None

Electrical

Errata 9 has been fixed, so any external circuitry used to work around this issue may need to be reviewed.

Software/Firmware Changes Required

Use version 2.1 or newer of the Pico SDK.

Transition Date(s)

Mass production will move to A4 in July 2025 and all other variants are now EOL.

Identification Method to Distinguish Change

The new product can be distinguished by examination of the chip. The part number printed on the top of the device will have the suffix `A4` , as shown in the image below.

Contact Details for more information

Please contact applications@raspberrypi.com if you have any queries about this PCN.

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