RAYSTAR Optronics, Inc.
曜凌光電股份有限公司

曜凌光電股份有限公司
Raystar Optronics, Inc.
T: +886-4-2565-0761 | F: +886-4-2565-0760
salescontact@raystar-optronics.com | www.raystar-optronics.com

RFH700D5-AWW-MNN

SPECIFICATION

CUSTOMER:

APPROVED BY	
PCB VERSION	
DATE	

FOR CUSTOMER USE ONLY

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

Release DATE:

TFT Display Inspection Specification: https://www.raystar-optronics.com/download/products.htm
Precaution in use of TFT module: https://www.raystar-optronics.com/download/declaration.htm

Revision History

VERSION	DATE	REVISED PAGE NO.	Note
0	2025/04/24		First issue

Contents

1.Module Classification Information

R	F	H	70	0D5	-	A	W	W	-	M	N	N
1	2	3	4	5	-	6	7	8	-	9	10	11

Item	Description		
1	R：Raystar Optronics Inc.		
2	Display Type：F→TFT Type, J→ Custom TFT		
3	Solution: A: 128x160 B:320x234 C:320x240 D:480x234 E:480x272 F:800x480 G:640x480 H:1024x600 I:320x480 J:240x320 K:1280x800 L:240x400 M:1024x768 N:128x128 O:480x800 P:640x320 Q:800x600 S:480x128 T:800x320		
4	Display Size：7.0” TFT		
5	Version Code.		
6	Model Type: A：TFT LCD E：TFT+FR+CONTROL BOARD J：TFT+FR+A/D BOARD N：TFT+FR+A/D BOARD+CONTROL BOARD S：TFT+FR+POWER BOARD (DC TO DC) 1：TFT+CONTROL BOARD	6：TFT+FR H：TFT+D/V BOARD I：TFT+FR+D/V BOARD B：TFT+POWER BD	
7	Polarizer Type, Temperature range, View direction	I→Transmissive, W. T, 6:00 ; C→Transmissive, N. T, 6:00 L→Transmissive, W.T,12:00 ; F→Transmissive, N.T,12:00 Y→Transmissive,W.T, IPS TFT ; W→Transmissive, Super W.T, IPS TFT A→Transmissive, N.T, IPS TFT Z→Transmissive, W.T, O-TFT R→Transmissive, Super W.T, O-TFT N→Transmissive, Super W.T, 6:00; Q→Transmissive, Super W.T, 12:00 V→Transmissive, Super W.T, VA TFT	
8	Backlight	W：LED, White	H：LED, High Light White
		F：CCFL, White	
9	Driver Method	D: Digital A: Analog L：LVDS M:MIPI	
10	Interface	N：without control board A：8Bit B：16Bit S:SPI Interface R: RS232 U:USB I: I2C	
11	TS	N：Without TS S：resistive touch panel C：capacitive touch panel capacitive touch panel (G-F-F) G：capacitive touch panel(G-G)	

2.Summary

The specification RF70D5 is a 7.0” a-Si TFT Liquid Crystal Display ODF cell.

The a-Si TFT-LCD cell will applied to a high transmittance operating in the normally black mode a-Si TFT -LCD product.

3.General Specifications

- Size: 7.0 inch
- Dot Matrix: 1024 x RGB x 600(TFT) dots
- Module dimension: 169.9(W) x 103.4(H) x 5.6(D) mm
- Active area: 154.2144 x 85.92 mm
- Pixel pitch: 0.1506x 0.1432 mm
- LCD type: TFT, Normally Black, Transmissive
- View Angle: 80/80/80/80
- TFT Driver IC: JD9165BA or Equivalent
- TFT Interface: 4-Lanes MIPI
- Backlight Type: LED,Normally White
- With /Without TP: Without TP
- Surface: Anti-Glare

*Color tone slight changed by temperature and driving voltage.

4.Interface

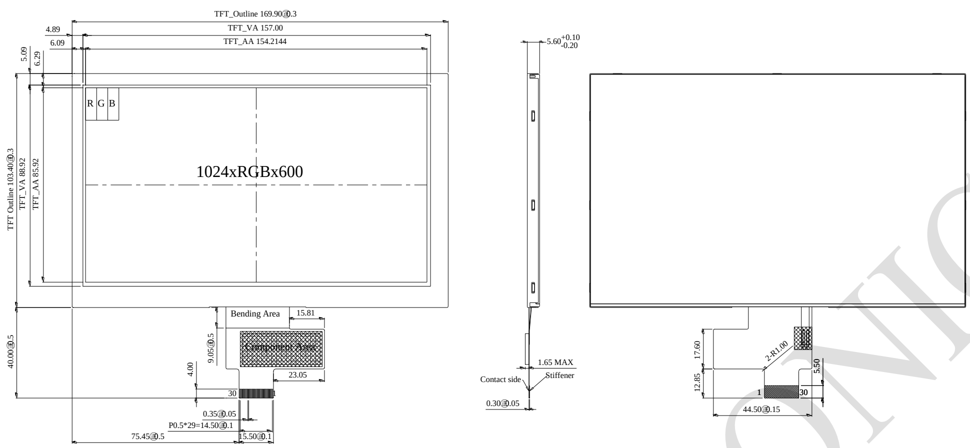
4.1. LCM PIN Definition

Pin No.	Symbol	Function	Remark
1	VLED+	LED Anode	
2	VLED+	LED Anode	
3	VGH	Positive power for TFT	
4	VGL	Negative power for TFT	
5	UPDN	Horizontal inversion	
6	SHLR	Vertical inversion	
7	VLED-	LED Cathode	
8	VLED-	LED Cathode	
9	AVDD	Power for Analog Circuit	
10	GND	Ground	
11	D3P	MIPI data input.	
12	D3N	MIPI data input.	
13	GND	Ground	
14	D2P	MIPI data input.	
15	D2N	MIPI data input.	
16	GND	Ground	
17	CLKP	MIPI clock input	
18	CLKN	MIPI clock input	
19	GND	Ground	
20	D1P	MIPI data input.	
21	D1N	MIPI data input.	
22	GND	Ground	
23	D0P	MIPI data input.	
24	D0N	MIPI data input.	
25	GND	Ground	
26	NC	No connection	
27	RESET	Global reset pin. Active Low to enter Reset State. Normally	

		pull high. Connecting with an RC reset circuit for stability.	
28	VDD(1.8V)	Digital circuit	
29	VDD(1.8V)	Digital circuit	
30	VCOMIN	Common voltage	

Note
When SHLR =”1”,set right to left scan direction.
When SHLR =”0”,set left to right scan direction.
When UPDN =”0”,set top to bottom scan direction.
When UPDN =”1”,set bottom to top scan direction

5.Contour Drawing



PIN NO.	SYMBOL
1	VLED+
2	VLED+
3	VGH
4	VGL
5	UPDN
6	SHLR
7	VLED-
8	VLED-
9	AVDD
10	GND
11	D3P
12	D3N
13	GND
14	D2P
15	D2N
16	GND
17	CLKP
18	CLKN
19	GND
20	D1P
21	D1N
22	GND
23	D0P
24	D0N
25	GND
26	NC
27	RESET
28	VDD (1.8V)
29	VDD (1.8V)
30	VCOMIN

VDD:1.8V
RESET: H:1.8V L:0V
STBYB:H:1.8V L:0V
SHLR:H:1.8V L:0V
UPDN:H:1.8V L:0V

The non-specified tolerance of dimension is ±0.3mm.

6.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-30	—	+85	℃
Storage Temperature	TST	-40	—	+90	℃

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. ≦60℃, 90% RH MAX. Temp. > 60℃, Absolute humidity shall be less than 90% RH at 60℃

7.Electrical Characteristics

7.1. Operating conditions:

Typical Operation Conditions

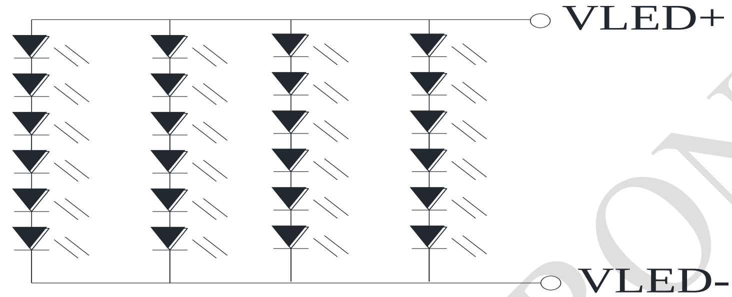
Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	VDD	1.71	1.8	1.89	V	
Analog Power	AVDD	-	11	-	V	
TFT Gate ON Voltage	VGH	19.5	20	20	V	Note1
TFT Gate OFF Voltage	VGL	-8.5	-8	-7.5	V	Note2
TFT Common Voltage	VCOMIN	-	4.9	-	V	Note3
Power Current	IDD	-	14	22	mA	VDD=1.8V
Analog Power Current	I_{AVDD}	-	18.5	-	mA	AVDD=11V
TFT Gate ON Current	I_{VGH}	-	1.5	-	mA	VGH=20V
TFT Gate OFF Current	I_{VGL}	-	1.5	-	mA	VGL=-8V
TFT Common Current	I_{VCOMIN}	-	1	-	uA	VCOM=4.9V

Note 1. VGH is TFT Gate operating Voltage.
Note 2. VGL is TFT Gate operating Voltage.
The storage structure of this model is CST (Storage on Common)
Note 3. Vcom must be adjusted to optimize display quality Crosstalk, Contrast Ratio and etc.

7.2. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	—	—	200	—	mA	-
LED voltage	VLED+	16.2	19.2	21.0	V	Note 1
LED Life Time	—	50,000	—	—	Hr	Note 2,3,4

Note 1 : There are 1 Groups LED



B/L CIRCUIT DIAGRAM

Note 2 : Ta = 25 ℃
Note 3 : Brightness to be decreased to 50% of the initial value
Note 4 : The single LED lamp case

8.MIPI Interface

8.1. DSI Format

Information is transferred between host processor and peripheral using one or more serial data signals and accompanying serial clock. The action of sending high-speed serial data across the bus is called a HS transmission or burst. Between transmissions, the differential data signal or Lane goes to a low-power state (LPS). Interfaces should be in LPS when they are not actively transmitting or receiving high-speed data. Figure 1 shows the basic structure of a HS transmission. N is the total number of bytes sent in the transmission.

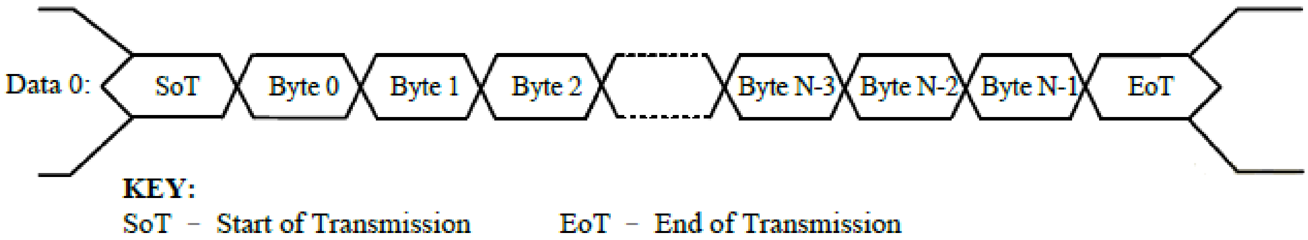


Figure 1: Basic HS Transmission Structure

Multi Lane Distribution and Merging

DSI is a Lane-scalable interface. Applications requiring more bandwidth than that provided by one Data Lane may expand the data path to two, three, or four Lanes wide and obtain approximately linear increases in peak bus bandwidth.
Multi-Lane implementations shall use a single common clock signal, shared by all Data Lanes. Conceptually, between the PHY and higher functional blocks is a layer that enables multi-Lane operation.
Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of Lanes, some Lanes may run out of data before others. Therefore, the Lane Management layer, as it buffers up the final set of less-than-N bytes, de-asserts its “valid data” signal into all Lanes for which there is no further data.
Although all Lanes start simultaneously with parallel Sots, each Lane operates independently and may complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier.
The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane Management layer. The Lane Management layer reconstructs the original sequence of bytes in the transmission. Figure 8.4 & 8.5 illustrate a variety of ways a HS transmission can terminate for different number of Lanes and packet lengths.

Number of Bytes, N transmitted is an integer multiple of the number of lanes

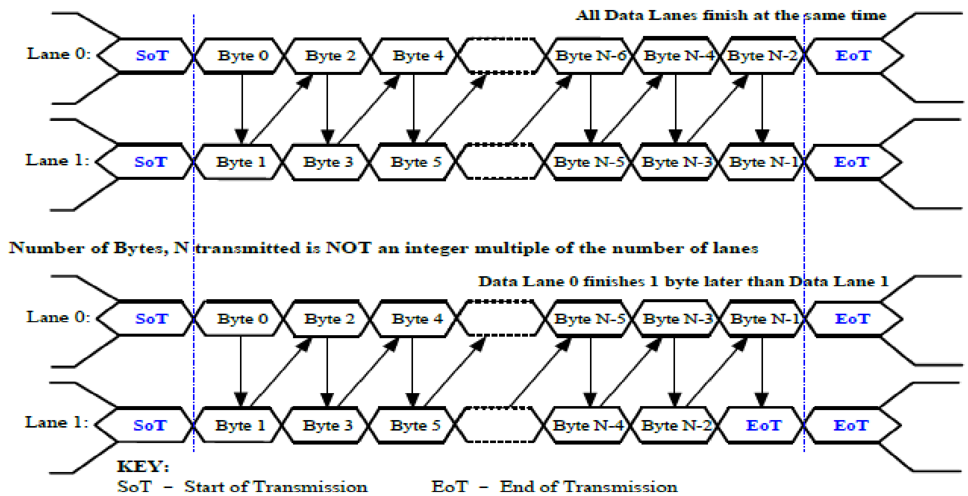


Figure 2: Two Lane HS Transmission Example

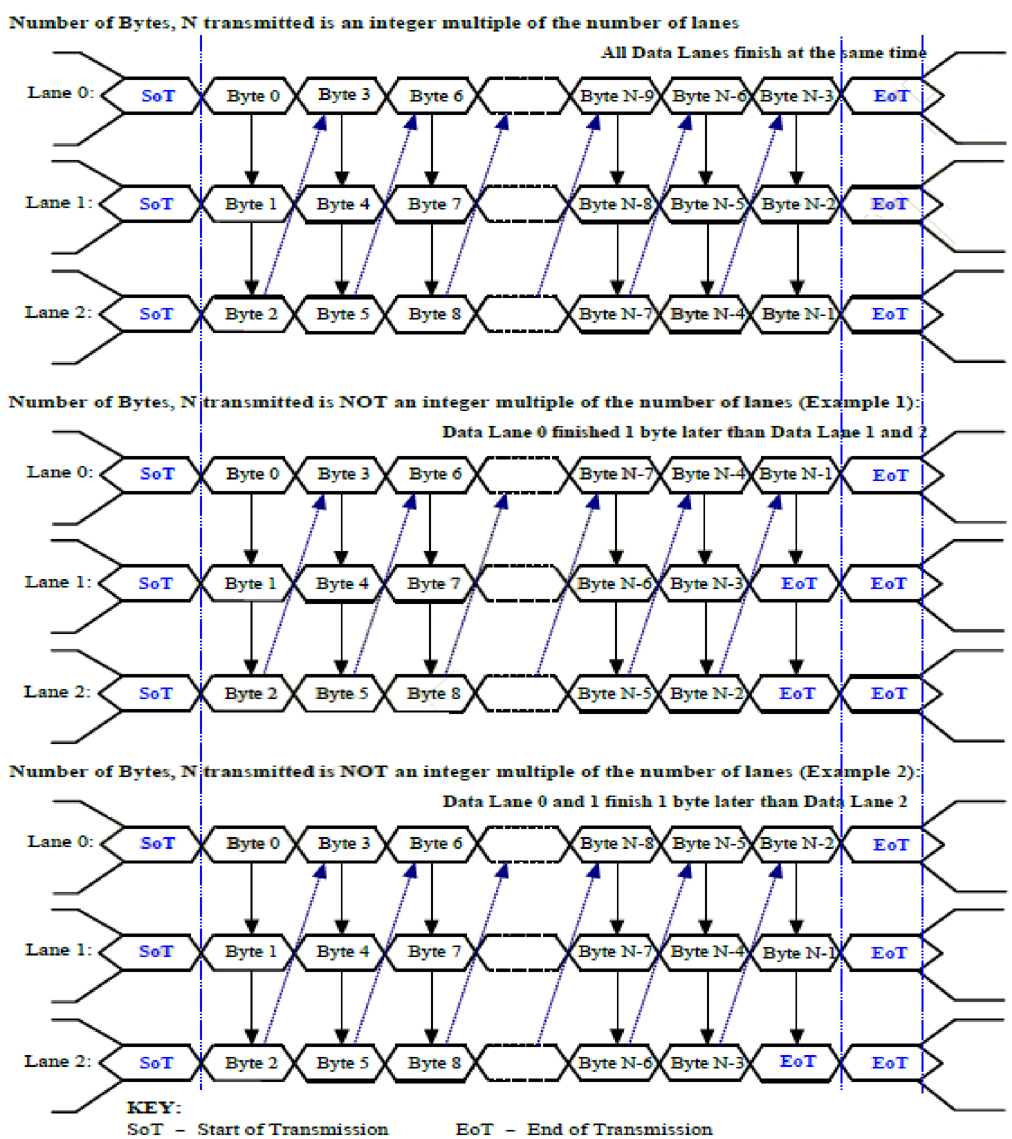


Figure 3: Three Lane HS Transmission Example

8.2. Video Mode Interface Timing

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

1 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

•**Non-Burst Mode with Sync Pulse –** enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

•**Non-Burst Mode with Sync Events –** similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.

•**Burst Mode –** RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral.

To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. The host processor should return to LP state once per scanline during the horizontal blanking time.

During the BLLP the DSI Link may do any of the following:

• Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX

• Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode

• Transmit one or more non-video packets from the host processor to the peripheral using HS Mode

• If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode

• Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VSS; all other lines shall start with VSE or HSS. Note that the position of synchronization packets, such as VSS and HSS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet.

Transmission packet components used in the figures in this section are defined in Figure 4 unless otherwise specified.

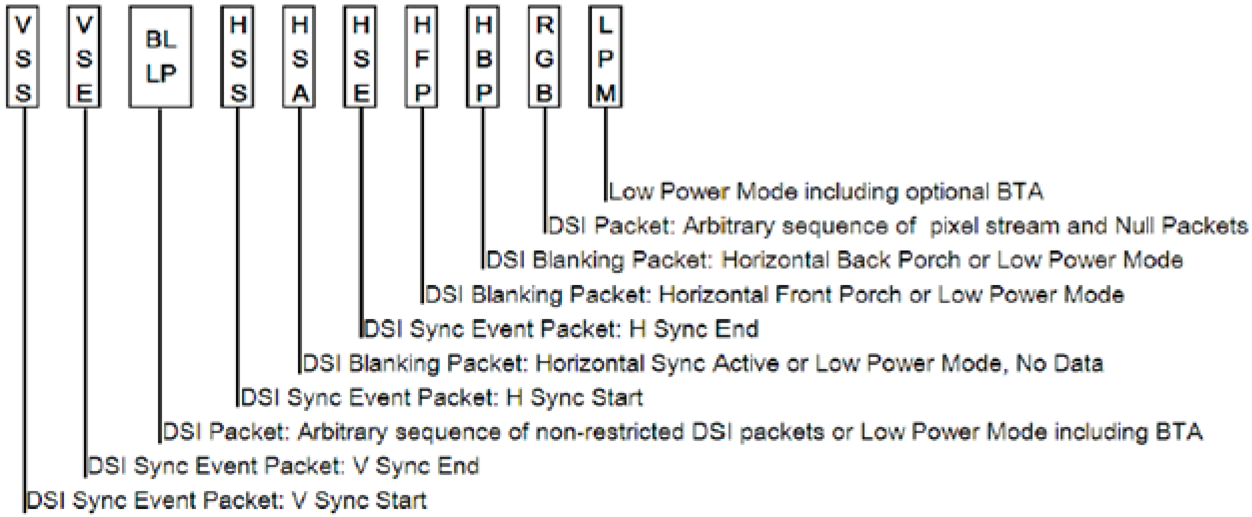


Figure 4: Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

2. Non-Burst sync pulse mode

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and width of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure 5

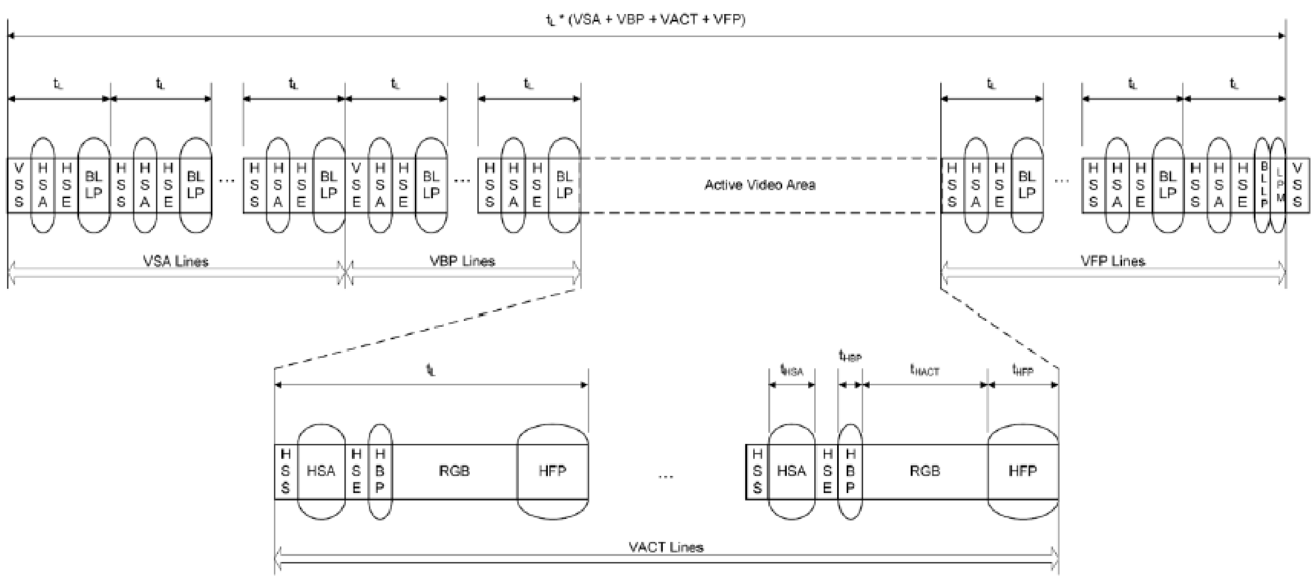


Figure 5: Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HAS (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power. During HAS, HBP and HFP periods, the bus should stay in the LP-11 state.

3. Non-Burst sync event mode

This mode is a simplification of the "Non-Burst Mode with Sync Pulses" format. Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. An example of this mode is shown in Figure 6.

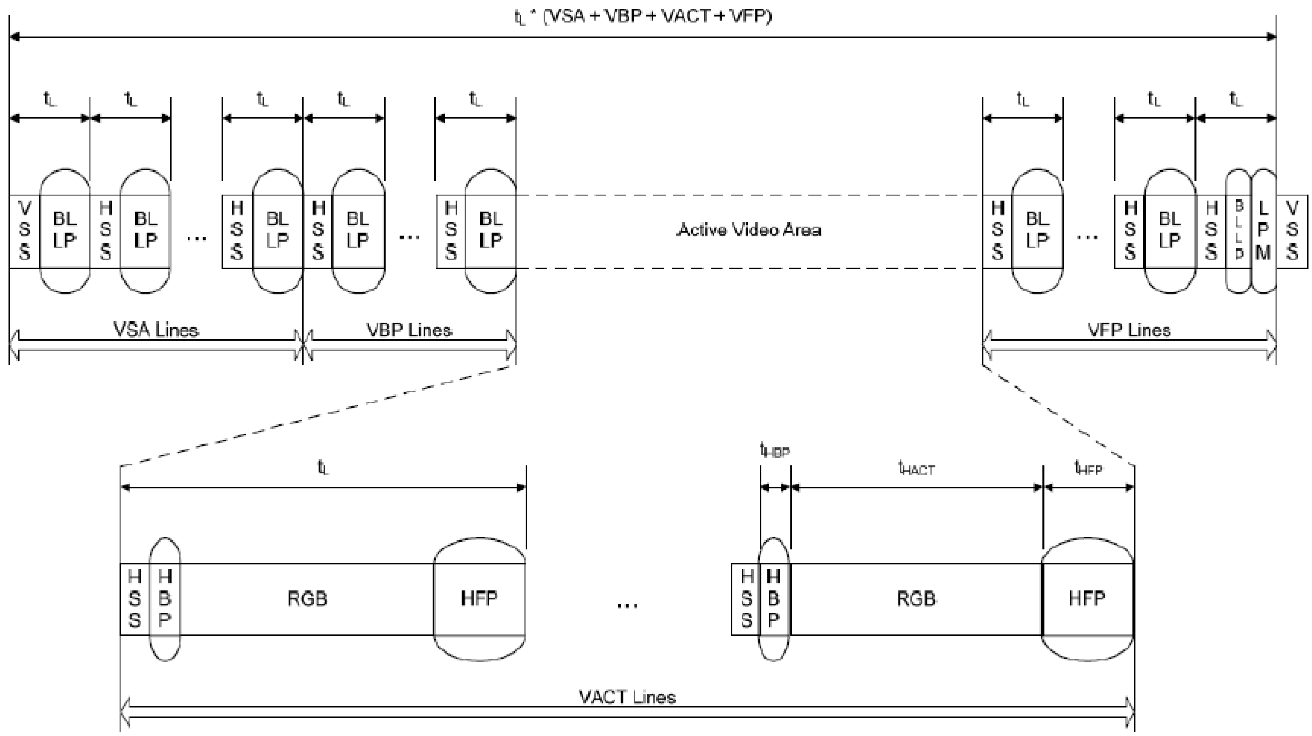


Figure 6: Video Mode Interface Timing: Non-Burst Transmission with Sync Events

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

4. Burst mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction.

Following HS pixel data transmission, the bus may stay in HS Mode for sending blanking packets or go to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its interval buffer memory to the display device. An example of this mode is shown in Figure 7

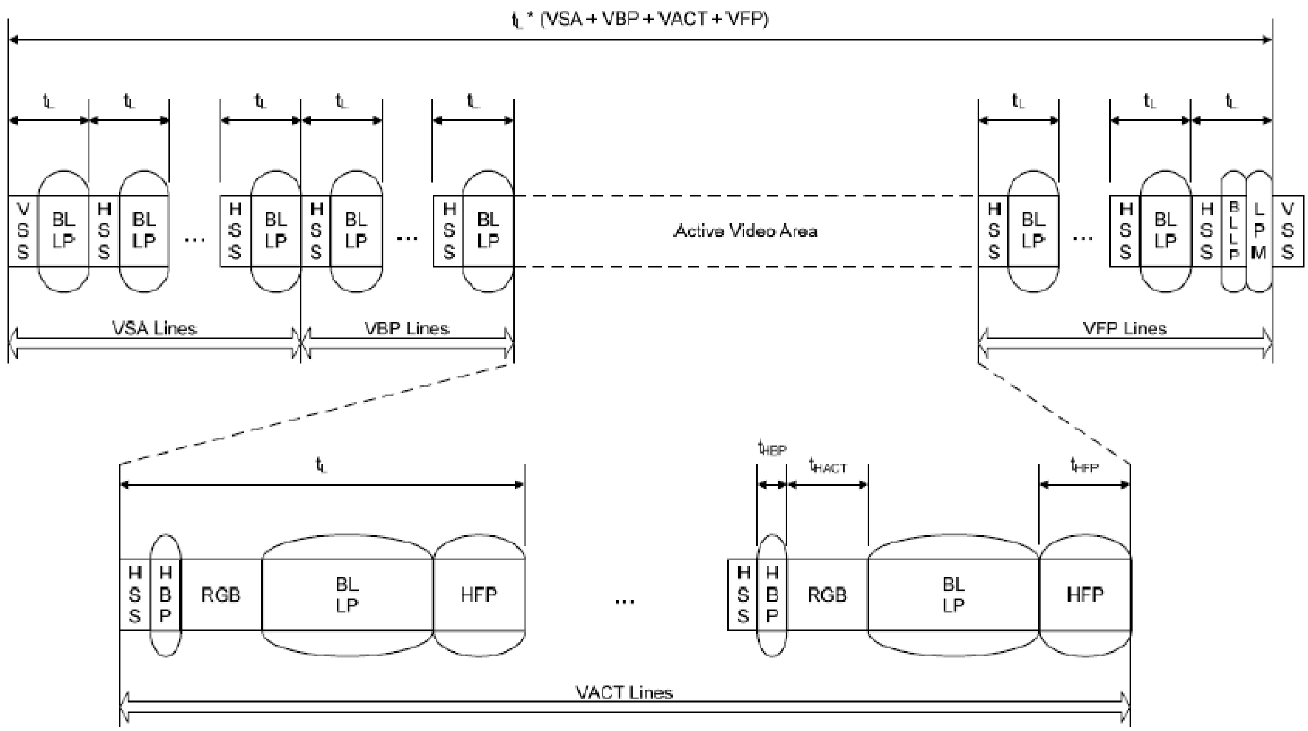


Figure 7: Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.3. DC characteristic

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
Low level input voltage	VIL	0	-	0.2VDD	V	Note 1
High level input voltage	VIH	0.8VDD	-	VDD	V	

Note 1:RESET, UPDN,SHLR

M8.4. IPI DC characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	120	ohm
HS transmit differential voltage(V_{OD}=V_{DP}-V_{DN})	|VOD|	100	200	250	mV
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Ground shift	V_{GNDSH}	-50	-	50	mV
Logic 0 input threshold	V_{IL}	0	-	550	mV
Logic 1 input threshold	V_{IH}	1000	-	1350	mV
Input hysteresis	V_{HYST}	25	-	-	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V
Output impedance of Low Power Transmitter	ZOLP	110			ohm
Logic 0 contention threshold	$V_{ILCD,MAX}$	-	-	200	mV
Logic 1 contention threshold	$V_{IHCD,MIN}$	450	-	-	mV
MIPI Digital Operating Current	$I_{VDDMIPI}$	-	15	20	mA
MIPI Digital Stand-by Current	I_{STMIPI}	-	-	250	uA

Note: MIPI Digital Operating and Stand-by Current is at RT 25℃ condition.

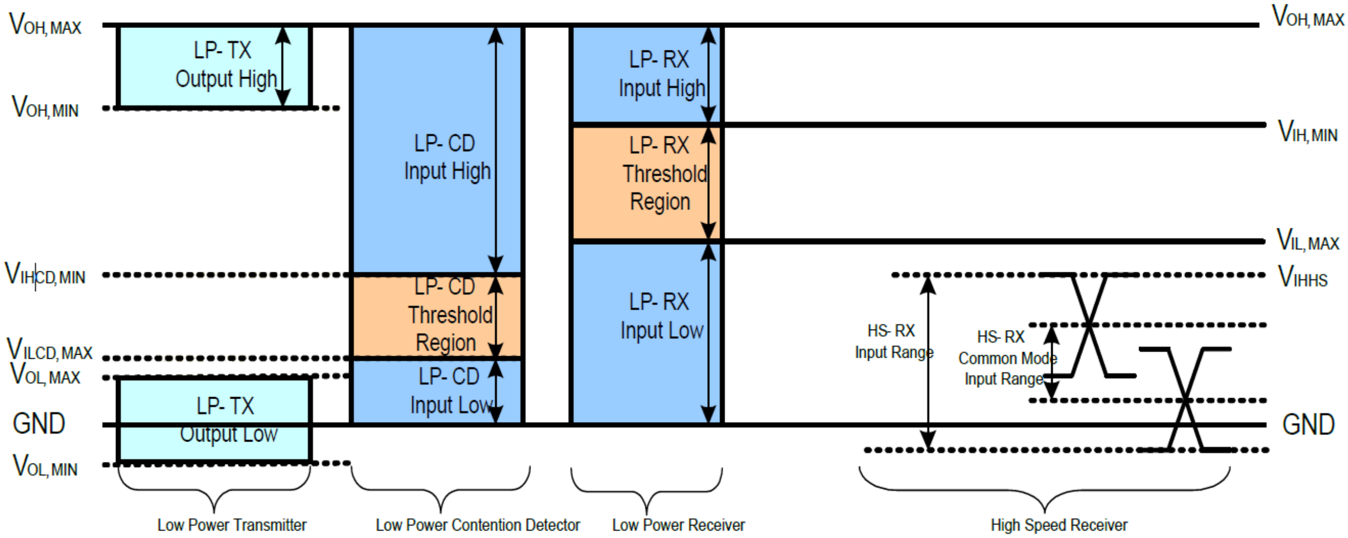


Figure 8: MIPI signaling and contention voltage levels

8.5. MIPI AC characteristic

1.MIPI Low Power Transmitter AC Specification

Parameter		Symbol	Min	Typ	Max	Units	Notes
15%~85% rising time and falling time		T_{RLP} / T_{FLP}	-	-	25	ns	-
30%~85% rising time and falling time		T_{REOT}	-	-	35	ns	-
Pulse width of LP exclusive-OR clock	First LP EXOR clock pulse after STOP state or Last pulse before stop state	$T_{LP\text{-}PULSE\text{-}TX}$	100	-	-	ns	-
	All other pulses		100	-	-	ns	-
Period of the LP EXOR clock(LP Speed)		$T_{LP\text{-}PER\text{-}TX}$	200	-	-	ns	-
Slew Rate @CLOAD =0pF		$\delta V/\delta t_{SR}$	20	-	500	mV/ns	-
Slew Rate @CLOAD =5pF			20	-	200	mV/ns	-
Slew Rate @CLOAD =20pF			20	-	150	mV/ns	-
Slew Rate @CLOAD =70pF			20	-	100	mV/ns	-
Load Capacitance		T_{RLP}	-	-	70	pF	-

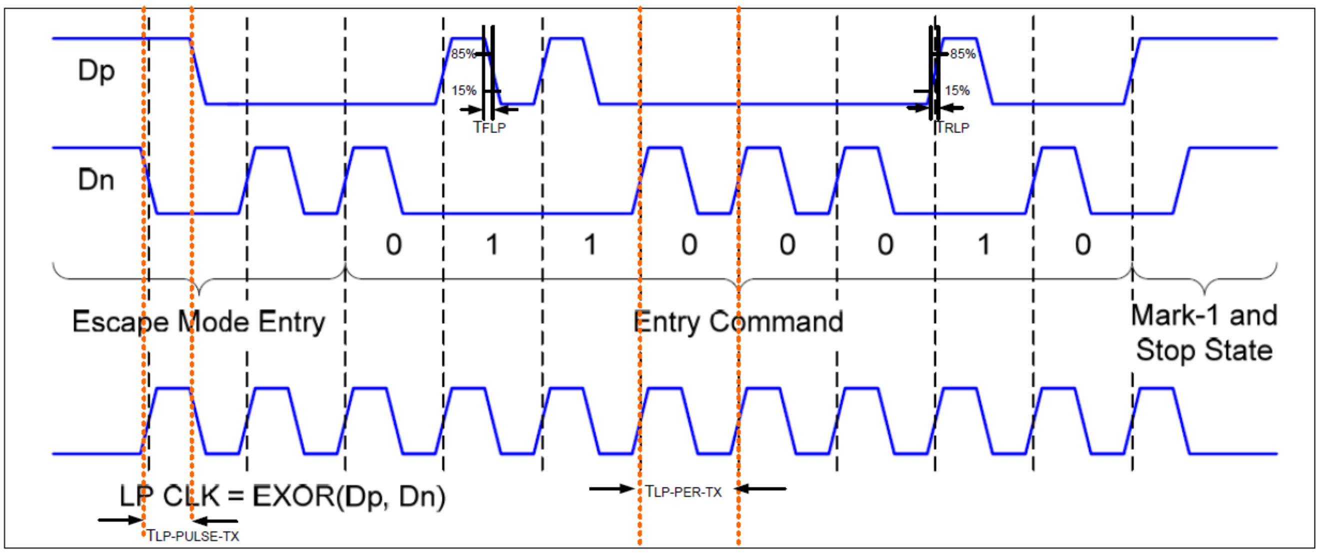


Figure 9: MIPI LP AC timing

2.MIPI Low Power Turnaround Procedure

Turnaround Procedure Operation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period	T_{LPX}	100	-	-	ns
Time-out before new TX side start driving	$T_{TA\text{-}Sure}$	T_{LPX}	-	$2T_{LPX}$	ns
Time to drive LP-00 by new TX	$T_{TA\text{-}GET}$	-	$5T_{LPX}$	-	ns
Time to drive LP-00 after Turnaround Request	$T_{TA\text{-}GO}$	-	$4T_{LPX}$	-	ns

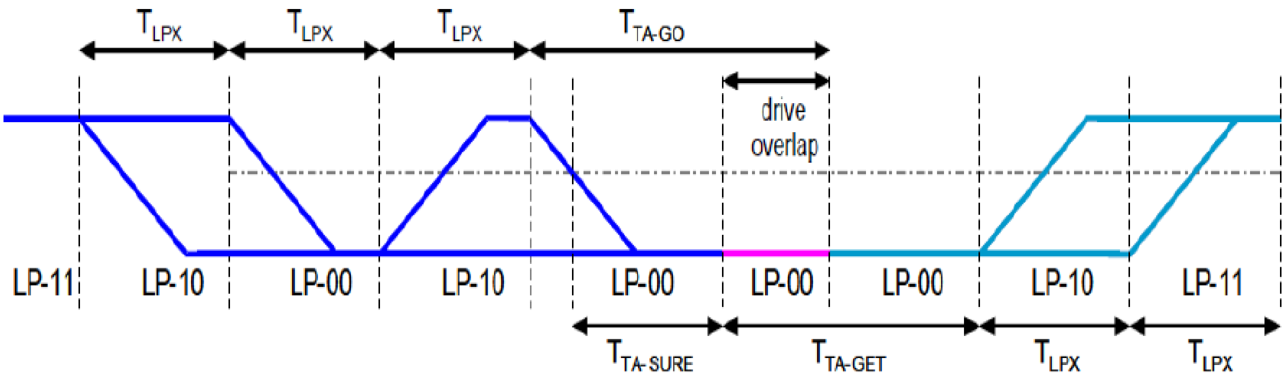


Figure 10: Turnaround Procedure

3.MIPI High Speed AC characteristics

DP: D0P/ D1P/D2P/D3P
DN: D0N/ D1N /D2N/D3P

Parameter	Descript	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60 ns + 52*UI	-		ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-		UI
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PRE.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.	Time for Dn to reach VTERM-EN	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THSPREPARE.	85 ns + 6*UI	-	145 ns + 10*UI	ns
T_{EOT}	Time from start of THS-TRAIL or TCLK-TRAIL period to start of LP-11 state	-	-	105ns+n*12*UI	-
$T_{HS-EXIT}$(1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	THS-PREPARE + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	100	-	-	ns
Ratio T_{LPX}	Ratio of TLPX(MASTER)/TLPS(SLAVE) between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	5*T_{LPX}			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	4*T_{LPX}			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	2*T_{LPX}	ns

Note: (1) For $T_{CLK-POST}$ example:
$T_{CLK-POST}$ min value =164UI when MIPI max frequency per lane = 0.5Gbps.
$T_{CLK-POST}$ min value =112UI when MIPI max frequency per lane = 1Gbps

(2) For TEOT:

When n = 1 for Forward-direction HS mode and n=4 for Reverse-direction HS mode

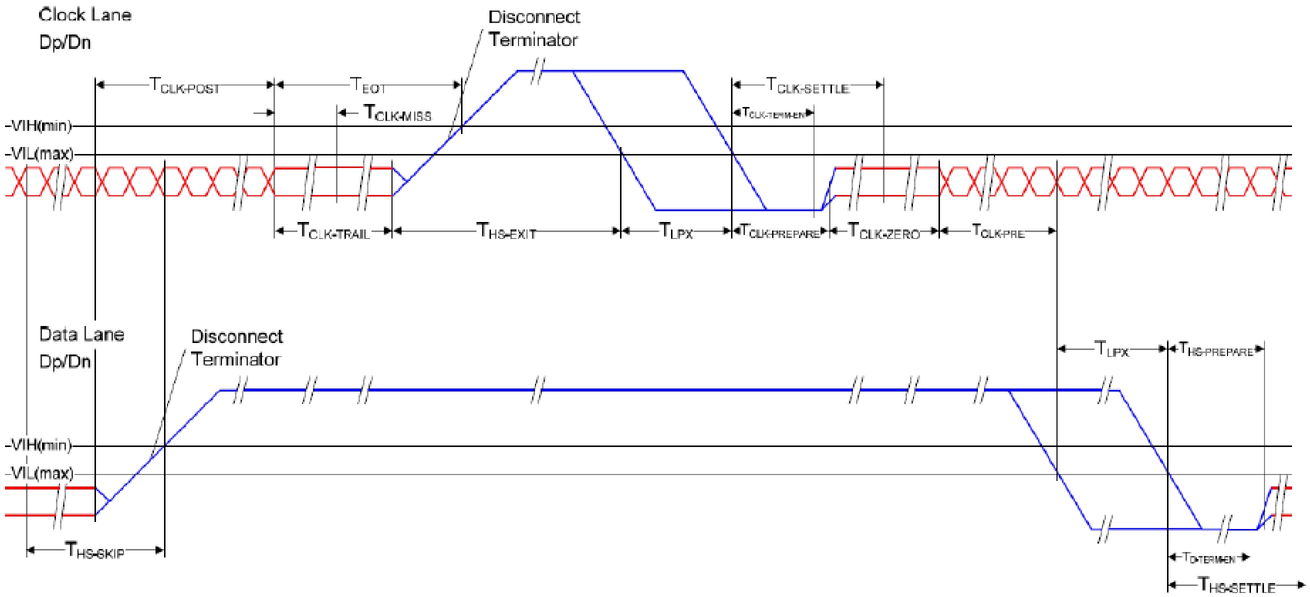


Figure 11: Switching the clock lane between clock transmission and low-power mode

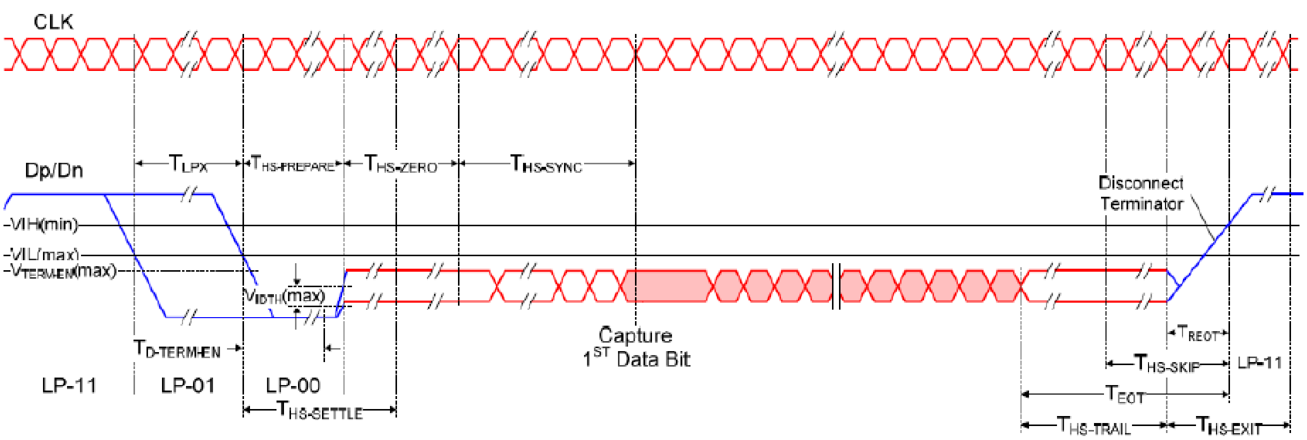


Figure 12: Timing of high-speed data transmission in bursts

4.MIPI data-clock timing specification

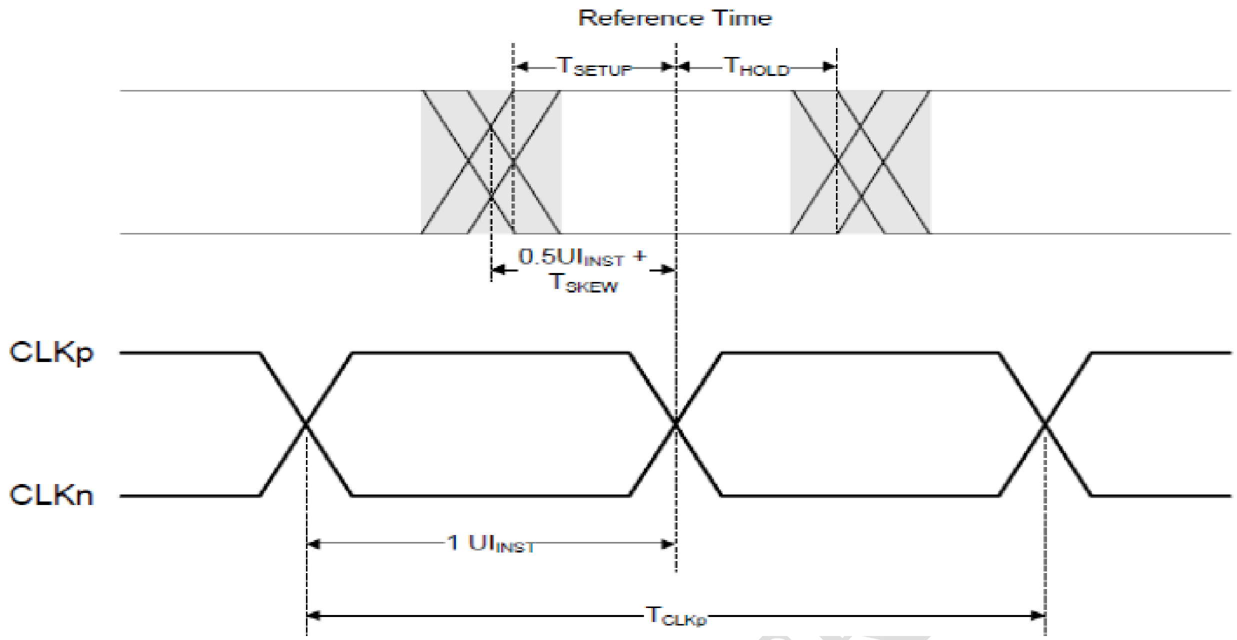


Figure 13: Data to clock timing

Parameter	Symbol	Min	Typ	Max	Units
Data to clock setup time	TSETUP[RX]	0.15(1)	-	-	UI_{INST}
Data to clock hold time	THOLD[RX]	0.15(1)	-	-	UI_{INST}

Note: (1) Total setup and hold window for receiver of 0.3* UIINST.

Table 1: Data to Clock Timing Specifications

8.6. MIPI timing characteristic

MIPI Input Timing	Symbol	1024RGBx600			Unit
		Min	Typ	Max	
MIPI 24-bit RGB@ 2 lane Operating Frequency	-	400	616	750	Mbps
MIPI 24-bit RGB@ 4 lane Operating Frequency	-	200	308	500	Mbps
Frame Rate@ 2 lane	-	48	60	-	Hz
Frame Rate@ 4 lane	-	48	60	-	Hz
Horizontal Total	tht	1114	1344	1400	DCLK
Hsync Pulse width	ths	1	24	HBP-1	DCLK
Horizontal Back Porch	thb	60	160	160	DCLK
Horizontal Valid Data	thd	1024			DCLK
Horizontal Front Porch	thfp	30	160	216	DCLK
Vertical Total	tvt	620	635	800	THT
Vsync Pulse Width	tvs	1	2	VBP-1	THT
Vertical Back Porch	tvb	8	23	100	THT
Vertical Valid Data	tvd	600			THT
Vertical Front Porch	tvfp	12	12	100	THT

9.Power Sequence

9.1. Power On Sequence

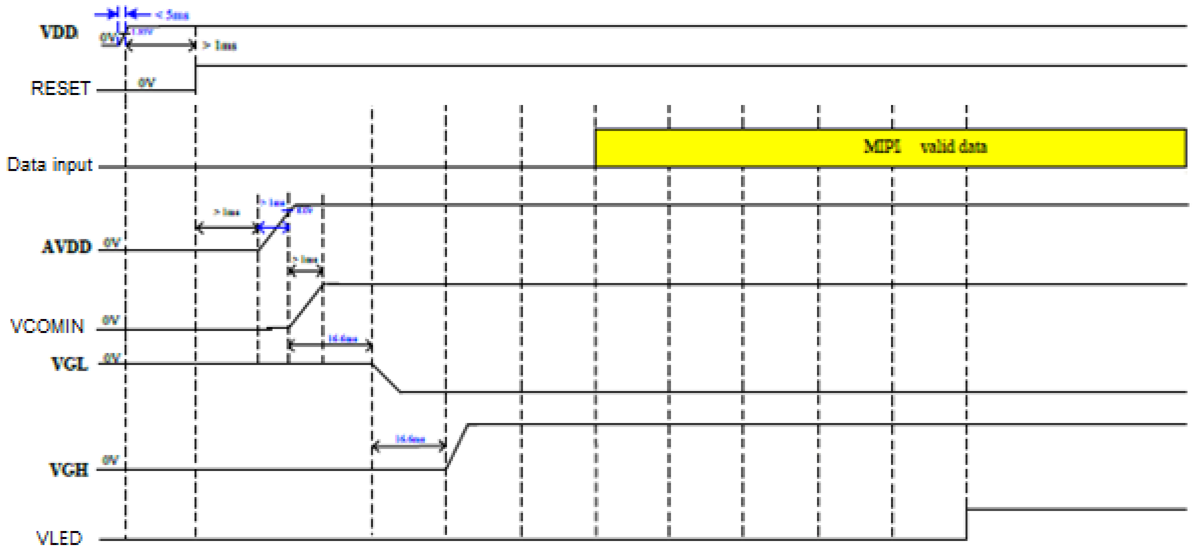


Figure 14: Power On timing chart

9.2. Power Off Sequence

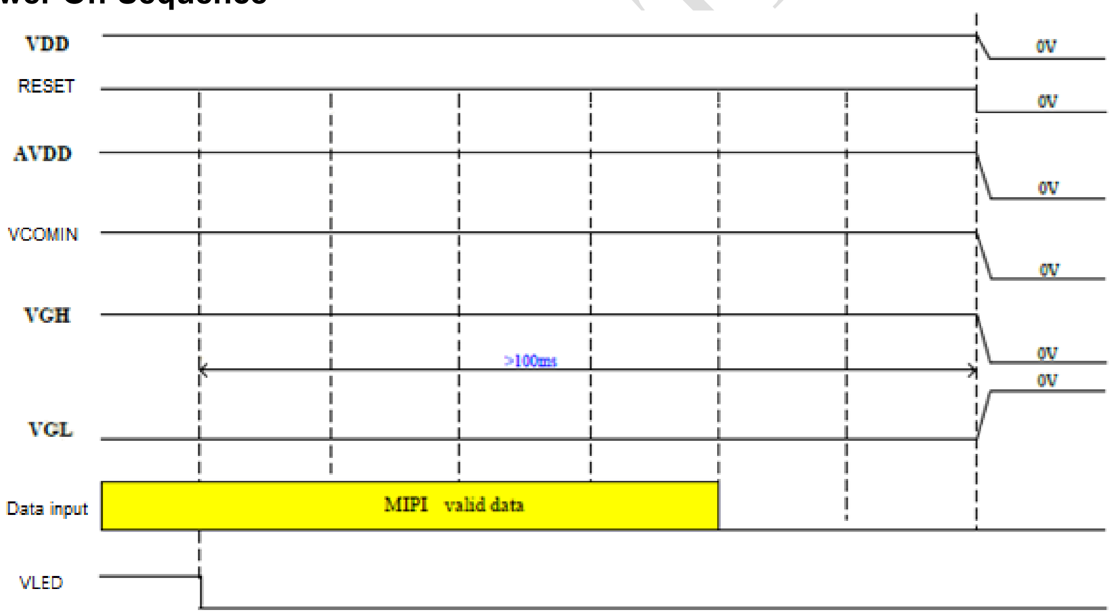


Figure 15: Power Off timing chart

10.Optical Characteristics

TFT LCD characteristic

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response time		Tr+ Tf	θ=0°、Φ=0°	-	30	35	.ms	Note 3
Contrast ratio		CR	At optimized viewing angle	700	1000	-	-	Note 4
Color Chromaticity	White	Wx	θ=0°、Φ=0	0.264	0.314	0.364	-	Note 2,6,7
		Wy		0.272	0.322	0.372	-	
Viewing angle	Hor.	ΘR	CR≧10	70	80	-	Deg.	Note 1
		ΘL		70	80	-		
	Ver.	ΦT		70	80	-		
		ΦB		70	80	-		
Brightness		-	-	500	600	-	cd/m2	Center of display
Uniformity		(U)	-	75	-	-	%	Note 5

Ta=25±2℃,

Note 1: Definition of viewing angle range

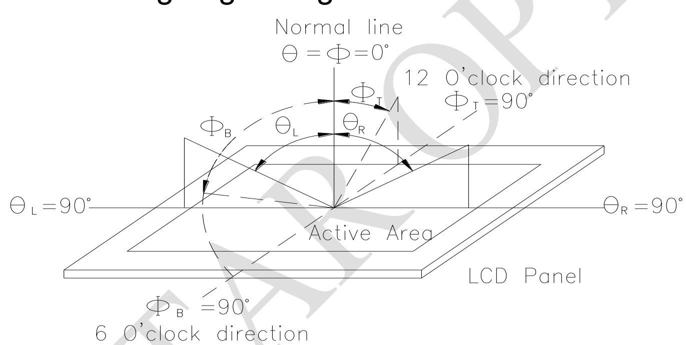


Fig.10.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

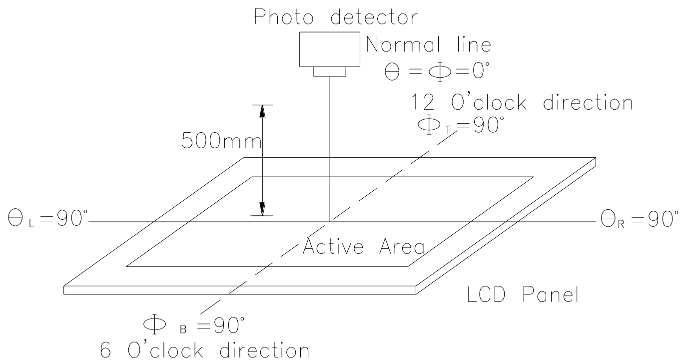
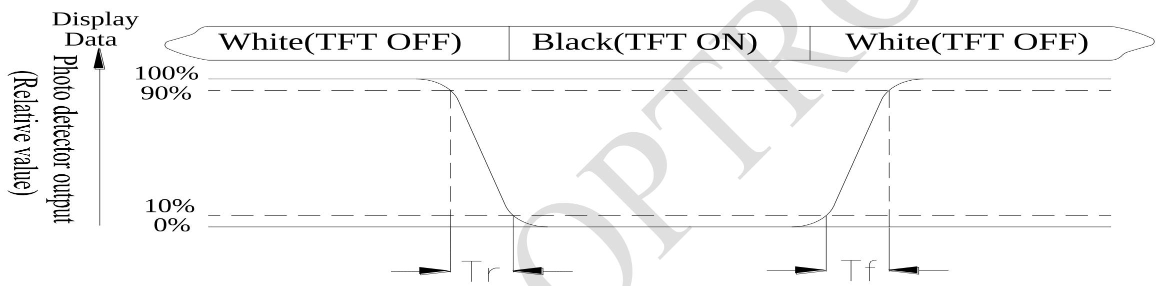


Fig. 10.2. Optical measurement system setup

Note 3: Definition of Response time:
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%



Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.
Luminance Uniformity (U) = Lmin/Lmax x100%
L = Active area length
W = Active area width

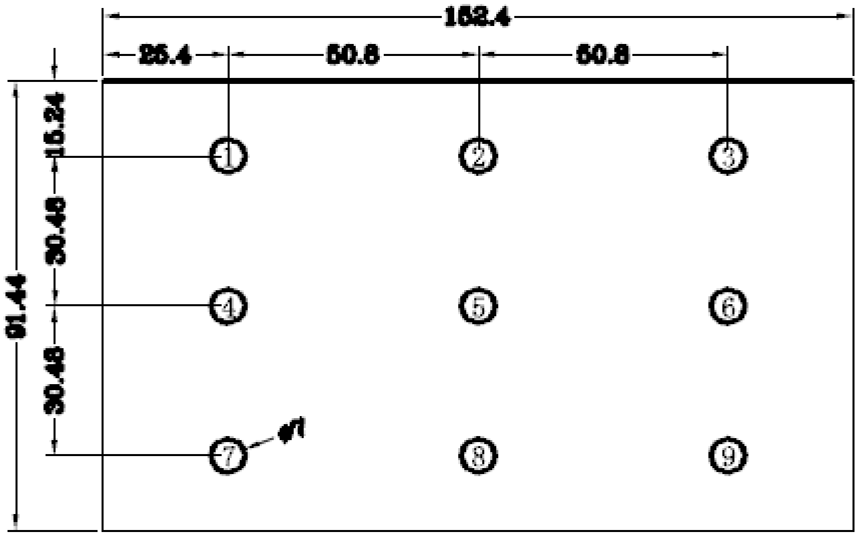


Fig10.3. Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

11.Reliability

Content of Reliability Test (Super Wide temperature, -30℃~85℃)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	90℃ 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-40℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85℃ 200hrs	2
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-30℃ 200hrs	1,2
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -30℃ 25℃ 85℃ 30min 5min 30min 1 cycle	-30℃/85℃ 10 cycles	2
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±4KV(Contact), ±4KV (air), RS=330Ω CS=150pF 10 times	4

Note1: No dew condensation to be observed.
Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.
Note3: The packing have to including into the vibration testing.
Note4: Endurance test applying the electric stress to the finished product housing

12.Initial Code For Reference

```
void JD9165A_tft_config(void)
{
    // resolution
    TFT_CFG.Horizontal = 1024;
    TFT_CFG.Vertical = 600;

    TFT_CFG.HFP = 160;
    TFT_CFG.HBP = 136;
    TFT_CFG.HPW = 24;

    TFT_CFG.VFP = 12;
    TFT_CFG.VBP = 21;
    TFT_CFG.VPW = 2;
    TFT_CFG.PCLK = 51200;
    TFT_CFG.REFRESH_RATE = 60;

    // bmp address
    TFT_CFG.BMP_ADDR = 0x000000;

    // display chip
    TFT_CFG.SSD1963 = ssd1963_null;
    TFT_CFG.RA8876 = ra8876_initial;
    TFT_CFG.RA8877 = ra8877_null;
    TFT_CFG.SSD2828 = ssd2828_initial;

    // RA8876 OSC
    TFT_CFG.OSC_FREQ = 10;
    TFT_CFG.SCAN_FREQ = 51;
    TFT_CFG.CORE_FREQ = TFT_CFG.SCAN_FREQ * 2;
    TFT_CFG.DRAM_FREQ = TFT_CFG.CORE_FREQ;

    // RA8876 parameter
    TFT_CFG.RA8876_TFT_Panel_Output = TFT_24bits;
    TFT_CFG.HostDataBus_Width = Host_16bits_DataBus;
    TFT_CFG.Memory_Write_Direction = 0;
    TFT_CFG.MainImage_ColorDepth = COLOR_DEPTH_16BPP;
    TFT_CFG.synchronous_signals = Sync_Mode;
    TFT_CFG.PCLK_Inversion = RISING;
    TFT_CFG.AW_COLOR_DEPTH = COLOR_DEPTH_16BPP;

    // SSD2828 parameter
    TFT_CFG.HSYNC_POLARITY = LOW_ACTIVE;
    TFT_CFG.VSYNC_POLARITY = LOW_ACTIVE;
    TFT_CFG.LAUNCH_TYPE = RISING;
    TFT_CFG.ORDER = RGB;
    // mipi setting
    TFT_CFG.LANE = 4;
```

```
	TFT_CFG.DEPTH = bpp24;
	TFT_CFG.LANE_SPEED = (uint64_t)TFT_CFG.PCLK * calc_bpp(TFT_CFG.DEPTH) / TFT_CFG.LANE / 1000;

	// Touch IC
	TFT_CFG.TP = ILI2130;
	TFT_CFG.FINGER = 5;
	TFT_CFG.CTP_RES.XMIN = 0;
	TFT_CFG.CTP_RES.XMAX = 16384;

	TFT_CFG.CTP_RES.YMIN = 0;
	TFT_CFG.CTP_RES.YMAX = 16384;

	TFT_CFG.POINT_SIZE = 6;
}

void JD9165A_init_config(void)
{
	mipi_dsi_dcs_write_1P(0x30, 0x00);
	mipi_dsi_dcs_write_seq(0xF7, 0x49, 0x61, 0x02, 0x00);
	mipi_dsi_dcs_write_1P(0x30, 0x01);
	mipi_dsi_dcs_write_1P(0x04, 0x00); // R04h[2]SHLR、R04h[3]UPDN setting by H/W pin
	// mipi_dsi_dcs_write_1P(0x05, 0x01); // BIST_EN setting by register
	// mipi_dsi_dcs_write_1P(0x06, 0x41); // BIST mode、r_shlr=1
	mipi_dsi_dcs_write_1P(0x06, 0x01); // r_shlr=1
	mipi_dsi_dcs_write_1P(0x0B, 0x10);
	mipi_dsi_dcs_write_1P(0x1F, 0x05);
	mipi_dsi_dcs_write_1P(0x23, 0x3C);
	mipi_dsi_dcs_write_1P(0x30, 0x02);
	mipi_dsi_dcs_write_1P(0x03, 0x22);
	mipi_dsi_dcs_write_1P(0x04, 0x06);
	mipi_dsi_dcs_write_1P(0x05, 0x66);
	mipi_dsi_dcs_write_1P(0x06, 0x80);
	mipi_dsi_dcs_write_1P(0x08, 0x3C);

	mipi_dsi_dcs_write_seq(0x0B, 0x17, 0x1B, 0x03, 0x10, 0x11, 0x1F, 0x1D, 0x06, 0x08, 0x16, 0x03);
	mipi_dsi_dcs_write_seq(0x0C, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03);
	mipi_dsi_dcs_write_seq(0x0D, 0x05, 0x1A, 0x03, 0x10, 0x11, 0x1E, 0x1C, 0x07, 0x09, 0x0A, 0x03);
	mipi_dsi_dcs_write_seq(0x0E, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03);
	mipi_dsi_dcs_write_seq(0x0F, 0x0A, 0x1A, 0x03, 0x10, 0x11, 0x1C, 0x1E, 0x09, 0x07, 0x05, 0x03);
	mipi_dsi_dcs_write_seq(0x10, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03);
	mipi_dsi_dcs_write_seq(0x11, 0x16, 0x1B, 0x03, 0x10, 0x11, 0x1D, 0x1F, 0x08, 0x06,
```

```
0x17, 0x03);
	mipi_dsi_dcs_write_seq(0x12, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03,
0x03, 0x03);
	mipi_dsi_dcs_write_seq(0x13, 0x00, 0x00, 0x00, 0x00);
	mipi_dsi_dcs_write_seq(0x14, 0x00, 0x00, 0x00, 0x00);
	mipi_dsi_dcs_write_seq(0x15, 0x00, 0x00, 0x00, 0x00);
	mipi_dsi_dcs_write_1P(0x17, 0x40);
	mipi_dsi_dcs_write_1P(0x18, 0x82);
	mipi_dsi_dcs_write_1P(0x30, 0x06);
	mipi_dsi_dcs_write_seq(0x12, 0x3F, 0x29, 0x2B, 0x39, 0x26, 0x25, 0x26, 0x25, 0x23,
0x14, 0x29, 0x21, 0x17, 0x2A);
	mipi_dsi_dcs_write_seq(0x13, 0x3F, 0x29, 0x2B, 0x39, 0x26, 0x25, 0x26, 0x25, 0x23,
0x14, 0x29, 0x21, 0x17, 0x2A);
	mipi_dsi_dcs_write_1P(0x30, 0x07);
	mipi_dsi_dcs_write_1P(0x00, 0x06);
	mipi_dsi_dcs_write_1P(0x0D, 0x01);
	mipi_dsi_dcs_write_1P(0x30, 0x08);
	mipi_dsi_dcs_write_1P(0x01, 0xB4);
	mipi_dsi_dcs_write_1P(0x30, 0x0A);
	mipi_dsi_dcs_write_1P(0x02, 0x4F);
	mipi_dsi_dcs_write_1P(0x0B, 0x40);
	mipi_dsi_dcs_write_1P(0x10, 0x82); // Z 改反 Z
	mipi_dsi_dcs_write_1P(0x13, 0x20); // 0x3A->0x20(减小 debug-20 度显示竖纹)
	mipi_dsi_dcs_write_1P(0x30, 0x0D);
	mipi_dsi_dcs_write_1P(0x0D, 0x04);
	mipi_dsi_dcs_write_1P(0x10, 0x0B);
	mipi_dsi_dcs_write_1P(0x11, 0x0B);
	mipi_dsi_dcs_write_1P(0x12, 0x0B);
	mipi_dsi_dcs_write_1P(0x13, 0x0B);
	mipi_dsi_dcs_write_1P(0x30, 0x00);

	mipi_dsi_dcs_write_NP(0x11); // Sleep Out
	delay_ms(120);
	mipi_dsi_dcs_write_NP(0x29); // Display On
	delay_ms(50);
}
```

LCM Sample Estimate Feedback Sheet		
Module Number： ________________		
1、Panel Specification：		
1. Panel Type：	□ Pass	□ NG ,________________
2. View Direction：	□ Pass	□ NG ,________________
3. Numbers of Dots：	□ Pass	□ NG ,________________
4. View Area：	□ Pass	□ NG ,________________
5. Active Area：	□ Pass	□ NG ,________________
6.Operating Temperature：	□ Pass	□ NG ,________________
7.Storage Temperature：	□ Pass	□ NG ,________________
8.Others：________________		
2、Mechanical Specification：		
1. PCB Size：	□ Pass	□ NG ,________________
2.Frame Size：	□ Pass	□ NG ,________________
3.Materal of Frame：	□ Pass	□ NG ,________________
4.Connector Position：	□ Pass	□ NG ,________________
5.Fix Hole Position：	□ Pass	□ NG ,________________
6.Backlight Position：	□ Pass	□ NG ,________________
7. Thickness of PCB：	□ Pass	□ NG ,________________
8. Height of Frame to PCB：	□ Pass	□ NG ,________________
9.Height of Module：	□ Pass	□ NG ,________________
10.Others：	□ Pass	□ NG ,________________
3、Relative Hole Size：		
1.Pitch of Connector：	□ Pass	□ NG ,________________
2.Hole size of Connector：	□ Pass	□ NG ,________________
3.Mounting Hole size：	□ Pass	□ NG ,________________
4.Mounting Hole Type：	□ Pass	□ NG ,________________
5.Others：	□ Pass	□ NG ,________________
4、Backlight Specification：		
1.B/L Type：	□ Pass	□ NG ,________________
2.B/L Color：	□ Pass	□ NG ,________________
3.B/L Driving Voltage (Reference for LED Type)：□ Pass □ NG ,____________		
4.B/L Driving Current：	□ Pass	□ NG ,________________
5.Brightness of B/L：	□ Pass	□ NG ,________________
6.B/L Solder Method：	□ Pass	□ NG ,________________
7.Others：	□ Pass	□ NG ,________________

＞＞ **Go to page 2** ＜＜

Page: 2

Module Number：____________________

5、Electronic Characteristics of Module：

1.Input Voltage：	□ Pass	□ NG ,___________________________
2.Supply Current：	□ Pass	□ NG ,___________________________
3.Driving Voltage for LCD：	□ Pass	□ NG ,____________________________
4.Contrast for LCD：	□ Pass	□ NG ,____________________________
5.B/L Driving Method：	□ Pass	□ NG ,___________________________
6.Negative Voltage Output：	□ Pass	□ NG ,__________________________
7.Interface Function：	□ Pass	□ NG ,___________________________
8.LCD Uniformity：	□ Pass	□ NG ,___________________________
9.ESD test：	□ Pass	□ NG ,___________________________
10.Others：	□ Pass	□ NG ,__________________________

6、Summary：

Sales signature：_________________

Customer Signature：_____________ **Date：___/___/___**