Re-imagining Cellular IoT Solutions

Cavli CQS29X
LTE CAT 4/2G Android/Linux Smart Module

Hardware Manual

External Release Version 1.7

Connect to our website and feel free to contact our technical support team for any assistance.

Cavli Inc

99 South Almaden Blvd., Suite 600, San Jose, California, 95113

Web: www.cavliwireless.com

IoT Connectivity Platform: www.cavlihubble.io

Support Center

https://www.cavliwireless.com/support-center.html

e-Mail: support@cavliwireless.com

For sales enquiries

https://www.cavliwireless.com/contact-us.html

e-Mail: sales@cavliwireless.com

More IoT Modules

https://www.cavliwireless.com/iot-modules/cellular-modules.html

Table of Contents

VERSION HISTORY

Version	Edit	Date
ERV 1.0	• Initial Version	17/09/2023
ERV 1.1	• Updated Timing Diagram	22/07/2024
ERV 1.2	• Pin Name and Functions updated • FM Antenna Information added • Memory information updated • Temperature information updated	28/08/2024
ERV 1.3	• Added DC characteristics	25/09/2024
ERV 1.4	• Updated Module I/O level • Updated Power consumption details • Mechanical Information updated	04/10/2024
ERV 1.5	• Updated power domain of Reset key	26/11/2024
ERV 1.6	• Updated OS details	24/12/2024
ERV 1.7	• Added Linux power consumption	21/01/2025

1 Introduction

This document is the **Hardware Manual** of the Cavli Wireless solution product **CQS29X Module**, which describes:

- ✓ The hardware composition and functional features of the module
- ✓ The definition and usage of the application interface
- ✓ The electrical performance and mechanical properties of the module

This document and the other application documents combined will enable users to develop end devices with the CQS29X Module.

2 Module Overview

2.1. Module Introduction

CQS29X is the LTE Cat 4 module from Cavli C-Series module family that supports data rates up to 150 Mbit/s in downlink and 50 Mbit/s in uplink with 2G fall back. The Android/Linux smart module is equipped with the Cortex A53 quad-core CPU architecture with built-in Adreno™ 702 GPU delivering higher graphics capabilities, better quality images and excellent power performance.

The CQS29X communication subsystem integrates **LTE CAT 4** along with GSM/GPRS technology. The modem Baseband and its RF transceiver covers 1/ 2/ 3/ 4/ 5/ 7/ 8/ 12/ 13/ 18/ 19/ 20/ 25/ 26/ 28/ 40/ 41/ 66/ 71 bands and GSM 900/GSM 1800 for world-wide deployment.

CQS29x supports versatile features such as in-built GNSS, USB 2.0/USB3.1, Camera and Display support, Touch Screen support, Bluetooth 5.0 & Wi-Fi making it ideal for wide range of applications such as automobile clusters, e-mobility, telematics, fleet management and point-of-sale terminals.

The CQS29x module can be used in the following applications

- ✓ Automobile Clusters
- ✓ Vehicle telematics
- ✓ Infotainment Unit
- ✓ Device management
- ✓ POS system.
- ✓ Smart city and smart home applications
- ✓ Connected retail applications- point of sale devices, automated teller machines, vending machines etc.

Table 1 Variant list based on Band configuration

Module	Bands
CQS29x - WW	**LTE BANDS:** 1/2/3/4/5/7/8/12/13/18/19/20/25/26/28/38/40/41/66/71 **GSM BANDS:** GSM900/ GSM1800
CQS29x - EAJ	**LTE BANDS:** 1/3/5/7/8/18/19/20/26/28/38/40/41 **GSM BANDS:** GSM900/ GSM1800
CQS29x - AN	**LTE BANDS:** 1/3/5/8/18/19/26/28 **GSM BANDS:** GSM900/ GSM1800
CQS29x - IN	**LTE BANDS:** 1/3/5/8/40/41 **GSM BANDS:** GSM900/ GSM1800
CQS29x - NA	**LTE BANDS:** 2/4/5/7/8/12/13/17/25/66/71 **GSM BANDS:** GSM900/ GSM1800

2.2. Module Characteristics

Table 2 Key Features

Characteristics		Description
Physical Characteristics		40.5 x 40.5 x 2.7 mm
Fixed Way		LCC+LGA package
Operating Voltage		3.5V – 4.4V Typical Voltage 4.2 V
Application Processor		Quad-core ARM Cortex-A53 64-bit CPU @ 2.0 GHz with 512 KB L2 cache
Modem DSP		Hexagon DSP v66k core
GPU		Adreno™ 702 GPU with 64-bit addressing, up to 845MHz
Memory Configuration		✓ 2GB LPDDRX + 16GB eMMC 5.1 ✓ 3GB LPDDRX + 32GB eMMC 5.1 ✓ 4GB LPDDRX + 64GB eMMC 5.1
OS		Android 14 / Linux
WLAN Features		✓ Support 2.4GHz & 5GHz frequency ✓ IEEE 802.11a/b/g/n/ac standards
Bluetooth Features		Bluetooth 5.0
Application Interface	USIM card	✓ Supports 1.8/2.95 V. ✓ Card detection function
	USB	✓ USB2.0 (High-Speed)/ USB3.1(Full-speed)
	UART	✓ Upto 7 UARTs ✓ UART4 is for Debugging
	Audio	✓ 3x Analog Audio Input (2x MIC) ✓ Upto 2 Digital Audio Input (2x DMIC) ✓ 3 Analog Audio Out (1x Head, 1x Aux, 1x Ear)

	SDC	✓ Compliant with SDIO 3.0 protocol ✓ 4-bit SDC
	I2C	✓ Upto 4 I2C Interfaces ✓ Version 3.0 Standard
	I3C	✓ Upto 2 I3C Interface ✓ Sensor based. Mainly for Accelerometer and Gyro meter
	LED Interface	✓ 1x Flash Interface ✓ 1x Charge indicator.
	GPIO	✓ Upto 71 Configurable GPIOs
	GNSS	✓ In-Built GNSS ✓ Qualcomm Location Suite V9 Engine ✓ **GNSS L1** (CQS290 & CQS291) ✓ **GNSS L1+L5** (CQS292) ✓ GPS/GLONASS/BDS/Galileo/QZSS/SBAS/ (NavIC with L5)
	ADC	✓ Generic ADC up to 15-bit resolution
	SPI	✓ Upto 5 SPI interface
	CSI	✓ 2x MIPI-CSI Interface for Camera ✓ [4 lane + 4 lane] / [4 lane + 2 lane + 1lane] ✓ D-PHY 1.2 / C-PHY 1.0 ✓ D-PHY: 2.5 Gbps/lane ✓ C-PHY: ~10 Gbps (3.42 Gbps/trio on three trios per port) ✓ 2x CCI I2C for Camera Control ✓ Support up to 25MP / 13MP +13MP with dual ISP ZSL ✓ Support 48MP nZSL
	LCM/DSI	✓ One MIPI-DSI Interface ✓ 4-bit D-PHY v1.2 ✓ 1.5 Gbps per lane architecture with split link support ✓ HD+ Display output ✓ 1680 x 720 resolution at 60FPS
	Touch Screen	✓ Capacitive Touch Screen Support ✓ Via I2C
	Antenna Interface	✓ Main x 1 ✓ Diversity x 1 ✓ GNSS × 1 ✓ Wi-Fi /BT/FM ✓ Characteristic impedance 50 Ω

	Haptic Driver	✓ Single Motor Driver Interface
Frequency Band		**LTE BANDS:** 1/ 2/ 3/ 4/ 5/ 7/ 8/ 12/ 13/ 18/ 19/ 20/ 25/ 26/ 28/38/ 40/ 41/ 66/ 71 **GSM BANDS:** GSM900/ GSM1800
Data Network		✓ FDD/TDD LTE CAT /4/2G ✓ Peak DL 150Mbps/ UL 50 Mbps (CAT 4) ✓ Peak DL 236.8Kbps/ UL 236.8 Kbps (2G)
AT Command		✓ Support for standard AT instruction sets
Network Protocol		✓ TCP(S) / UDP / HTTP(S) / MQTT(S) / FTP(S)
Temperature Range		✓ Normal working temperature: - 30℃ to +85℃ ✓ Storage temperature: -55℃ to +125℃
Humidity		RH5%～RH90%

NOTE

- *The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.*

2.3. Module Function

CQS29X Module mainly consists of the following circuit units:

- ✓ Baseband processing unit
- ✓ Power Management unit
- ✓ Memory unit
- ✓ RF Transceiver unit
- ✓ RF front-end unit
- ✓ RF Band SAW Duplex array
- ✓ Multi-Band PA
- ✓ Interfaces

The functional block diagram of the CQS29X module is shown below：

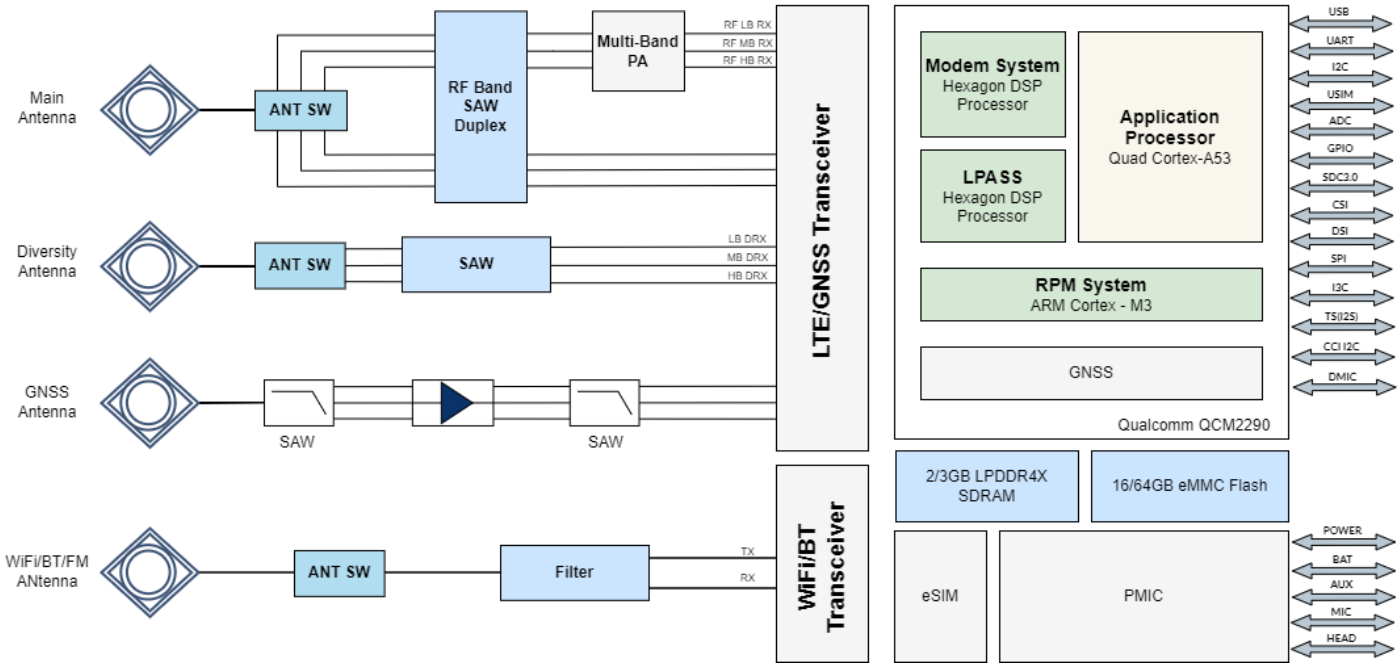


Figure 1 CQS29X Functional Block Diagram

2.4 Module Working Mode

Table 3 Working Modes

Working Mode	Description
Turn off the machine	In the case of shutdown, the module is fully powered off.
Flight Mode	The module closes the module RF circuit, unable to interact with the network
Dormancy	The module closes most functions, and it will synchronize with the network.
Ideal State	Turn on the machine and register the network successfully, in the idle state
Data transmission	The module is in working state and has data interaction with the network.

3 Interface Application Description

3.1 Chapter Overview

This chapter mainly describes the interface definition and application of this module. It contains the following sections:

- Module Interface
- Power Interface
- Switching Machine Reset Mode
- USB Interface
- UART Interface
- SPI Interface
- I2C/I3C Interfaces
- SDC interface
- USIM Interface
- Motor Drive Interface
- LED Interface
- GPIO Interface
- ADC
- LCM interface
- Touch Control Interface
- Camera interface
- Audio Interface
- Antenna Interface
- Control Interface
- GNSS Interface

3.2 Module Interface

3.2.1 CQS29X Pin Layout

CQS29X pins are assigned as follows：

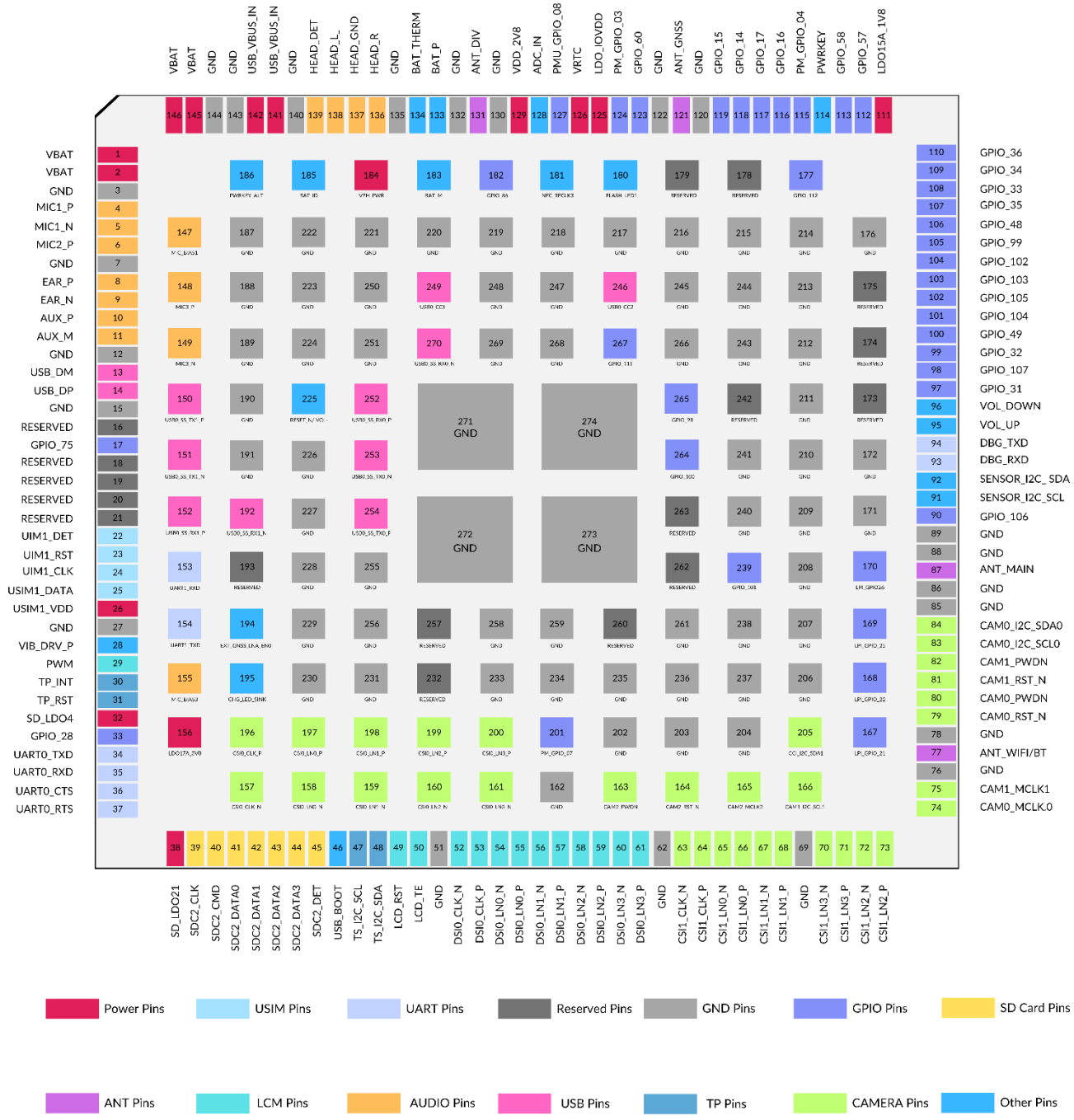


Figure 2 CQS29X module Interface definition (top view)

NOTE

- *All RESERVED and unused pin feet need to be left floating*

3.2.2 Pin Description

Table 4 Pin Description

Pin Type	Description
PAD TYPE	
AI	Analog Input
AO	Analog Output
B	Bidirectional digital with CMOS input
DI	Digital Input (CMOS)
DO	Digital Output (CMOS)
DIO	Digital Input/Output
OD	Open Drain
H	High voltage tolerant
Z	High Impedance output
PI	Power Input
PO	Power Output
PIO	Power Input/Output
Pad pull details	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpupk = default no-pull with programmable option following the colon (:) PD: pdpupk = default pull-down with programmable option following the colon (:) PU: pdpupk = default pull-up with programmable option following the colon (:) KP: pdpupk = default keeper with programmable option following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device

3.2.3 Absolute maximum ratings

The absolute maximum ratings table reflects the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Operating conditions.

Table 5 Absolute Maximum

Pin Type	V_min	V_max
P2	-0.3 V	3.41 V
P3	-0.3 V	2.09 V
P5	-0.3 V	3.41 V
P7	-0.3 V	2.09 V
P9	-0.3 V	3.52 V
VB	-0.3 V	6 V
CSI	-0.3 V	1.39 V
DSI	-0.3 V	1.39 V

3.2.4 CQS29X Pin Interface

The CQS29X module has the LGA interface. The module interface definition is shown in the following table:

Table 6 Pin Interface

Pin No.	Pin Name	Pad Type	Description & Configurable function	Pad Voltage	DC Characteristics
1	VBATT	PI	Module input Voltage Pin	VB	Vmin = 3.5V Vnom =4V Vmax = 4.4 V
2	VBATT	PI	Module input Voltage Pin	VB	
3	GND	-	Ground Pin	-	
4	MIC1_P	AI	Microphone input for channel 1 (+)	-	
5	MIC1_N	AI	Microphone input for channel 1 (-)	-	
6	MIC2_P	AI	Microphone input for headset (+)	-	
7	GND	-	Ground Pin	-	

8	EAR_P	AO	Earpiece output (+)		
9	EAR_N	AO	Earpiece output (-)		
10	AUX_P	AO	Audio line differential output (+)		
11	AUX_M	AO	Audio line differential output (-)		
12	GND	-	Ground Pin		
13	USB0_HS_SM_D_N	AIO	USB differential data (-)		
14	USB0_HS_SM_D_P	AIO	USB differential data (+)		
15	GND	-	Ground Pin		
16	RESERVED	-	-		
17	GPIO_75	DI	(U)SIM2 card hot-plug detect	P3	
18	RESERVED	-	-	P5	
19	RESERVED	-	-	P5	
20	RESERVED	-	-	P5	
21	RESERVED	-	-	-	
22	UIM1_PRESENT	DI	(U)SIM1 card hot-plug detect	P3	V_{IL}max = 0.63 V V_{IH}min = 1.17 V
23	UIM1_RESET	DO	(U)SIM1 card reset	P5	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM_VDD
24	UIM1_CLK	DO	(U)SIM1 card clock	P5	
25	USIM1_DATA	DIO	(U)SIM1 card data	P5	V_{IL}max = 0.2 × USIM_VDD V_{IH}min = 0.7 × USIM_VDD V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM_VDD
26	USIM_VDD	PO	(U)SIM1 card power supply	-	$I_o$max = 67 mA **1.8 V (U)SIM:** Vmax = 1.85 V Vmin = 1.75 V **2.95 V (U)SIM:** Vmax = 3.1 V Vmin = 2.8 V
27	GND	-	Ground Pin	-	
28	VIB_DRV	PO	Vibration motor driver output control	-	$V_O$min = 1.5 V $V_O$max = 3.3 V $I_O$max = 100 mA
29	WLED_PWM	DO	PWM Output	P3	
30	TS_INT_N	DI	TP interrupt		V_{IL}max = 0.63 V V_{IH}min = 1.17 V

31	TS_RST	DO	TP reset		V_{OL}max = 0.45 V V_{OH}min = 1.35 V
32	VREG_L4A_2P96	PO	1.8/2.95 V output power for SD card pull-up circuits		1.8/2.95 V 22 mA
33	GPIO_28	DIO	General-purpose input/output	P3	
34	UART0_TXD	DO	UART0 transmit	P3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V
35	UART0_RXD	DI	UART0 receive	P3	V_{IL}max = 0.63 V V_{IH}min = 1.17 V
36	UART0_CTS	DI	DCE clear to send signal from DTE	P3	V_{IL}max = 0.63 V V_{IH}min = 1.17 V
37	UART0_RTS	DO	DCE request to send signal to DTE	P3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V
38	VREG_L21A_2P96	PO	SD card power supply		2.95 V/841 mA
39	SDC2_CLK	DO	SD card clock	P2	
40	SDC2_CMD	DIO	SD card command	P2	
41	SDC2_DATA_0	DIO	SDIO data bit 0	P2	
42	SDC2_DATA_1	DIO	SDIO data bit 1	P2	
43	SDC2_DATA_2	DIO	SDIO data bit 2	P2	
44	SDC2_DATA_3	DIO	SDIO data bit 3	P2	
45	SD_CARD_DET_N	DI	SD card hot-plug detect	P3	V_{IL}max = 0.63 V V_{IH}min = 1.17 V
46	FORCED_USB_BOOT	DI	Force the module into emergency download mode	P3	
47	TS_I2C_SCL	OD	TP I2C clock	P3	
48	TS_I2C_SDA	OD	TP I2C data	P3	
49	LCD_RST_N	DO	LCD reset	P3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V
50	LCD_TE	DI	LCD tearing effect	P3	V_{IL}max = 0.63 V V_{IH}min = 1.17 V
51	GND	-	Ground Pin	-	
52	DSI0_CLK_N	AO	LCD MIPI clock (-)	DSI	
53	DSI0_CLK_P	AO	LCD MIPI clock (+)	DSI	
54	DSI0_LN0_N	AO	LCD MIPI lane 0 data (-)	DSI	
55	DSI0_L0_P	AO	LCD MIPI lane 0 data (+)	DSI	
56	DSI0_L1_N	AO	LCD MIPI lane 1 data (-)	DSI	

57	DSI0_L1_P	AO	LCD MIPI lane 1 data (+)	DSI	
58	DSI0_L2_N	AO	LCD MIPI lane 2 data (-)	DSI	
59	DSI0_L2_P	AO	LCD MIPI lane 2 data (+)	DSI	
60	DSI0_L3_N	AO	LCD MIPI lane 3 data (-)	DSI	
61	DSI0_L3_P	AO	LCD MIPI lane 3 data (+)	DSI	
62	GND	-	Ground Pin	-	
63	CSI1_CLK_N	AI	MIPI CSI1 clock (-)	CSI	
64	CSI1_CLK_P	AI	MIPI CSI1 clock (+)	CSI	
65	CSI1_LN0_N	AI	MIPI CSI1 lane 0 data (-)	CSI	
66	CSI1_LN0_P	AI	MIPI CSI1 lane 0 data (+)	CSI	
67	CSI1_LN1_N	AI	MIPI CSI1 lane 1 data (-)	CSI	
68	CSI1_LN1_P	AI	MIPI CSI1 lane 1 data (+)	CSI	
69	GND	-	Ground Pin	-	
70	CSI1_LN3_N	AI	MIPI CSI1 lane 3 data (-)	CSI	
71	CSI1_LN3_P	AI	MIPI CSI1 lane 3 data (+)	CSI	
72	CSI1_LN2_N	AI	MIPI CSI1 lane 2 data (-)	CSI	
73	CSI1_LN2_P	AI	MIPI CSI1 lane 2 data (+)	CSI	
74	CAM0_MCLK0	DO	Master clock of camera 0	P3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V
75	CAM_MCLK1	DO	Master clock of camera 1	P3	
76	GND	-	Ground Pin	-	
77	WIFI/BT_ANT	AIO	Wi-Fi/Bluetooth antenna interface	-	
78	GND	-	Ground Pin	-	
79	CAM0_RST_N	DO	Reset of camera 0	P3	
80	CAM0_PWDN	DO	Power down of camera 0	P3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V
81	CAM1_RST_N	DO	Reset of camera 1	P3	
82	CAM1_PWDN	DO	Power down of camera 1	P3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V
83	CCI_I2C_SCL0	OD	I2C clock of camera 0	P3	
84	CCI_I2C_SDA0	OD	I2C data of camera 0	P3	
85	GND	-	Ground Pin	-	
86	GND	-	Ground Pin	-	

87	MAIN_ANT	AIO	Main antenna interface	-	
88	GND	-	Ground Pin	-	
89	GND	-	Ground Pin	-	
90	GPIO_106	DIO	General-purpose input/output	P3	
91	SNSR_I2C_SCL	OD	I2C clock for external sensor	P3	
92	SNSR_I2C_SDA	OD	I2C data for external sensor	P3	
93	DBG_RXD	DI	Debug UART receive	P3	V_{IL}max = 0.63 V V_{IH}min = 1.17 V
94	DBG_TXD	DO	Debug UART transmit	P3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V
95	VOL_UP	DI	Volume up	P3	V_{IL}max = 0.63 V V_{IH}min = 1.17 V
96	VOL_DOWN	DI	Volume down	P3	
97	GPIO_31	DIO	General-purpose input/output	P3	
98	GPIO_107	DIO	General-purpose input/output	P3	
99	GPIO_32	DIO	General-purpose input/output	P3	
100	GPIO_49	DIO	General-purpose input/output	P3	
101	GPIO_104	DIO	General-purpose input/output	P3	
102	GPIO_105	DIO	General-purpose input/output	P3	
103	GPIO_103	DIO	General-purpose input/output	P3	
104	GPIO_102	DIO	General-purpose input/output	P3	
105	GPIO_99	DIO	General-purpose input/output	P3	
106	GPIO_48	DIO	General-purpose input/output	P3	
107	GPIO_35	DIO	General-purpose input/output	P3	
108	GPIO_33	DIO	General-purpose input/output	P3	
109	GPIO_34	DIO	General-purpose input/output	P3	

110	GPIO_36	DIO	General-purpose input/output	P3	
111	VREG_L15A_1P8	PO	1.8V output		Vnom = 1.8 V $I_O$max = 200 mA
112	GPIO_57	DIO	General-purpose input/output	P3	
113	GPIO_58	DIO	General-purpose input/output	P3	
114	PWRKEY	DI	Turn on/off the module	P3	
115	PM_GPIO_04	DIO	General-purpose input/output	P3	
116	GPIO_16	DIO	General-purpose input/output	P3	
117	GPIO_17	DIO	General-purpose input/output	P3	
118	GPIO_14	DIO	General-purpose input/output	P3	
119	GPIO_15	DIO	General-purpose input/output	P3	
120	GND	-	Ground Pin	-	
121	GNSS_ANT	AI	GNSS antenna interface	-	
122	GND	-	Ground Pin	-	
123	GPIO_60	DIO	General-purpose input/output	P3	
124	PM_GPIO_03	DIO	General-purpose input/output	P3	
125	VREG_L15A_1P8	PO	1.8V output	-	Vnom = 1.8 V $I_O$max = 300 mA
126	VRTC	PO	Power supply for RTC	-	$V_o$max = 3.2 V $V_I$min = 2.5 V $V_I$max = 3.2 V
127	PMU_GPIO_08	DIO	General-purpose input/output	P3	
128	ADC_IN	AI	General-purpose ADC interface	-	
129	VDD_2V8	PO	2.8V output	-	Vnom = 2.8 V $I_O$max = 500 mA
130	GND	-	Ground Pin	-	
131	DIV_ANT	AI	Diversity antenna interface	-	

132	GND	-	Ground Pin	-	
133	BAT_P	AI	Battery voltage detect (+)		
134	BAT_THERM	AI	Battery temperature detect		
135	GND	-	Ground Pin	-	
136	HEAD_R	AO	Headphone right channel output		
137	HEAD_GND	AO	Headphone reference ground (FM Antenna function integrated)		
138	HEAD_L	AO	Headphone left channel output		
139	HEAD_DET	AI	Headset hot-plug detect		
140	GND	-	Ground Pin	-	
141	USB_VBUS_IN	PIO	Charging power input. Power supply for OTG device. USB/adaptor insertion detection.		Vmax = 6.0 V Vmin = 4.0 V Vnom = 5.0 V
142	USB_VBUS_IN	PIO	Charging power input. Power supply for OTG device. USB/adaptor insertion detection.		Vmax = 6.0 V Vmin = 4.0 V Vnom = 5.0 V
143	GND	-	Ground Pin	-	
144	GND	-	Ground Pin	-	
145	VBATT	PI	Module input Voltage Pin	VB	Vmin = 3.5V Vnom =4V Vmax = 4.4 V
146	VBATT	PI	Module input Voltage Pin	VB	
147	MIC_BIAS1	PO	Bias voltage output for 1st microphone	-	Vomin = 1.6 V Vomax = 2.85 V
148	MIC3_P	AI	Microphone input for channel 3 (+)	-	
149	MIC3_N	AI	Microphone input for channel 3 (-)	-	
150	USB0_SS_TX1_P	AO	USB 3.1 channel 2 superspeed transmit (+)		
151	USB0_SS_TX1_N	AO	USB 3.1 channel 2 superspeed transmit (-)		
152	USB0_SS_RX1_P	AI	USB 3.1 channel 2 superspeed receive (+)		
153	UART1_RXD	DI	UART1 receive	P3	

154	UART1_TXD	DO	UART1 transmit	P3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V
155	MIC_BIAS3	PO	Bias voltage output for 3rd microphone	-	Vnom = 1.8 V
156	VREG_L17A_3P0	PO	3.0V output		Vnom = 3.0 V $I_O$max = 192 mA
157	CSI0_CLK_N	AI	MIPI CSI0 clock (-)	CSI	
158	CSI0_LN0_N	AI	MIPI CSI0 lane 0 data (-)	CSI	
159	CSI0_LN1_N	AI	MIPI CSI0 lane 1 data (-)	CSI	
160	CSI0_LN2_N	AI	MIPI CSI0 lane 2 data (-)	CSI	
161	CSI0_LN3_N	AI	MIPI CSI0 lane 3 data (-)	CSI	
162	GND	-	Ground Pin	-	
163	CAM2_PWDN	DO	Power down of camera 2	P3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V
164	CAM2_RST_N	DO	Reset of camera 2	P3	
165	CAM_MCLK2	DO	Master clock of camera 2	P3	
166	CCI_I2C_SCL1	OD	I2C clock of camera 1	P3	
167	LPI_GPIO_21	DIO	General-purpose input/output		
168	LPI_GPIO_22	DIO	General-purpose input/output		
169	LPI_GPIO_25	DIO	General-purpose input/output		
170	LPI_GPIO_26	DIO	General-purpose input/output		
171	GND	-	Ground Pin	-	
172	GND	-	Ground Pin	-	
173	RESERVED	-	-	P3	
174	RESERVED	-	-		
175	RESERVED	-	-		
176	GND	-	Ground Pin	-	
177	GPIO_112	DIO	General-purpose input/output	P3	
178	RESERVED	-	-		
179	RESERVED	-	-		
180	FLASH_LED1	AO	Flash/torch driver output		$I_O$max = 1 A

181	NFC_RFCLK3	DO	NFC clock	P3	
182	GPIO_86	DIO	General-purpose input/output	P3	
183	BAT_M	AI	Battery voltage detect (-)		
184	VPH_PWR	PO	Power supply for peripherals		Vmin = 3.5 V Vnom = 3.8 V Vmax = 4.4 V
185	BAT_ID	AI	Battery type detect		V_{I}min = 0 V V_{I}max = 1.875 V
186	PWRKEY_ALT	DI	Cable power-on; Initiate power-on when grounded		
187	GND	-	Ground Pin	-	
188	GND	-	Ground Pin	-	
189	GND	-	Ground Pin	-	
190	GND	-	Ground Pin	-	
191	GND	-	Ground Pin		
192	USB0_SS_RX1_N	AI	USB 3.1 channel 2 superspeed receive (-)		
193	RESERVED	-	-		
194	EXT_GPS_LNA_EN0	DI	GNSS LNA enable control		
195	CHG_LED_SINK	DO	Indicate the module's charging status		I_{I}max = 5 mA
196	CSI0_CLK_P	AI	MIPI CSI0 clock (+)	CSI	
197	CSI0_LN0_P	AI	MIPI CSI0 lane 0 data (+)	CSI	
198	CSI0_LN1_P	AI	MIPI CSI0 lane 1 data (+)	CSI	
199	CSI0_LN2_P	AI	MIPI CSI0 lane 2 data (+)	CSI	
200	CSI0_LN3_P	AI	MIPI CSI0 lane 3 data (+)	CSI	
201	PM_GPIO_07	DIO	General-purpose input/output	P3	
202	GND	-	Ground Pin	-	
203	GND	-	Ground Pin	-	
204	GND	-	Ground Pin	-	
205	CCI_I2C_SDA1	OD	I2C data of camera 1	P3	
206	GND	-	Ground Pin	-	
207	GND	-	Ground Pin	-	
208	GND	-	Ground Pin	-	

209	GND	-	Ground Pin	-	
210	GND	-	Ground Pin	-	
211	GND	-	Ground Pin	-	
212	GND	-	Ground Pin	-	
213	GND	-	Ground Pin	-	
214	GND	-	Ground Pin	-	
215	GND	-	Ground Pin	-	
216	GND	-	Ground Pin	-	
217	GND	-	Ground Pin	-	
218	GND	-	Ground Pin	-	
219	GND	-	Ground Pin	-	
220	GND	-	Ground Pin	-	
221	GND	-	Ground Pin	-	
222	GND	-	Ground Pin	-	
223	GND	-	Ground Pin	-	
224	GND	-	Ground Pin	-	
225	RESET_IN/VOL-	DI	Reset the module	P3	
226	GND	-	Ground Pin	-	
227	GND	-	Ground Pin	-	
228	GND	-	Ground Pin	-	
229	GND	-	Ground Pin	-	
230	GND	-	Ground Pin	-	
231	GND	-	Ground Pin	-	
232	RESERVED	-	-		
233	GND	-	Ground Pin	-	
234	GND	-	Ground Pin	-	
235	GND	-	Ground Pin	-	
236	GND	-	Ground Pin	-	
237	GND	-	Ground Pin	-	
238	GND	-	Ground Pin	-	
239	GPIO_101	DIO	General-purpose IO	P3	
240	GND	-	Ground Pin	-	

241	GND	-	Ground Pin	-	
242	RESERVED	-	-		
243	GND	-	Ground Pin	-	
244	GND	-	Ground Pin	-	
245	GND	-	Ground Pin	-	
246	USB0_CC2	AI	USB Type-C detect 2		
247	GND	-	Ground Pin	-	
248	GND	-	Ground Pin	-	
249	USB0_CC1	AI	USB Type-C detect 1		
250	GND	-	Ground Pin	-	
251	GND	-	Ground Pin	-	
252	USB0_SS_RX0_P	AI	USB 3.1 channel 1 superspeed receive (+)		
253	USB0_SS_TX0_N	AO	USB 3.1 channel 1 superspeed transmit (-)		
254	USB0_SS_TX0_P	AO	USB 3.1 channel 1 superspeed transmit (+)		
255	GND	-	Ground Pin	-	
256	GND	-	Ground Pin	-	
257	RESERVED	-	-		
258	GND	-	Ground Pin	-	
259	GND	-	Ground Pin	-	
260	RESERVED	-	-		
261	GND	-	Ground Pin	-	
262	RESERVED	-	-		
263	RESERVED	-	-		
264	GPIO_100	DIO	General-purpose IO	P3	
265	GPIO_98	DIO	General-purpose input/output	P3	
266	GND	-	Ground Pin	-	
267	GPIO_111	DIO	General-purpose input/output	P3	
268	GND	-	Ground Pin	-	
269	GND	-	Ground Pin	-	

270	USB0_SS_RX0_N	AI	USB 3.1 channel 1 superspeed receive (-)		
271	GND	-	Ground Pin	-	
272	GND	-	Ground Pin	-	
273	GND	-	Ground Pin	-	
274	GND	-	Ground Pin	-	

NOTE

- *The module typically has an IO port level of 1.8V (in addition to the SIM, the SIM card port level supports 1.8V/3V).*
- *This module defines the RESERVED pin as a reserved pin. It is recommended to be suspended and must not be used*

3.3 Power Interfaces

The CQS29X module provides three VBATT pins to connect to the external power supply. The module is to be operated between the voltages of 3.5 V to 4.4 V and the recommended operating voltage is 4.2V. Ensure the source is capable of providing a sufficient current. If the power supply is not sufficient or unstable, the module is under the risk of improper functionality or even module turn OFF. Therefore, ensure the voltages are kept within the specified ranges and that there is minimal or no noise within the trace. A surge/transient suppressor near to the external source is advised.

3.3.1 Power supply design

Ensure the source is capable of providing a current rating of at least 3A, so design accordingly. An LDO is advised if the voltage difference between the supply and the module is not much.

A buck converter is advised if the voltage difference between the supply and the module is quite significant

A power design of a 12V external supply to the module via a Buck converter that outputs to 4.1V/6A is given below

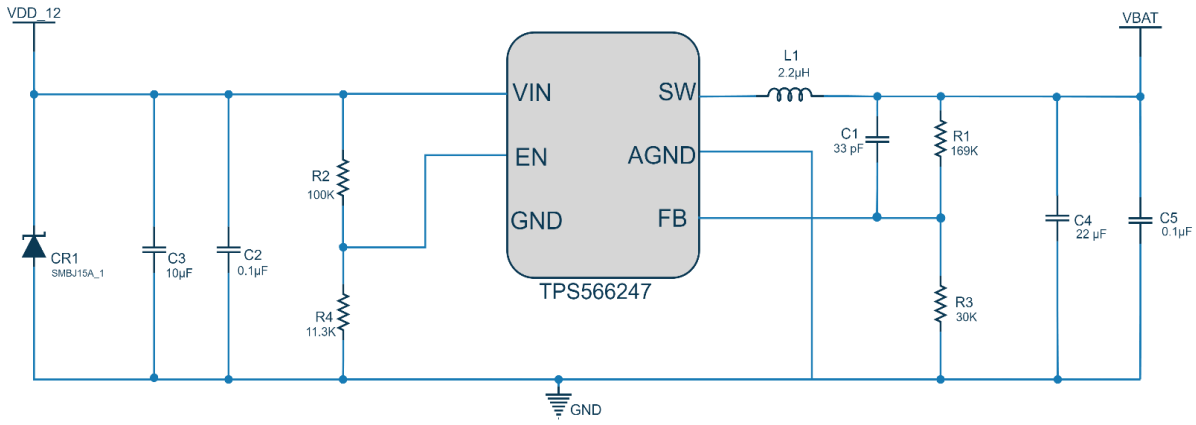


Figure 3 Power supply reference circuit

3.3.2 Power reference circuit

Ensure the voltages are kept within the specified ranges and that there is minimal or no noise within the trace. Advised to keep the VBATT trace width within 3mm. A surge/transient suppressor near to the external source is advised.

The advised VBATT circuit design is given below.

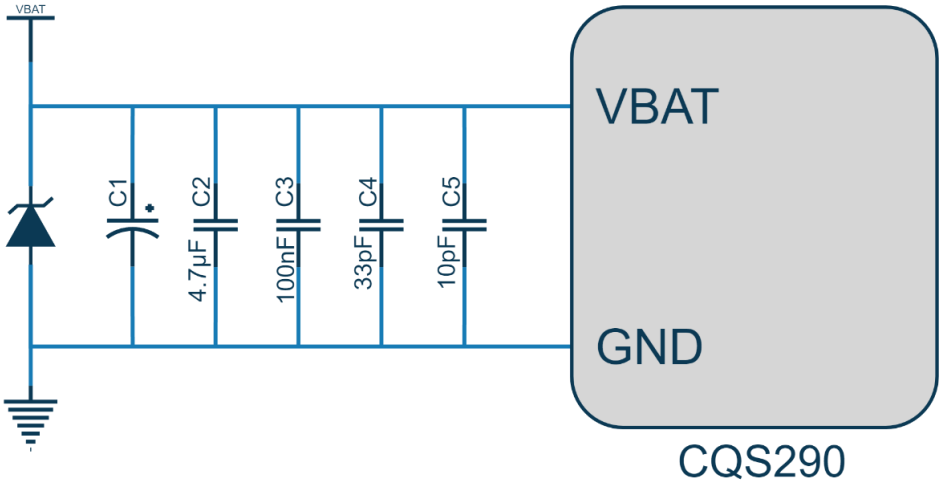


Figure 4 Power reference circuit

3.4 Switching Machine Reset Mode

3.4.1 Turn ON Control

The module, provided that a continued stable-power supply is given to the VBATT, is powered ON by pulling down/grounding the PWRKEY pin for 2000ms.

Table 7 Power Key definition

Pin No.	Pin name	I/O	Description
114	PWRKEY	DI	Active Low pin
186	PWRKEY_ALT	DI	Cable power-on; Initiate power-on when grounded

NOTE

- *For auto bootup PWRKEY_ALT (Pin 186) can be hardwired to GND*

The reference schematic for Power ON using a switch is given below:

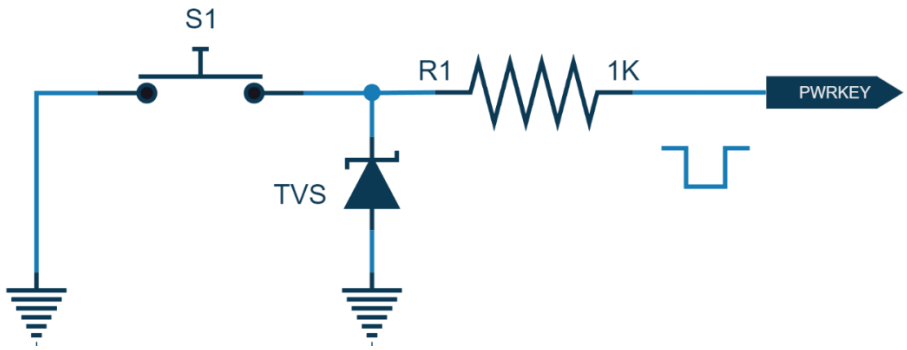


Figure 5 Power ON using a switch

The reference schematic for Power ON using an inverting transistor is given below:

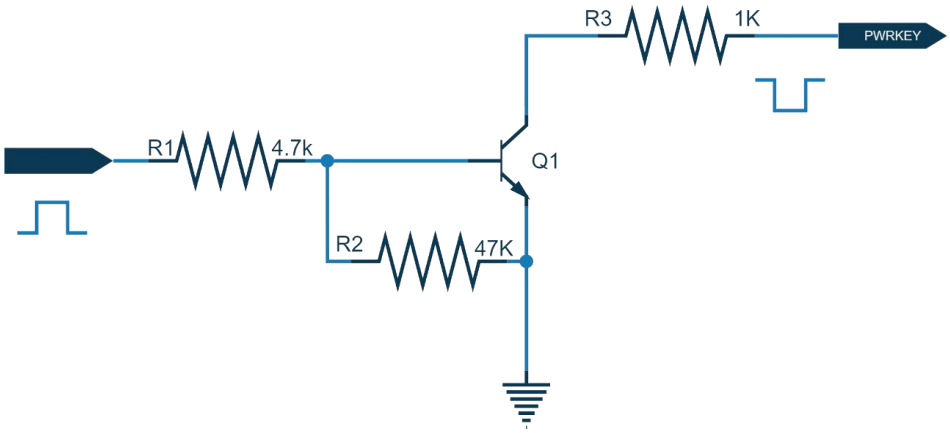


Figure 6 Power ON using an inverting transistor

3.4.2 Reset Control

The module is Reset by pulling down/grounding the RESET_IN pin (Pin 225). Pull the pin up after successful Reset.

Table 8 RESET pin definition

Pin No.	Pin name	I/O	Voltage Definition	Description
225	RESET_IN	DI	P3	Module Reset Control

The reference schematic for Reset using a switch is given below:

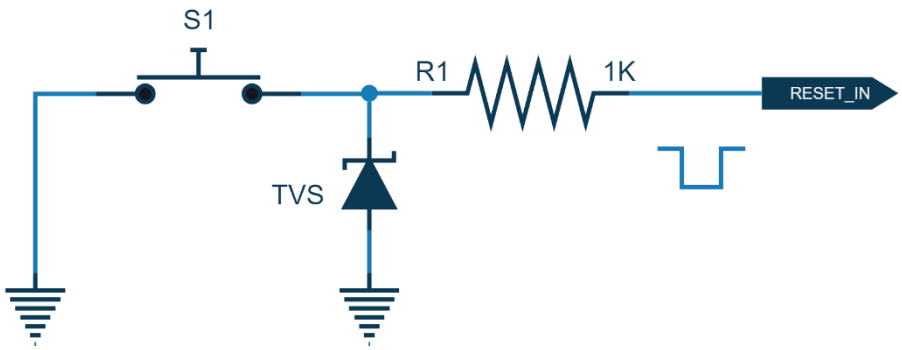


Figure 7 Reset using switch

The reference schematic for Reset using an inverting transistor is given below:

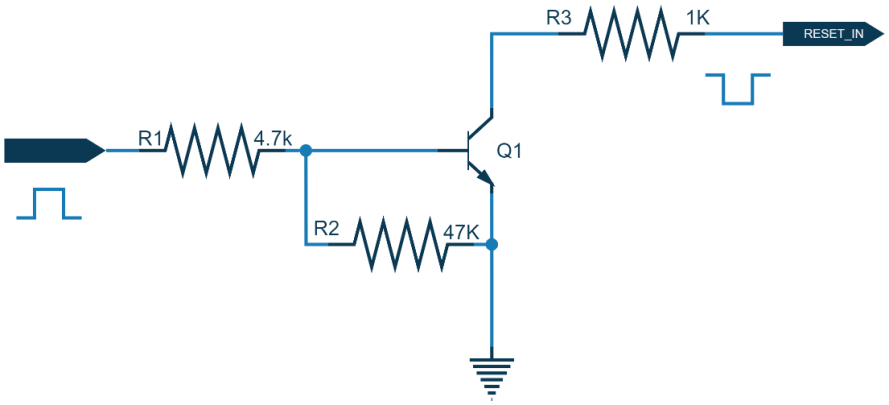


Figure 8 Reset using inverting transistor

3.4.3 USB Boot

FORCED_USB_BOOT (Pin 46) is an emergency download interface. You can force the module to enter emergency. download mode by pulling it up to VREG_L15A_1P8 pin (Pin 111) during power-on. This is an emergency option when failures such as abnormal start-up or running occur.

3.5 USB Interface

The module supports USB 2.0 and USB 3.1 standard of High speeds up to 480Mbps and Full speed up to 12Mbps. It complies with USB 2.0 standard by providing a high-speed differential channel of USB_DP and USB_DM pins (Pin 14 and 13).

Table 9 USB2.0 Interface pin definition

Pin No.	Pin name	I/O	Description
141, 142	USB_VBUS_IN	PI, PO	USB Voltage Bus
14	USB_DP	AIO	USB differential signal +
13	USB_DM	AIO	USB differential signal -

Table 10 USB 3.1 interface pin definition

Pin No.	Pin name	I/O	Description
141, 142	USB_VBUS_IN	PI, PO	USB Voltage Bus
249	USB0_CC1	AI	CC1
246	USB0_CC2	AI	CC2
252	USB0_SS_RX0_P	AI	USB 3.1 channel 1 super-speed receive (+)
270	USB0_SS_RX0_N	AI	USB 3.1 channel 1 super-speed receive (-)
254	USB0_SS_TX0_P	AO	USB 3.1 channel 1 super-speed transmit (+)
253	USB0_SS_TX0_N	AO	USB 3.1 channel 1 super-speed transmit (-)
152	USB0_SS_RX1_P	AI	USB 3.1 channel 2 super-speed receive (+)
192	USB0_SS_RX1_N	AI	USB 3.1 channel 2 super-speed receive (-)
150	USB0_SS_TX1_P	AO	USB 3.1 channel 2 super-speed transmit (-)
151	USB0_SS_TX1_N	AO	USB 3.1 channel 2 super-speed transmit (-)

The USB reference circuit diagram in USB 2.0 mode is given below:

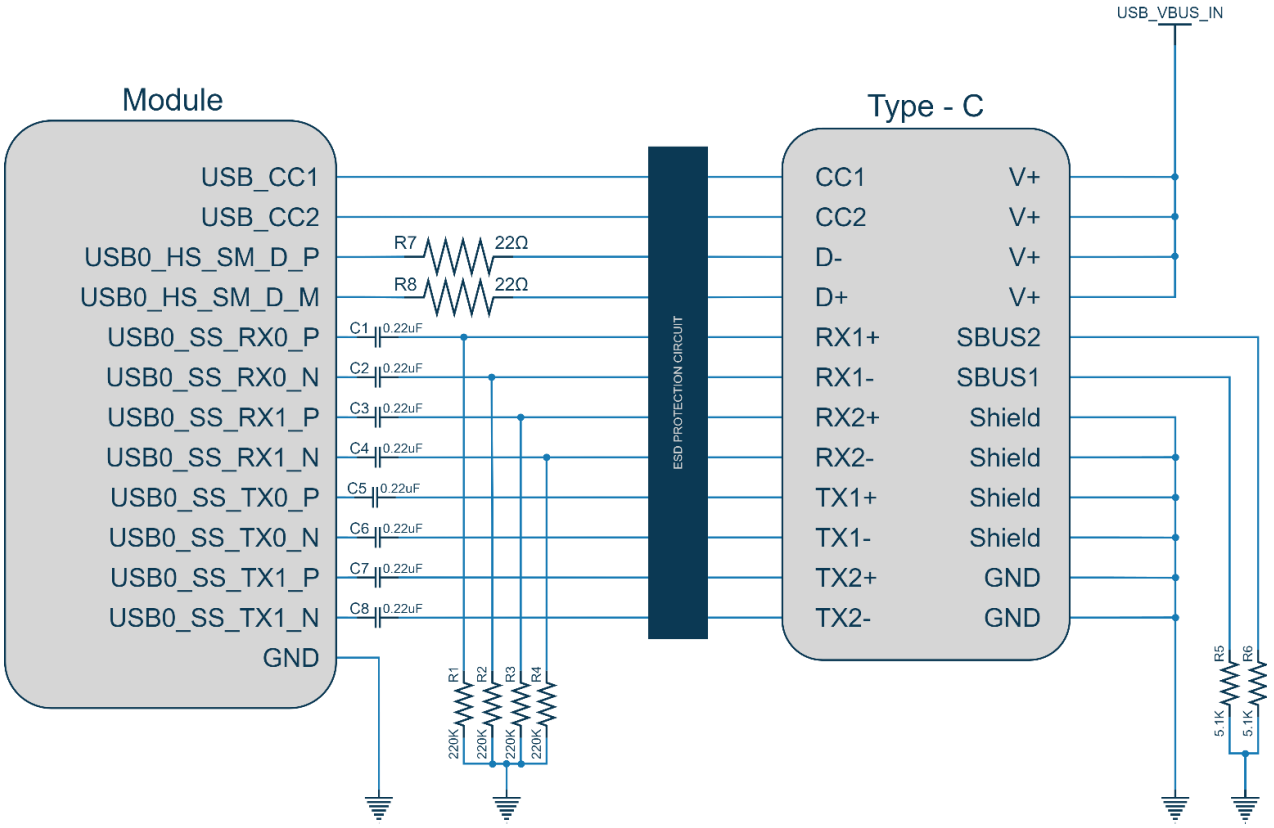


Figure 9 USB 3.1 Interface

NOTE

- *USB_VBUS and CC pins must be connected for USB enumeration*

3.6 UART Interface

CQS292 provide 3 UART interfaces

- ✓ UART0: 4 wire UART interface, supports RTS and CTS hardware flow control.
- ✓ UART4: 2 wire debug UART interface, dedicated for debugging.
- ✓ UART1: 2 wire UART interface

NOTE

- *Please look into Alternate function table if additional pins need to be configured as UART.*

3.6.1 UART1 Serial Port

2-wire UART Interface meant for external/peripheral Interfacing

Table 11 UART1 Serial port application

Pin No.	Pin name	I/O	Description	Parameter	Level value (V)		
					min	typical	max
153	UART1_RXD	DI	Data reception	VOH	P - 0.45	-	P
				VOL	0	-	0.45
154	UART1_TXD	DO	Data transmission	VIH	0.65 × P	-	P + 0.3 V
				VIL	-0.3 V		0.35 × P

3.6.2 UART4 Serial Port

This is the Debug UART of the module meant for debugging purposes

The pins are defined as follows：

Table 12 UART Port serial port definition

Pin No.	Pin name	I/O	Description	Parameter	Level value (V)		
					min	typical	max
93	DBG_RXD	DI	Data reception	VOH	P - 0.45	-	P
				VOL	0	-	0.45
94	DBG_TXD	DO	Data transmission	VIH	0.65 × P	-	P + 0.3 V
				VIL	-0.3 V		0.35 × P

3.6.3 UART0 Serial Port

4-wire UART Interface with CTS and RTS Hardware Flow Control for peripheral Interfacing

Table 13 UART5 serial port pin definition

Pin No.	Pin name	I/O	Description	Parameter	Level value (V)		
					min	typical	max
36	UART0_CTS	DI					
37	UART0_RTS	DO					
34	UART0_TXD	DI	Data transmission	VOH	P - 0.45	-	P
				VOL	0	-	0.45
35	UART0_RXD	DO	Data reception	VIH	0.65 × P	-	P + 0.3 V
				VIL	-0.3 V		0.35 × P

3.6.4 Serial Port Application Circuit

The serial level is 1.8V.

To use a 2-wire serial port, User may refer to the following serial port design:

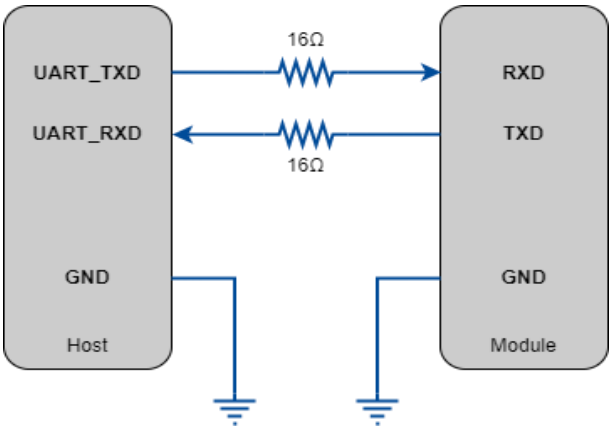


Figure 10 UART Serial port design

The serial port of the module is TTL 1.8V level. If the serial port needs to be connected to the MCU of 3.3V level, it is necessary to add a level conversion chip externally to achieve level matching. Use an external 1.8V power source for VCCA. For the chip connection method, refer to the following circuit:

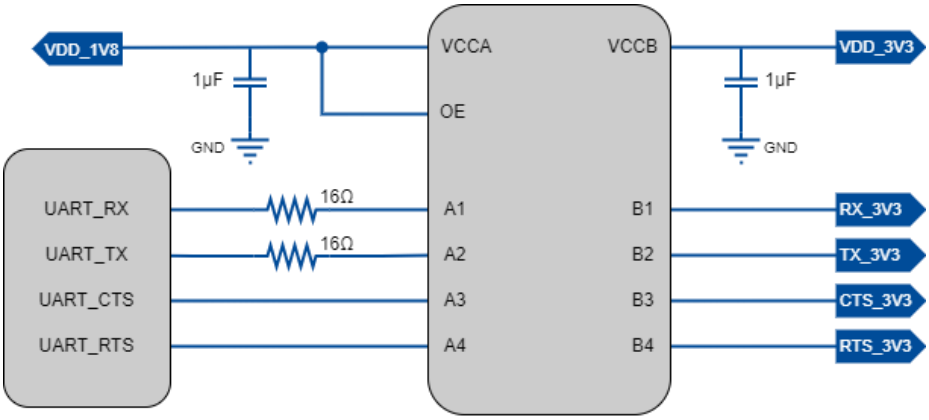


Figure 11 Level conversion technique

3.7 SPI interface

The module has a single SPI Interface and functions only in the Master mode.

Table 14 SPI interface pin definition

Pin No.	Pin name	I/O	Description
154	SPI_SCLK	DO	Clock
82	SPI_MOSI	DI	Master output slave input
80	SPI_MISO	DI	Master input slave output
153	SPI_CS	DO	Slave select

NOTE

- *Please look into Alternate function table if additional pins need to be configured as SPI.*

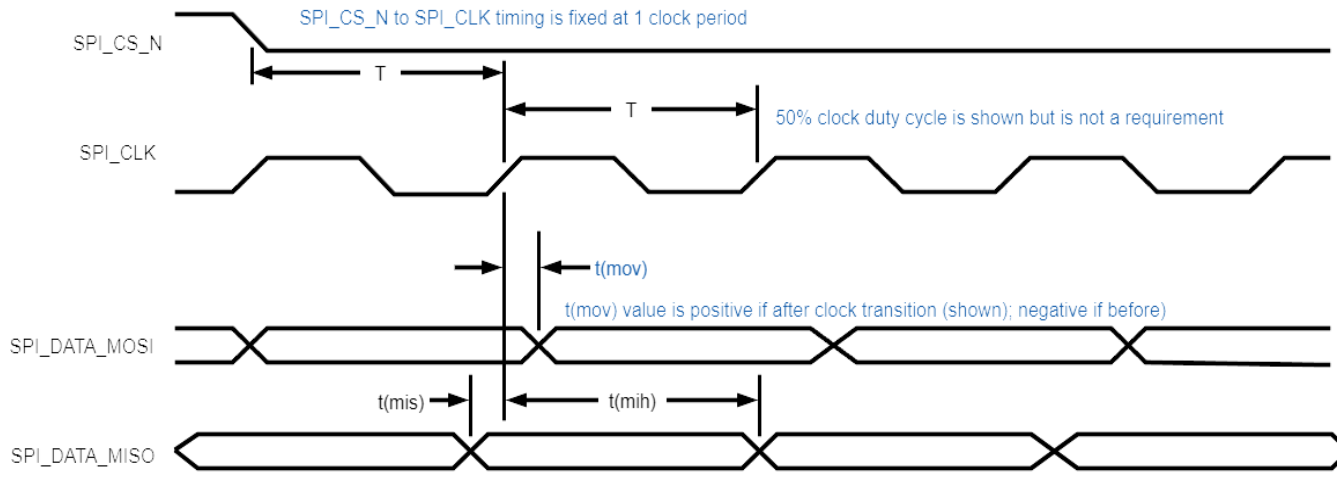


Figure 12: SPI Timing diagram

3.8 I2C/I3C Interface

The module supports four I2C interfaces. All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8V. SENSOR_I2C only supports sensors of ADSP architecture. CAM0_I2C and CAM1_I2C signals are controlled by Linux kernel code and support connection with video-output-related devices.

The I3C Interface complies with the version 1.0 standard. Works in both Master and Slave mode.

Table 15 I2C Pin definition

Pin No.	Pin name	I/O	Description	Parameter	Level value (V)		
					min	typical	max
91	SNSR_I2C_SCL	OD	I2C bus data input and output	VOH	P - 0.45	-	P
				VOL	0	-	0.45
				VIH	0.65 × P	-	P + 0.3 V
				VIL	-0.3 V		0.35 × P
92	SNSR_I2C_SDA	OD	I2C bus clock output	VOH	P - 0.45	-	P
				VOL	0	-	0.45
47	TS_I2C_SCL	OD		VOH	P - 0.45	-	P

			I2C bus clock output	VOL	0	-	0.45
				VIH	0.65 × P	-	P + 0.3 V
				VIL	-0.3 V		0.35 × P
48	TS_I2C_SDA	OD	I2C bus data input and output	VOH	P - 0.45	-	P
				VOL	0	-	0.45
83	CCI_I2C_SCL0	OD	Camera I2C bus clock output	VIH	0.65 × P	-	P + 0.3 V
				VIL	-0.3 V		0.35 × P
84	CCI_I2C_SDA0	OD	Camera I2C bus data input and output	VOH	P - 0.45	-	P
				VOL	0	-	0.45
				VIH	0.65 × P	-	P + 0.3 V
				VIL	-0.3 V		0.35 × P
166	CCI_I2C_SCL1	DO	Camera I2C bus clock output	VIH	0.65 × P	-	P + 0.3 V
				VIL	-0.3 V		0.35 × P
205	CCI_I2C_SDA1	OD	Camera I2C bus data input and output	VOH	P - 0.45	-	P
				VOL	0	-	0.45
				VIH	0.65 × P	-	P + 0.3 V
				VIL	-0.3 V		0.35 × P

NOTE

- *Please look into Alternate function table if additional pins need to be configured as I2C.*

The I2C/I3C reference circuit is connected as follows:

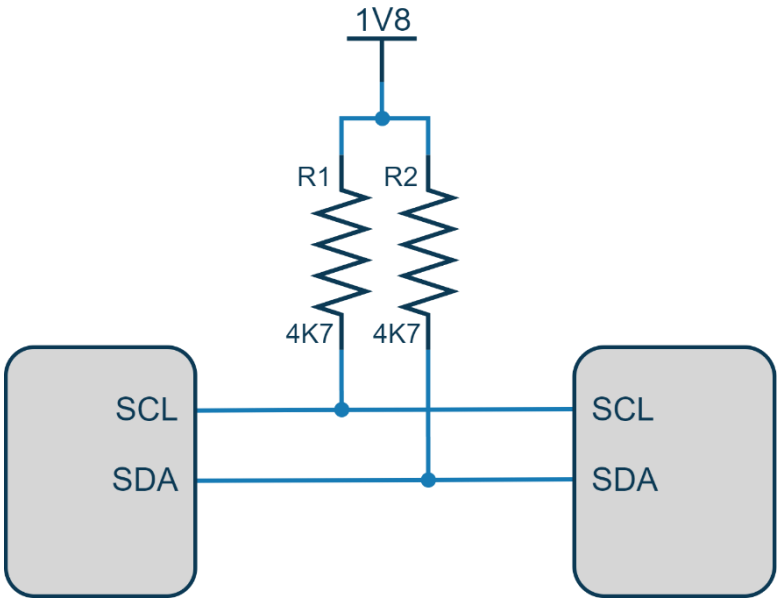


Figure 13 I2C Reference Circuit

3.9 SDC Interface

The module has a single SDC 4-bit interface which is SD 3.0 compliant. It supports hot swap functionality and has dual voltage support.

Table 16 SDC Interface Pin definitions

Pin No.	Pin name	I/O	Description
45	SD_CARD_DET_N	DI	Detect SD Card
43	SDC2_DATA_2	DIO	SD card Data 2
44	SDC2_DATA_3	DIO	SD card Data 3
40	SDC2_CMD	DIO	SD Command Pin
39	SDC2_CLK	DO	SD Clock Pin
41	SDC2_DATA_0	DIO	SD card Data 1
42	SDC2_DATA_1	DIO	SD card Data 0
38	VREG_L21A_2P96	PO	SD card power supply
32	VREG_L4A_2P96	PO	1.8/2.95 V output power for SD card pull-up circuits

The SDC reference circuit is connected as follows:

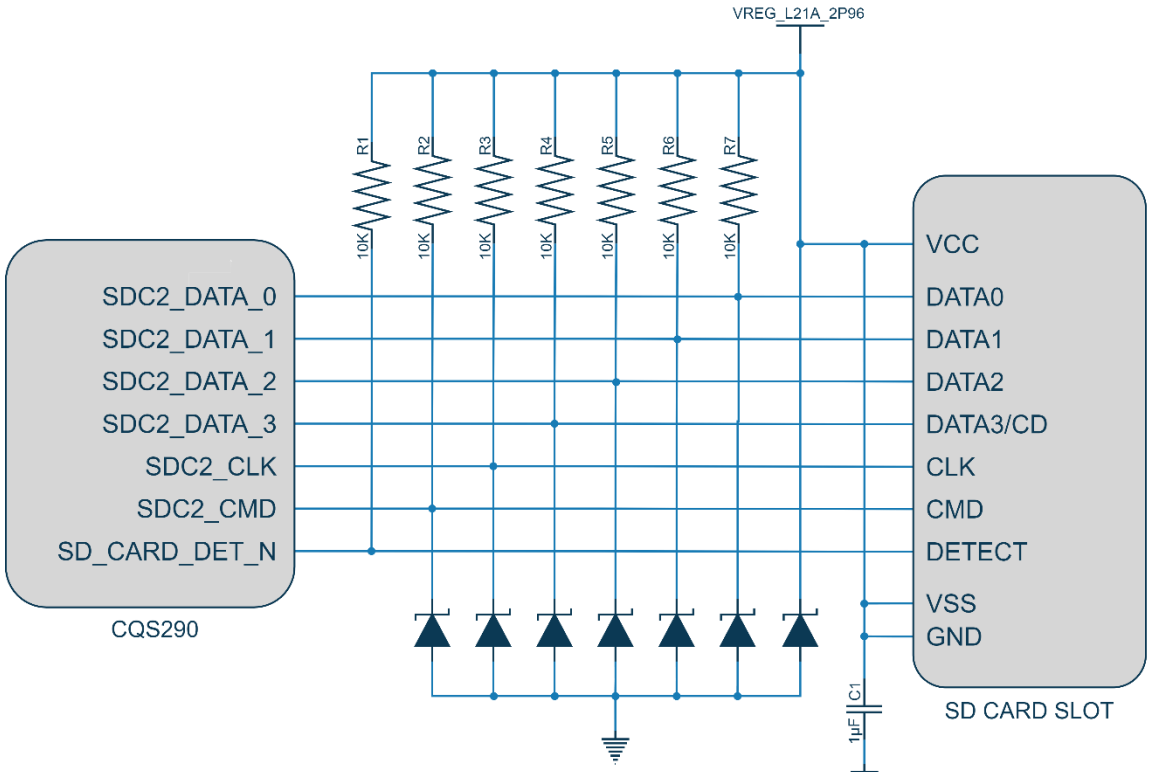


Figure 14 SDC Reference Circuit

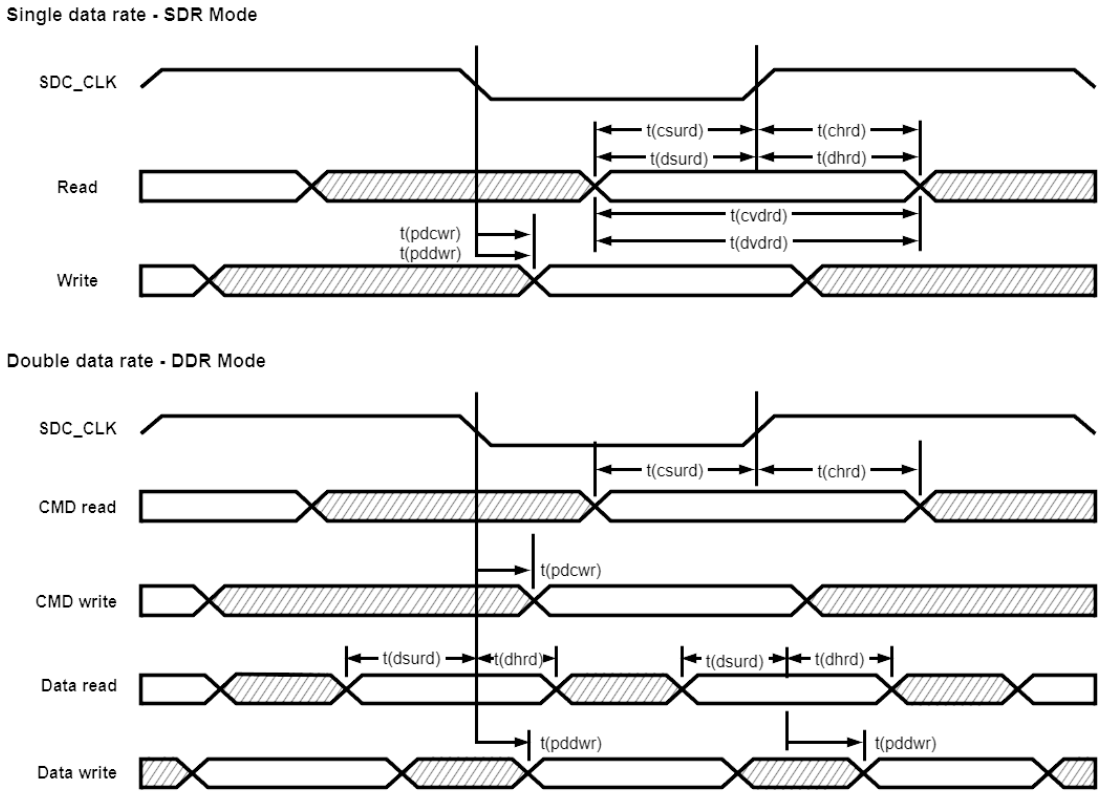


Figure 15: SD Timing Diagram 1

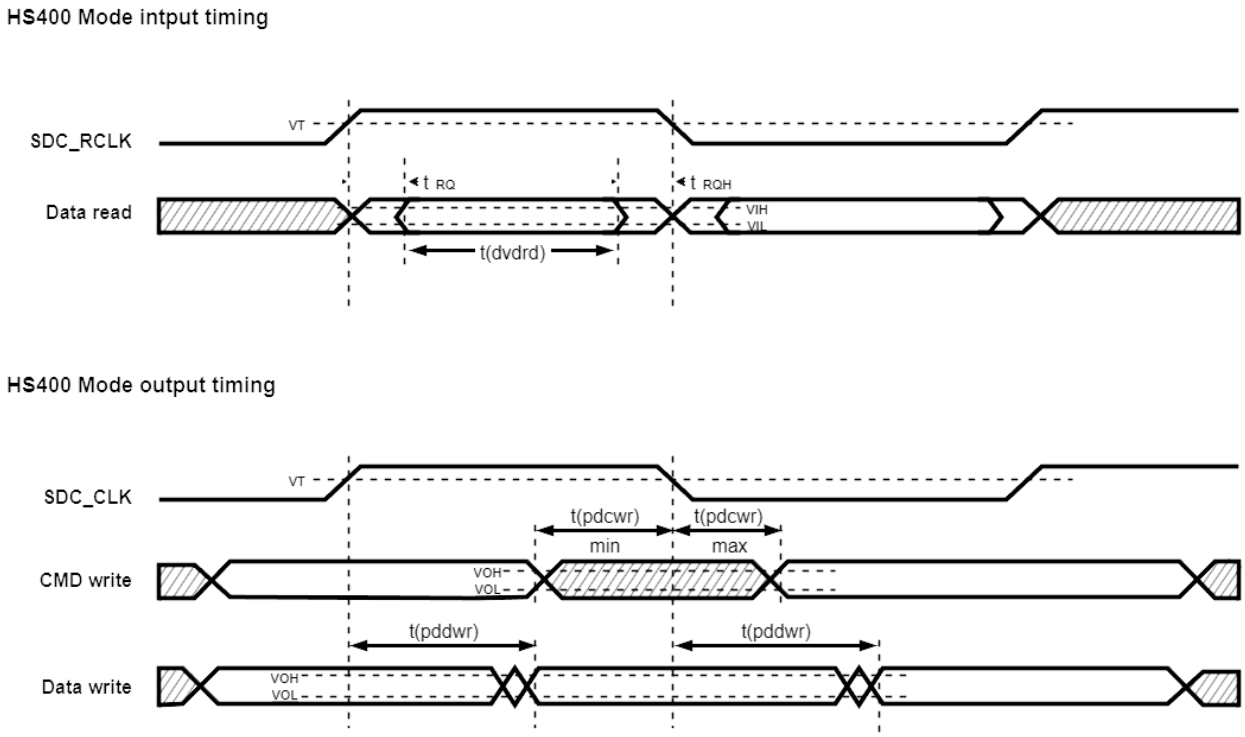


Figure 16: SD Timing Diagram 2

3.10 USIM Interface

The module has a single external SIM Interface. DSDS support enabled by default and supports dual voltages of 1.8V and 2.95V. The interface has a hot-plug functionality via its UIM1_PRESENT pin (Pin 22). If the hot plug is not needed, leave the pin open.

Table 17 Sim card signal definition

Pin No.	Pin name	I/O	Description
26	USIM_VDD	PO	(U)SIM1 card power supply
25	USIM1_DATA	DIO	USIM card data
24	UIM1_CLK	DO	USIM card clock
23	UIM1_RESET	DO	USIM card reset
22	UIM1_PRESENT	DI	USIM card detection

3.10.1 USIM Card Reference Circuit

The CQS29X module does not come with a USIM card slot. The User needs to design a USIM card slot on their own interface board.

The USIM card interface reference circuit is as follows:

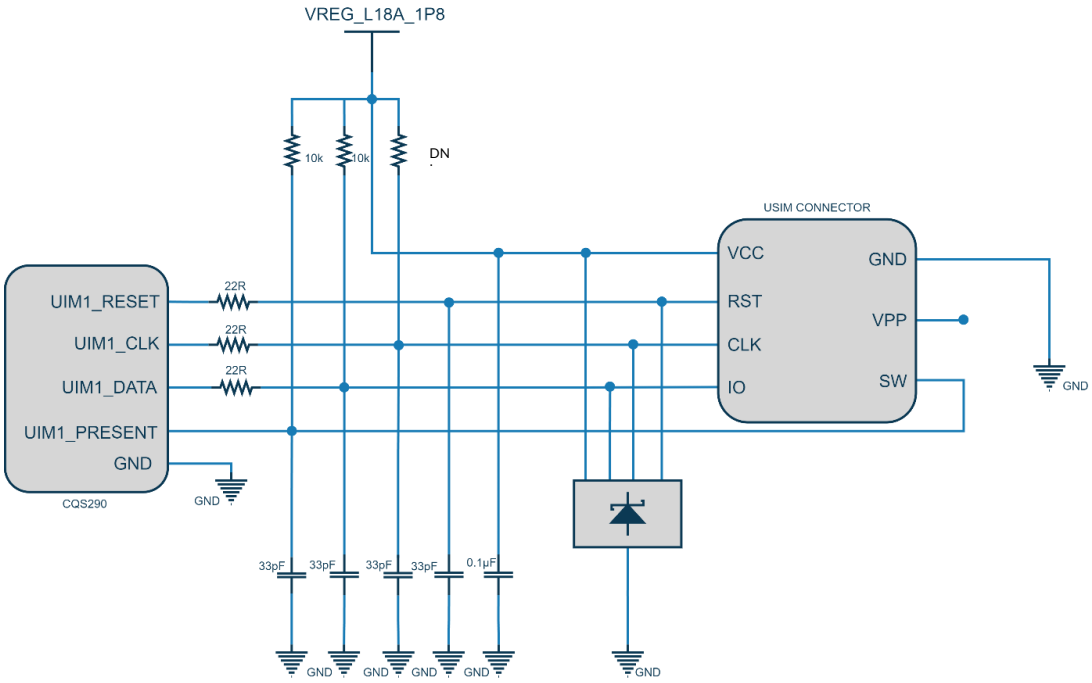


Figure 17 USIM design circuit diagram

NOTE

- *The USIM interface cable is recommended to use ONSEMI's SMF15C device for ESD protection. The peripheral circuit components should be placed close to the card holder. The SIM card holder is close to the module layout.*
- *The USIM card circuit is susceptible to radio frequency interference and does not recognize or drop the card. Therefore, the card slot should be placed as far as possible from the RF radiation of the antenna. The card trace should be as far away as possible from the RF, power supply and high-speed signal lines.*
- *The ground of the USIM deck and the ground of the module should maintain good connectivity.*

3.11 Motor Drive Interface

The module is capable of driving a vibrator motor via its VIB_DRV pin (Pin 28).

Ensure that once the motor stops working and the module pin is disconnected, a proper discharge circuit is present to prevent any possible damage that may arise.

The pin definition of the motor drive interface is listed below.

Table 18 Motor drive interface pin definitions

Pin No.	Pin name	I/O	Description
28	VIB_DRV	PO	Vibration motor driver output control

The reference circuit is shown below.

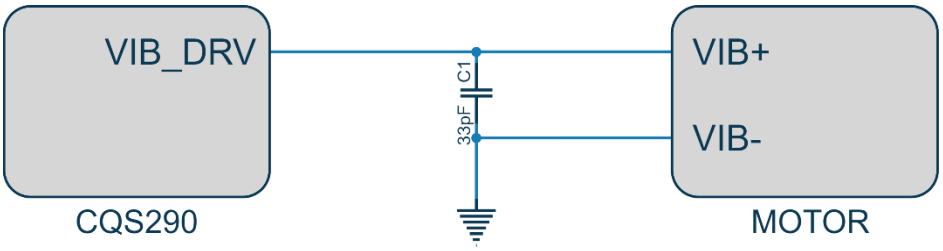


Figure 18 Motor controller reference circuit

3.12 LED Interfaces

The module by default has three LED Interfaces

Table 19 LED Interface Pin definitions

Pin No.	Pin name	I/O	Description
180	FLASH_LED1	AO	Flash/torch driver output
195	CHG_LED_SINK	DO	Indicate the module's charging status

3.13 General Purpose GPIO Interface

The module has thirty-three configurable GPIOs and has a power domain of 1.8V

Table 20 General GPIO Pin definitions

Pin No.	Pin Name	I/O	Functional description
33	GPIO_28	DIO	General-purpose input/output
90	GPIO_106	DIO	General-purpose input/output
97	GPIO_31	DIO	General-purpose input/output

98	GPIO_107	DIO	General-purpose input/output
99	GPIO_32	DIO	General-purpose input/output
100	GPIO_49	DIO	General-purpose input/output
101	GPIO_104	DIO	General-purpose input/output
102	GPIO_105	DIO	General-purpose input/output
103	GPIO_103	DIO	General-purpose input/output
104	GPIO_102	DIO	General-purpose input/output
105	GPIO_99	DIO	General-purpose input/output
106	GPIO_48	DIO	General-purpose input/output
107	GPIO_35	DIO	General-purpose input/output
108	GPIO_33	DIO	General-purpose input/output
109	GPIO_34	DIO	General-purpose input/output
110	GPIO_36	DIO	General-purpose input/output
112	GPIO_57	DIO	General-purpose input/output
113	GPIO_58	DIO	General-purpose input/output
116	GPIO_16	DIO	General-purpose input/output
117	GPIO_17	DIO	General-purpose input/output
118	GPIO_14	DIO	General-purpose input/output
119	GPIO_15	DIO	General-purpose input/output
123	GPIO_60	DIO	General-purpose input/output
173	GPIO_45	DIO	General-purpose input/output
177	GPIO_112	DIO	General-purpose input/output

182	GPIO_86	DIO	General-purpose input/output
239	GPIO_101	DIO	General-purpose input/output
264	GPIO_100	DIO	General-purpose input/output
265	GPIO_98	DIO	General-purpose input/output
267	GPIO_111	DIO	General-purpose input/output
115	PM_GPIO_04	DIO	General-purpose input/output
124	PM_GPIO_03	DIO	General-purpose input/output
127	PMU_GPIO_08	DIO	General-purpose input/output
201	PM_GPIO_07	DIO	General-purpose input/output
167	LPI_GPIO_21	DIO	General-purpose input/output
168	LPI_GPIO_22	DIO	General-purpose input/output
169	LPI_GPIO_25	DIO	General-purpose input/output
170	LPI_GPIO_26	DIO	General-purpose input/output

NOTE

- *Please look into Alternate function table if additional pins need to be configured as GPIO.*

3.14 ADC

The module has one Analog-to-Digital Converter Interface.

Table 21 ADC Convertor Pin definitions

Pin No.	Pin name	I/O	Description
128	ADC_IN	AI	General-purpose ADC interface

3.15 LCM Interface

The module provides one LCM Interface via the MIPI-DSI Standard. It is a 4-bit D-PHY v1.2 supported DSI Lane at 1.5 Gbps per lane architecture with split link support. It provides an HD+ Display output of 1680 x 720 resolution at 60FPS.

It is advised to add common mode filters in series to the differential lines closer to the LCM Connector to avoid Electro-magnetic interferences.

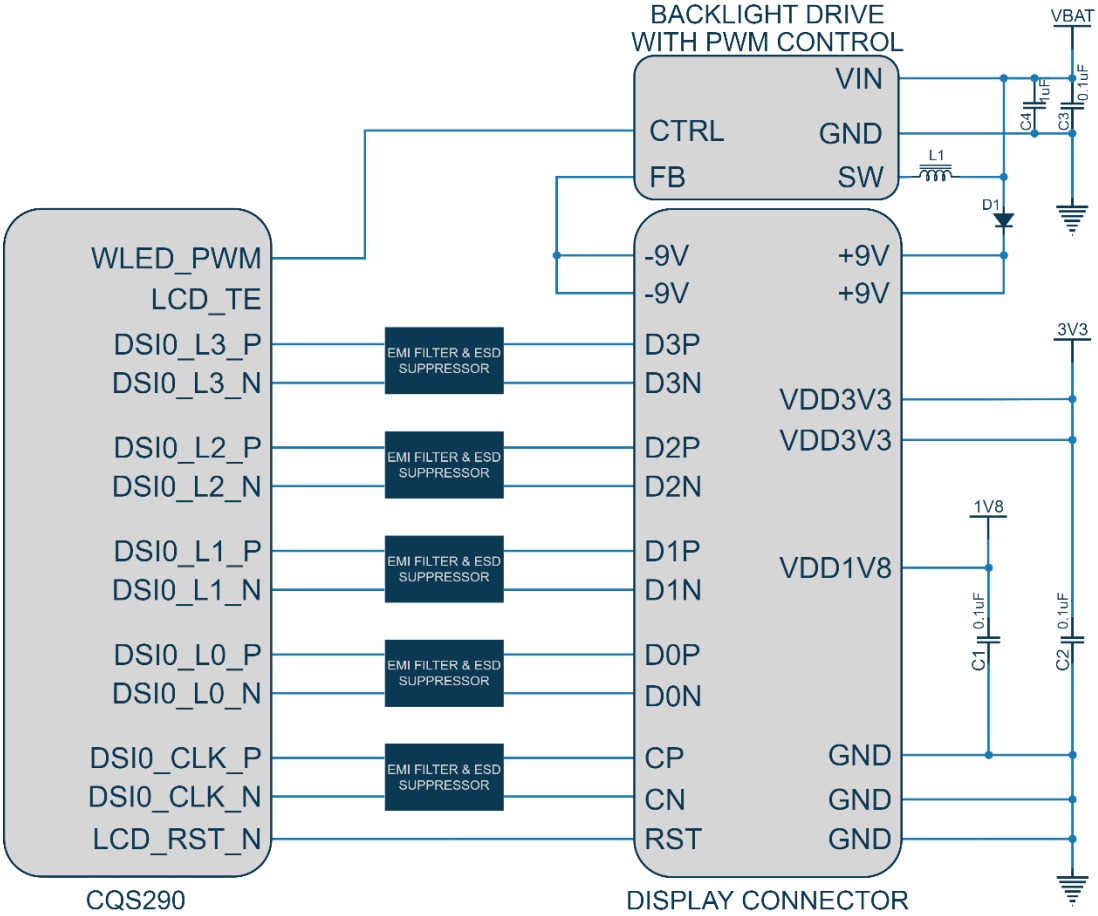


Figure 19 MIPI-DSI interface

Table 22 LCM(DSI) Interface Pin definitions

Pin No.	Signal name	I/O	Description
52	DSI0_CLK_N	AO	LCD MIPI clock (-)
53	DSI0_CLK_P	AO	LCD MIPI clock (+)
54	DSI0_LN0_N	AO	LCD MIPI lane 0 data (-)
55	DSI0_L0_P	AO	LCD MIPI lane 0 data (+)

56	DSI0_L1_N	AO	LCD MIPI lane 1 data (-)
57	DSI0_L1_P	AO	LCD MIPI lane 1 data (+)
58	DSI0_L2_N	AO	LCD MIPI lane 2 data (-)
59	DSI0_L2_P	AO	LCD MIPI lane 2 data (+)
60	DSI0_L3_N	AO	LCD MIPI lane 3 data (-)
61	DSI0_L3_P	AO	LCD MIPI lane 3 data (+)
50	LCD_TE	DI	LCD Tearing effect output
49	LCD_RST_N	DO	LCD Reset
29	WLED_PWM	DO	LCD Backlight control

3.16 Touch Control Interface

The module provides a Capacitive Touch Screen (TS) interface support over I2C along with corresponding power and interrupt pins.

A reference circuit for the TS interface is shown below.

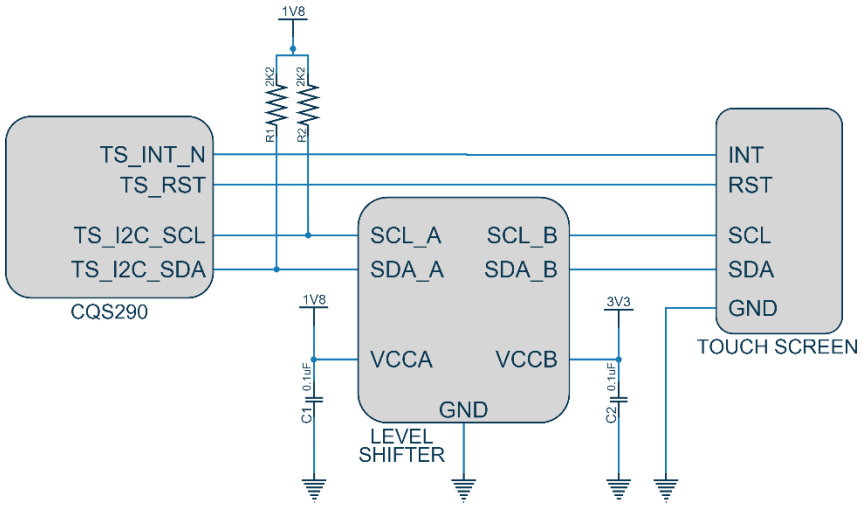


Figure 20 Touchscreen Interface

Table 23 TS Interface Pin definitions

Pin No.	Pin name	I/O	Description
30	TS_INT_N	DI	Touch Screen Interrupt
31	TS_RST	DO	Touch Screen Reset
47	TS_I2C_SCL	OD	Touch Screen Clock
48	TS_I2C_SDA	OD	Touch Screen Data

3.17 Camera Serial Interface

The module has two MIPI-CSI 4-bit based Camera interfaces. It supports a maximum pixel output of 25MP.

The module controls the camera interfaces using its two CCI I2C interfaces

The camera setup can be:

- Two cameras of 4-lane + 4-lane or
- Three cameras of 4-lane + 2-lane + 1-lane

The quality of the picture is also reliant on the camera sensor and lens specifications

Table 24 CSI Interface Pin definition

Pin No.	Signal name	I/O	Description
63	CSI1_CLK_N	AI	MIPI CSI1 clock (-)
64	CSI1_CLK_P	AI	MIPI CSI1 clock (+)
65	CSI1_LN0_N	AI	MIPI CSI1 lane 0 data (-)
66	CSI1_LN0_P	AI	MIPI CSI1 lane 0 data (+)
67	CSI1_LN1_N	AI	MIPI CSI1 lane 1 data (-)
68	CSI1_LN1_P	AI	MIPI CSI1 lane 1 data (+)
70	CSI1_LN3_N	AI	MIPI CSI1 lane 3 data (-)
71	CSI1_LN3_P	AI	MIPI CSI1 lane 3 data (+)

72	CSI1_LN2_N	AI	MIPI CSI1 lane 2 data (-)
73	CSI1_LN2_P	AI	MIPI CSI1 lane 2 data (+)
157	CSI0_CLK_N	AI	MIPI CSI0 clock (-)
158	CSI0_LN0_N	AI	MIPI CSI0 lane 0 data (-)
159	CSI0_LN1_N	AI	MIPI CSI0 lane 1 data (-)
160	CSI0_LN2_N	AI	MIPI CSI0 lane 2 data (-)
161	CSI0_LN3_N	AI	MIPI CSI0 lane 3 data (-)
196	CSI0_CLK_P	AI	MIPI CSI0 clock (+)
197	CSI0_LN0_P	AI	MIPI CSI0 lane 0 data (+)
198	CSI0_LN1_P	AI	MIPI CSI0 lane 1 data (+)
199	CSI0_LN2_P	AI	MIPI CSI0 lane 2 data (+)
200	CSI0_LN3_P	AI	MIPI CSI0 lane 3 data (+)
74	CAM0_MCLK0	DO	Master clock of camera 0
75	CAM_MCLK1	DO	Master clock of camera 1
79	CAM0_RST_N	DO	Reset of camera 0
80	CAM0_PWDN	DO	Power down of camera 0
81	CAM1_RST_N	DO	Reset of camera 1
82	CAM1_PWDN	DO	Power down of camera 1
83	CCI_I2C_SCL0	OD	I2C clock of camera 0
84	CCI_I2C_SDA0	OD	I2C data of camera 0
163	CAM2_PWDN	DO	Power down of camera 2

164	CAM2_RST_N	DO	Reset of camera 2
165	CAM_MCLK2	DO	Master clock of camera 2
166	CCI_I2C_SCL1	OD	I2C clock of camera 1
205	CCI_I2C_SDA1	OD	I2C data of camera 1

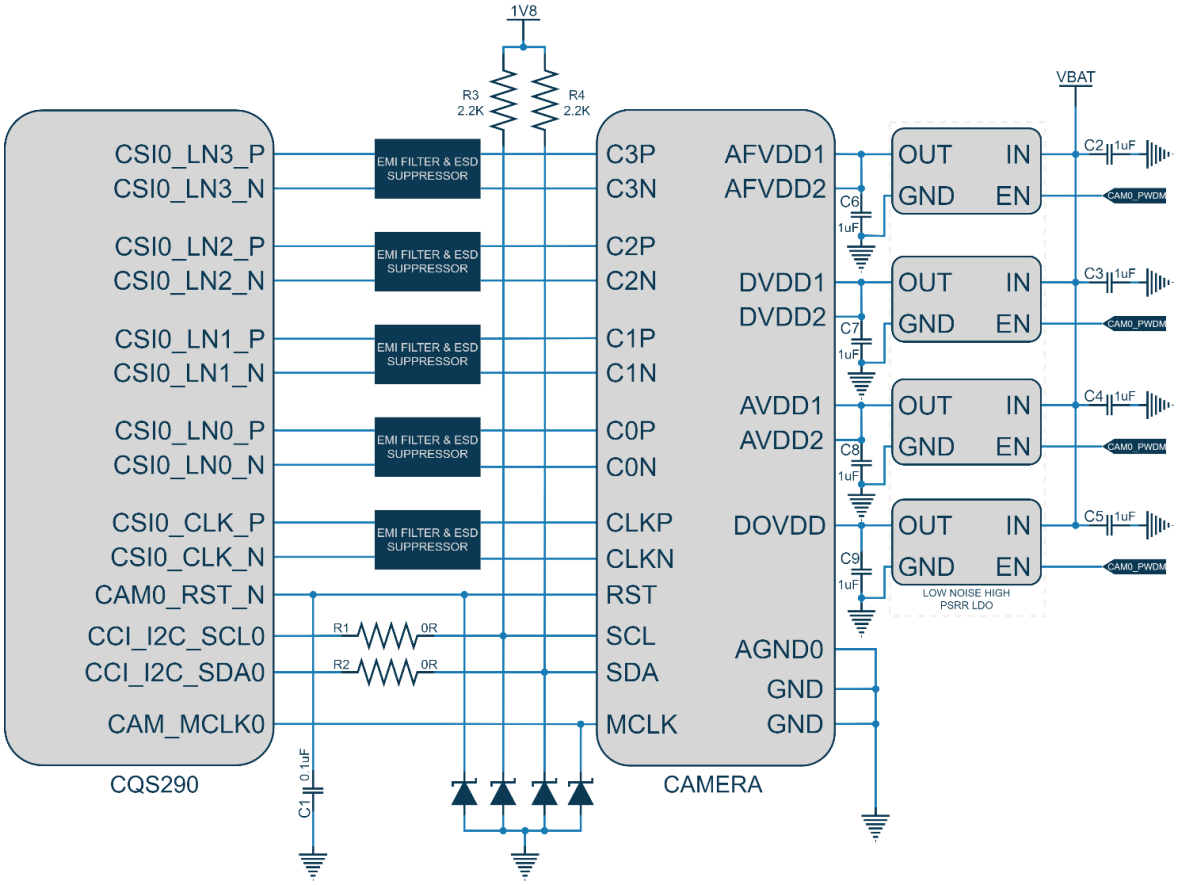


Figure 21 Camera Serial Interface Reference Circuit

3.18 Audio Interfaces

The module provides two analog output channels (1x Headphone, 1x Aux), two analog input channels (2x MIC) and two digital input channels (2xDMIC).

The audio is parsed through the I2S Standards

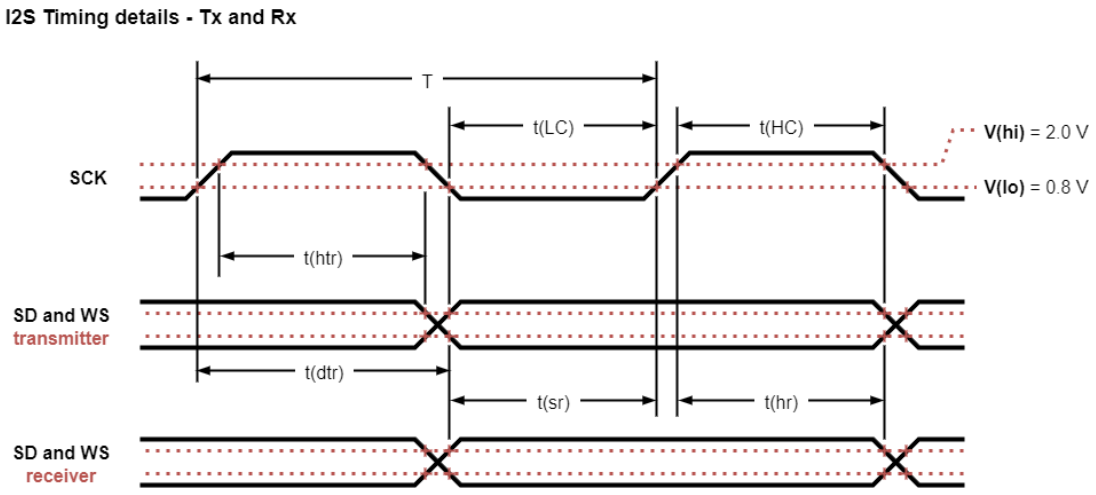


Figure 22: I2S Timing Diagram

3.18.1 Head

The module provides an analog audio output via this interface and can be given to a headphone jack. Hot plug detection is possible using the HEAD_DET pin (Pin 16)

Table 25 Head pin definition

Pin No.	Pin name	I/O	Description
138	HEAD_L	AO	Left side Headphone Out
136	HEAD_R	AO	Right side Headphone Out
137	HEAD_GND	GND	Headphone Ground
139	HEAD_DET	AIO	Headphone Detect

3.18.2 Line out

The module provides an analog audio output this interface. This can be connected to a speaker via an amplifier.

Table 26 AUX Pin definition

Pin No.	Pin name	I/O	Description
10	AUX_P	AO	Auxiliary out positive
11	AUX_M	AO	Auxiliary out negative

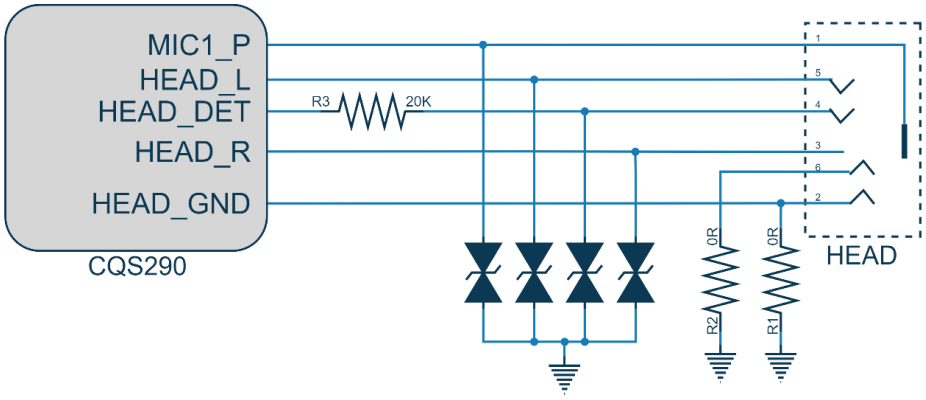


Figure 23 Head Jack

3.18.3 EAR

The module provides an analog audio output this interface. This can be connected to a speaker via an amplifier.

Table 27 AUX Pin definition

Pin No.	Pin name	I/O	Description
8	EAR_P	AO	Earpiece out positive
9	EAR_N	AO	Earpiece out negative

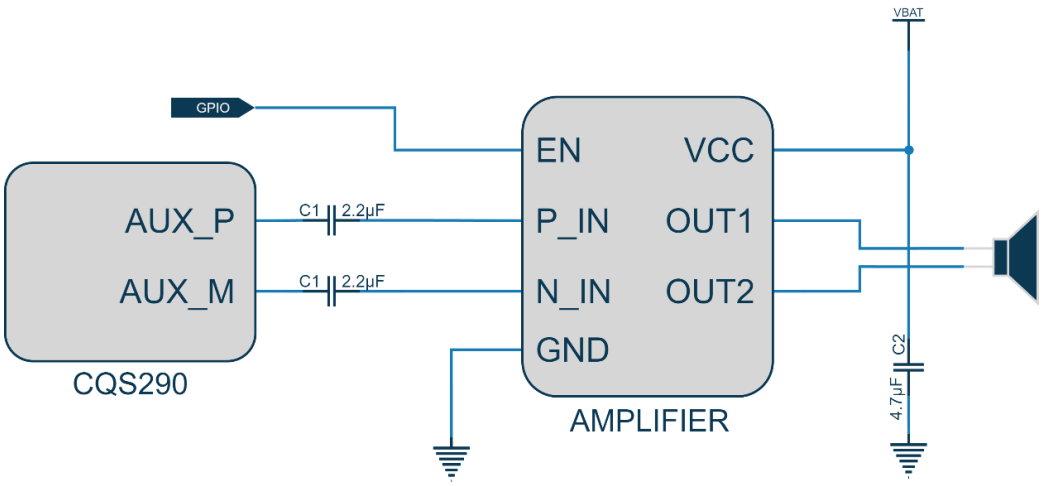


Figure 24 Audio Jack

NOTE

- *Audio Gain control is done via software.*

3.18.4 Analog MIC

The module supports two analog audio inputs. ECM is possible.

Table 28 Analog MIC Pin definition

Pin No.	Pin name	I/O	Description
4	MIC1_P	AI	Microphone input for channel 1 (+)
5	MIC1_N	AI	Microphone input for channel 1 (-)
6	MIC2_P	AI	Microphone input for headset (+)
147	MIC_BIAS1	PO	Bias voltage 1 output for microphone
148	MIC3_P	AI	Microphone input for channel 3 (+)
149	MIC3_N	AI	Microphone input for channel 3 (-)
155	MIC_BIAS3	PO	Bias voltage 3 output for microphone

3.19 Charging Interface

The module supports battery charging. The battery charger IC in the module supports trickle charging, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion batteries.

- ✓ Trickle charging: There are two steps in this mode. When the battery voltage is below 2.1 V, a 90mA trickle charging current is applied to the battery. When the battery voltage is charged up and is between 2.1 V and 3.4 V, the charging current can be set to 400 mA maximally.
- ✓ Constant current mode (CC mode): When the battery is increased to 3.4 to 4.35 V, the system will switch to CC mode. The maximum charging current is 1.85 A when an adapter is used for battery charging, and the maximum charging current is 450 mA for USB charging.
- ✓ Constant voltage mode (CV mode): When the battery voltage reaches the final value 4.35 V, the system will switch to CV mode and the charging current will decrease gradually. When the battery level reaches 100 %, charging is completed.

Table 29 Charging Interface pin definition

Pin No.	Pin name	I/O	Description
133	BAT_P	AI	Battery voltage detect (+)
183	BAT_M	AI	Battery voltage detect (-)
134	BAT_THERM	AI	Battery temperature detect
185	BAT_ID	AI	Battery type detect

3.20 Antenna

The CQS29X module provides four antenna interfaces, one Main set antenna interface, which is responsible for the LTE and GSM signals of the transceiver module, a Diversity antenna, a GNSS antenna interface and a WiFi/BT antenna interface.

The impedance of the antenna interfaces is 50 ohms.

Table 30 Antenna Interface pin definition

Pin No.	Signal Name	IO	Description	Remarks
87	MAIN_ANT	AIO	Main antenna interface	50Ω characteristic impedance
131	DIV_ANT	AI	Diversity antenna interface	50Ω characteristic impedance
121	GNSS_ANT	AI	GNSS antenna interface	50Ω characteristic impedance
77	WIFI/BT_ANT	AIO	WiFi/BT/FM antenna interface	50Ω characteristic impedance

The pin-201 of the CQS29X is the main antenna interface and pin 171 is diversity antenna interface.

To facilitate the debugging of the antenna, a **π**-type matching circuit needs to be added to the main board, and a 50-ohm impedance line is taken.

Recommended circuit is shown below：

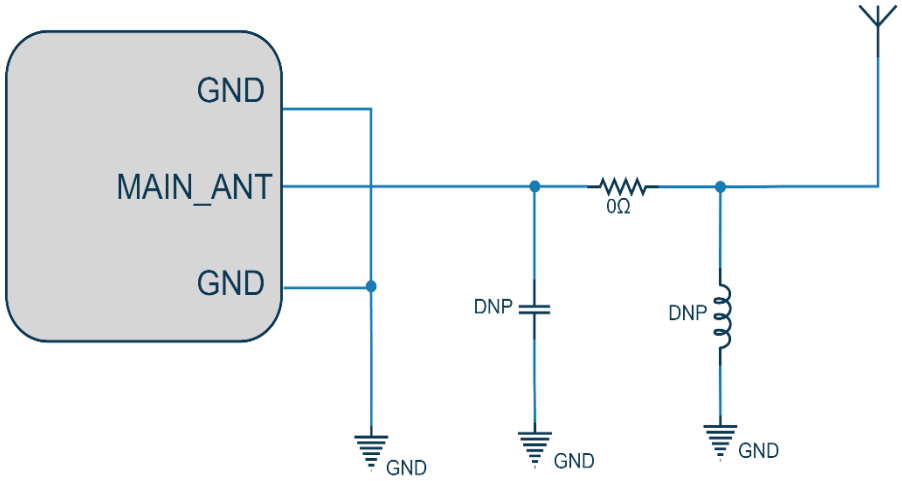


Figure 25 Main antenna matching circuit

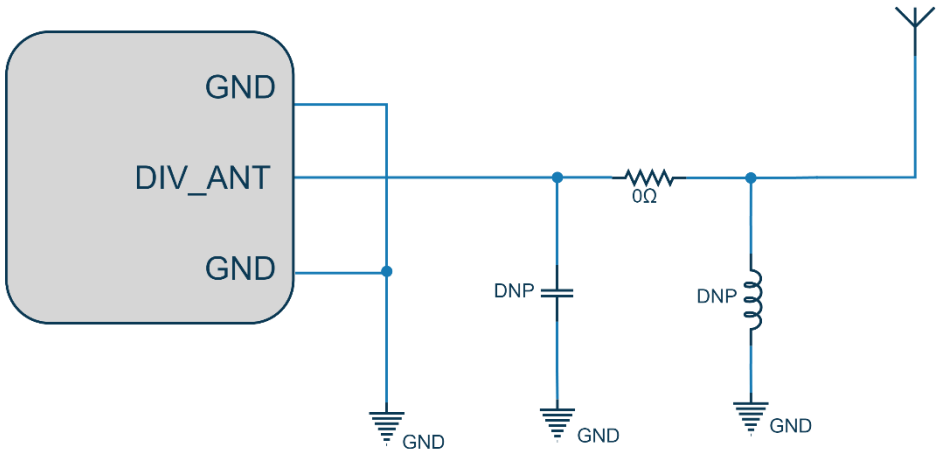


Figure 26 Diversity Antenna matching circuit

The pin 163 of CQS29X is the GNSS antenna interface.

The CQS29X has a dedicated antenna **L1**, it supports GPS, GLONASS, BEIDOU, QZSS, Galileo,

With QZSS and SBAS Ranging support.

In order to facilitate antenna debugging, a **π**-type matching circuit needs to be added to the motherboard and a 50-ohm impedance line is used.

NOTE

- *The GNSS antenna needs to maintain a certain distance from the main antenna.*
- *The GNSS antenna has two antenna connection mode:*

Passive antenna mode and Active antenna mode

- *External power needs to be provided since the module itself cannot supply power to GNSS Active antenna.*

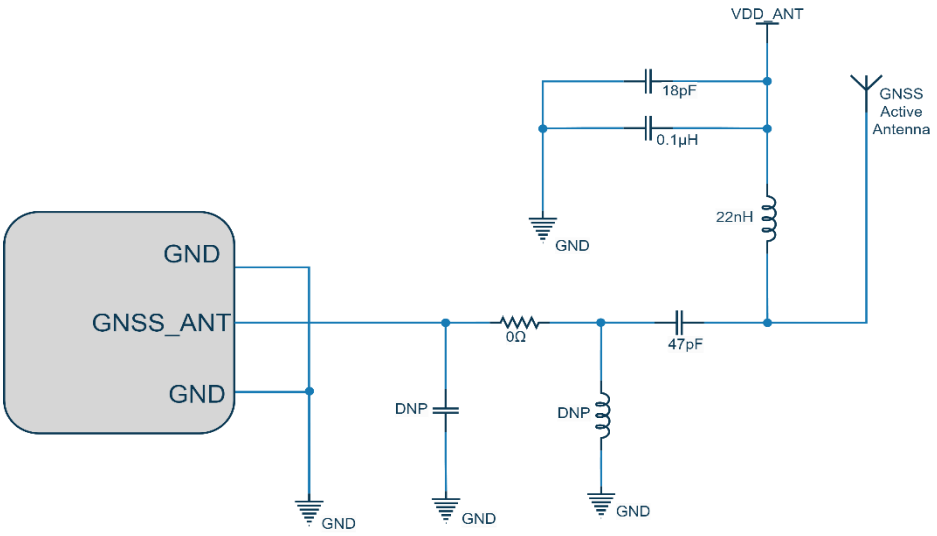


Figure 27 GNSS active antenna matching circuit

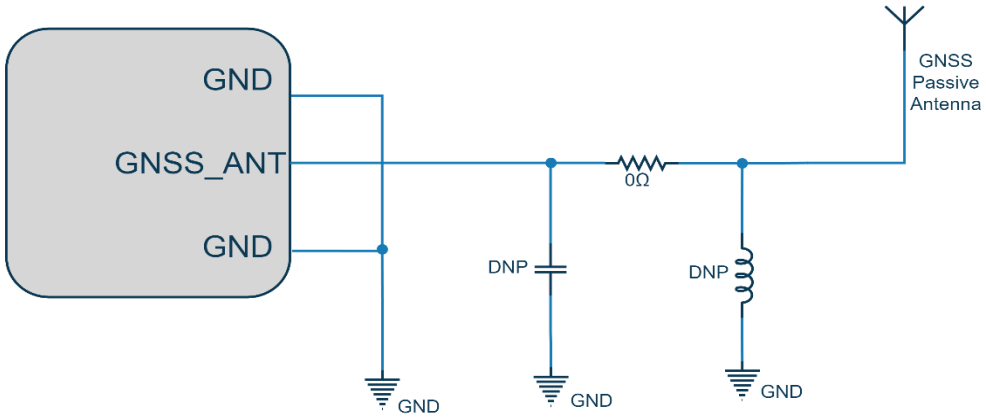


Figure 28 GNSS passive antenna matching circuit

NOTE

- *An external LDO can be selected to supply power according to the active antenna requirement.*
- *If the module is designed with a passive antenna, then the VDD circuit is not needed.*
- *The LTE_MAIN antenna is distributed reasonably to improve the receiving sensitivity.*
- *In actual use, the antenna board can be debugged and optimized according to the user's circuit board.*
- *Antenna impedance traces need to be away from digital signal lines, power supplies and other*

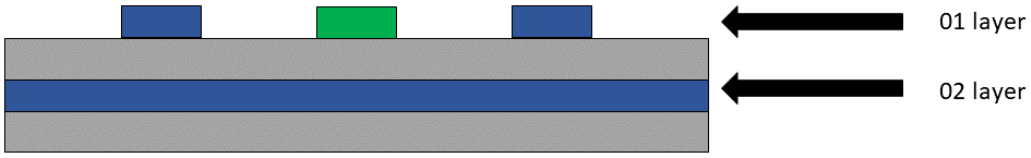
interference signals.

- *The antenna impedance traces need to be three-dimensionally packaged, and the ground holes are added on both sides of the trace to isolate.*

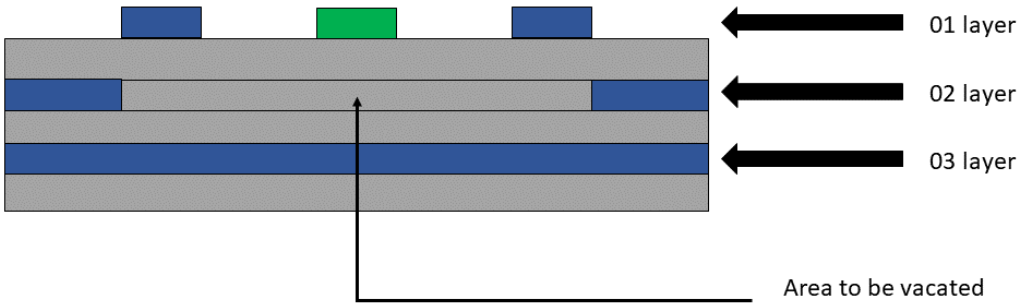
3.20.1 RF Trace Reference

The main set of the CQS29X module are extracted by pad. The antenna pad to the antenna feed point must use microstrip lines or other types of RF traces. The characteristic impedance of the signal line should be controlled at 50Ω.

The impedance of the RF signal line is determined by the material's dielectric constant, trace width (W), ground clearance (S), and reference ground plane height (H). Therefore, the RF trace requires an impedance simulation tool to calculate the impedance of the RF trace.



MODE 1 - Reference ground is the second layer PCB coplanar transmission line structure



MODE 2 - Reference ground is the third layer PCB coplanar transmission line structure

Figure 29 Coplanar Antenna

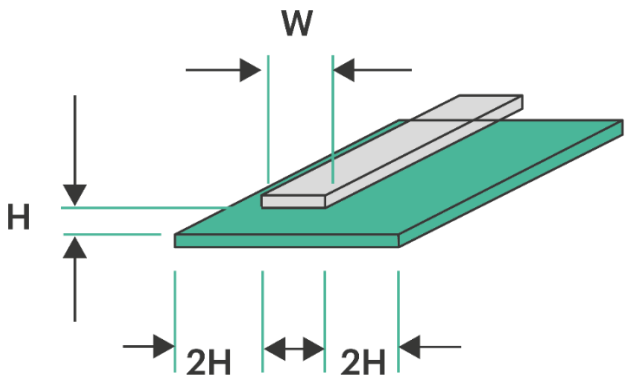


Figure 30 The complete structure of the two-layer PCB microstrip line

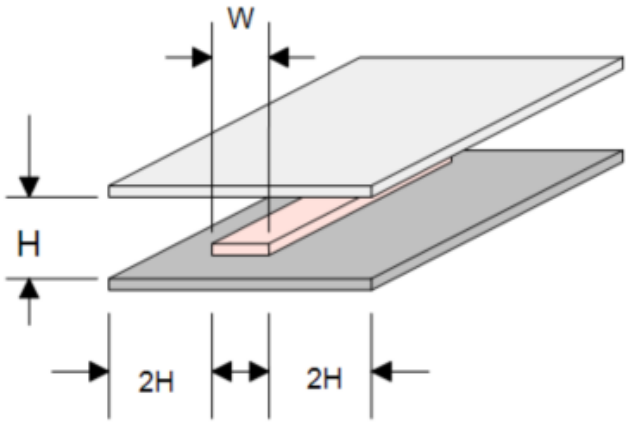


Figure 31 The complete structure of the multilayer PCB strip line

NOTE

- *Since Coplanar antennas are having maximum noise immunity, it is preferred.*

3.21 GNSS Interface

Multi – GNSS receiver:

- ✓ **L1 / L1+L5** multi-band GNSS receiver
- ✓ Multi-Constellation GPS/GLONASS/Galileo/Bei Dou/QZSS.

Table 31 Main parameters of the RF connector

Pin No.	Signal name	I/O	Description
163	GNSS_L1	AI	GNSS L1 antenna interface

3.22 FM Interface

FM functionality is integrated in CQS29x. The current design will allow the earphone itself to serve as the FM antenna when plugged into the headphone jack. In case an external antenna for FM is to be interfaced, it should be connected to the GND reference pin of the Headphone (HEAD_GND)

Table 32 FM Antenna pin

Pin No.	Signal name	I/O	Description
137	HEAD_GND	AI	FM antenna function integrated

4 Overall Technical Indicators

4.1 Chapter Overview

The CQS29X module RF overall specifications include the following sections:

- ✓ Working frequency
- ✓ GNSS Performances
- ✓ Antenna requirements

4.2 Working Frequency

Table 33 RF frequency table

Frequency band	Uplink frequency	Downstream frequency	Mode
LTE B1	1920MHz–1980MHz	2110MHz–2170MHz	FDD
LTE B2	1850 MHz– 1910 MHz	1930 MHz– 1990 MHz	FDD
LTE B3	1710MHz–1785MHz	1805MHz–1880MHz	FDD
LTE B4	1710 MHz– 1755 MHz	2110 MHz– 2155 MHz	FDD
LTE B5	824MHz–849MHz	869MHz–894MHz	FDD
LTE B7	2500MHz–2570MHz	2620MHz – 2690MHz	FDD
LTE B8	880MHz–915MHz	925MHz–960MHz	FDD
LTE B12	699MHz – 716MHz	729MHz – 746MHz	FDD
LTE B13	777 MHz – 787 MHz	746 MHz – 756 MHz	FDD
LTE B18	815 MHz – 830 MHz	860 MHz – 875 MHz	FDD
LTE B19	830MHz – 845MHz	875MHz – 890MHz	FDD
LTE B20	832MHz– 862MHz	791MHz– 821MHz	FDD
LTE B25	1850MHz – 1915MHz	1930MHz – 1995MHz	FDD
LTE B26	814MHz – 849MHz	859MHz – 894MHz	FDD

LTE B28	703MHz – 748MHz	758MHz – 803MHz	FDD
LTE B40	2300MHz – 2400Mhz	2300MHz – 2400Mhz	TDD
LTE B41	2496MHz – 2690MHz	2496MHz – 2690MHz	TDD
LTE B66	1710 MHz – 1780 MHz	2110 MHz – 2200 MHz	FDD
LTE B71	663MHz – 698MHz	617MHz – 652MHz	FDD
GSM 900	880MHz-915MHz	925MHz-960MHz	FDD
GSM 1800	1710MHz-1785MHz	1805MHz-1880MHz	FDD

5 Interface Electrical Characteristics

5.1 Chapter Overview

- Working storage temperature
- Electrostatic property
- Module IO level
- Power supply
- Power consumption characteristics

5.2 Working Storage Temperature

Table 34 CQS29X module working storage temperature

Parameter	Minimum	Maximum
Normal operating temperature	-35°C	+85°C
Storage temperature	-55°C	125°C

5.3 Electrostatic Property

There is no overvoltage protection inside the CQS29X module.

The ESD protection is required when the module is used to ensure product quality.

ESD design recommendations:

- ✓ The USB port needs to add TVS on VDD, D+, D- for protection, and the TVS parasitic capacitance on D+/D- is <2pF
- ✓ The module's USIM card external pin needs to be protected by TVS, and the parasitic capacitance requirement is <10pF
- ✓ The PCB layout of the protective device should be as close as possible to the "V" line to avoid the "T" line
- ✓ The ground plane around the module guarantees integrity and should not be split

✓ ESD control of the surrounding environment and operators is required during module production, assembly and laboratory testing

Table 35 CQS29X ESD Features

Test port	Contact discharge	Air discharge	Unit
USB interface	±4	±8	KV
USIM interface	±4	±8	KV
VBAT power supply	±4	±8	KV

5.4 Module I/O Level

5.4.1 Operating Range

The operating voltages are listed below.

Table 36 Operating Condition

Pin Type		V_min	V_typical	V_max
P2	Low Voltage	1.70 V	1.80 V	1.90 V
	High Voltage	2.70 V	2.95 V	3.10 V
P3	-	1.70 V	1.80 V	1.90 V
P5	Low Voltage	1.70 V	1.80 V	2.95 V
	High Voltage	2.70 V	2.95 V	3.10 V
P7	-	1.70 V	1.80 V	1.90 V
VB		3.50 V	4.2 V	4.40 V
CSI		1.15 V	1.20 V	1.26 V
DSI		1.15 V	1.20 V	1.26 V

5.4.2 Digital-logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

Table 37 1.8 V GPIO Digital Logic Characteristics

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × P	P + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3 V	0.35 × P	V
V_{OH}	High-level output voltage, CMOS	P - 0.45	P	V
V_{OL}	Low-level output voltage, CMOS	0.0	0.45	V
I_{IH}	Input high leakage current	-	1.0	µA
I_{IL}	Input low leakage current	-1.0	-	µA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)

Table 38 SDC 2.95V mode DC Specifications (P=P2)

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage	0.65 × P	P + 0.3 V	V
V_{IL}	Low-level input voltage	-0.3 V	0.25 × P	V
V_{OH}	High-level output voltage	0.75 × P	P	V
V_{OL}	Low-level output voltage	0.0	0.15 × P	V
I_{IH}	Input high leakage current	-	10	µA
I_{IL}	Input low leakage current	-10	-	µA
$R_{PULL-UP}$	Pull-up resistance	10	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	100	kΩ

Table 39 SDC 1.8V mode DC Specifications (P=P2)

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage	1.27	2	V
V_{IL}	Low-level input voltage	-0.3 V	0.58	V
V_{OH}	High-level output voltage	1.4	-	V
V_{OL}	Low-level output voltage	-	0.45	V
I_{IH}	Input high leakage current	-	5	µA
I_{IL}	Input low leakage current	-5	-	µA
$R_{PULL-UP}$	Pull-up resistance	10	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	100	kΩ

Table 40 UIM 2.95V / 1.8V mode DC Specifications (P=P5)

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage	0.7 × P	P + 0.3 V	V
V_{IL}	Low-level input voltage	-0.3 V	0.2 × P	V
V_{OH}	High-level output voltage	0.8 × P	P	V
V_{OL}	Low-level output voltage	0.0	0.4	V
I_{IH}	Input high leakage current	-20	20	µA
I_{IL}	Input low leakage current	-	1000	µA
$R_{PULL-UP}$	Pull-up resistance	10	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	100	kΩ

5.5 Power Supply

The CQS29X module input power requirements are as follows:

Table 41 CQS29X Module operating voltage

Parameter	Minimum value	Typical value	Maximum value
Input Voltage	3.5V	4.2V	4.4V

The power-on time of any interface of the module must not be earlier than the boot time of the module, otherwise the module may be abnormal or damaged.

5.6 Power Consumption

Table 42 Android Power Consumption table

Mode	Band	Current consumption @ 23dBm and 3.7V		
		GNSS + Tx Idle	GNSS + Peak Tx @ Centre frequency	Unit
CAT 4 (Android)	Band 1	94.5	610	mA
	Band 2	94.7	600	mA
	Band 3	93.7	520	mA
	Band 4	93.5	530	mA
	Band 5	93.5	510	mA
	Band 7	93.5	500	mA
	Band 8	94.81	510	mA
	Band 12	93.81	520	mA
	Band 13	98.4	560	mA
	Band 17	93.21	500	mA
	Band 18	94.7	500	mA
	Band 19	94.4	540	mA
	Band 20	94.6	600	mA
	Band 25	94.2	650	mA
	Band 26	94.3	540	mA
	Band 28	96	520	mA
	Band 38	94.35	325	mA
	Band 40	93.3	336	mA
	Band 41	93.5	328.4	mA

	Band 66	94.25	680	mA
AT+CFUN=0		92.7		mA
SLEEP		7.1		mA
SHUTDOWN		27.05		uA

Table 43 Linux Power Consumption table

Mode	Band	Current consumption @ 23dBm and 3.7V		
		Tx Idle	Peak Tx @ Centre frequency	Unit
CAT 4 (Linux)	Band 1	89.55	880	mA
	Band 2	89.96	790	mA
	Band 3	90.38	720	mA
	Band 4	89.72	710	mA
	Band 5	89.88	700	mA
	Band 7	89.92	810	mA
	Band 8	89.91	660	mA
	Band 12	89.81	700	mA
	Band 13	91.44	750	mA
	Band 17	89.92	660	mA
	Band 18	89.72	720	mA
	Band 19	89.58	730	mA
	Band 20	89.52	750	mA
	Band 25	89.95	880	mA
	Band 26	89.88	700	mA
	Band 28	89.86	710	mA
	Band 38	89.86	429.82	mA
	Band 40	89.79	560	mA
	Band 41	89.85	430.29	mA
	Band 66	90.35	970	mA
AT+CFUN=0	-	87.34	-	mA
SLEEP	-	TBD	-	mA
SHUTDOWN	-	26.56	-	uA

6 Structural and Mechanical Properties

6.1 CQS29X module mechanical size

The figure below shows the top and bottom view of the module.

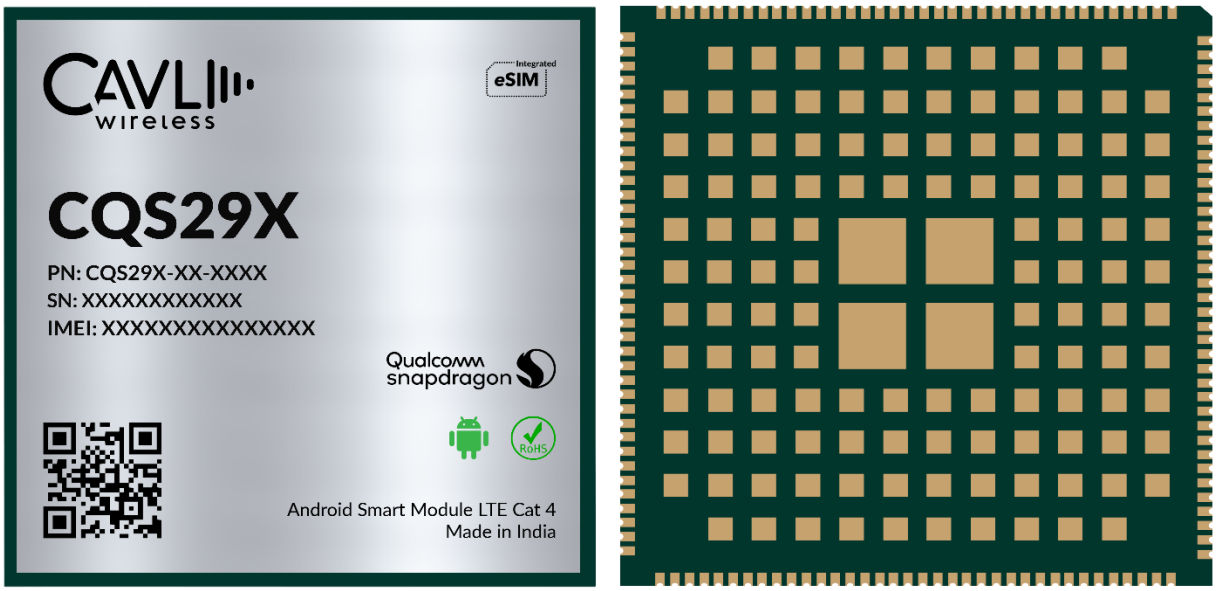


Figure 32 Top view and bottom view of the module

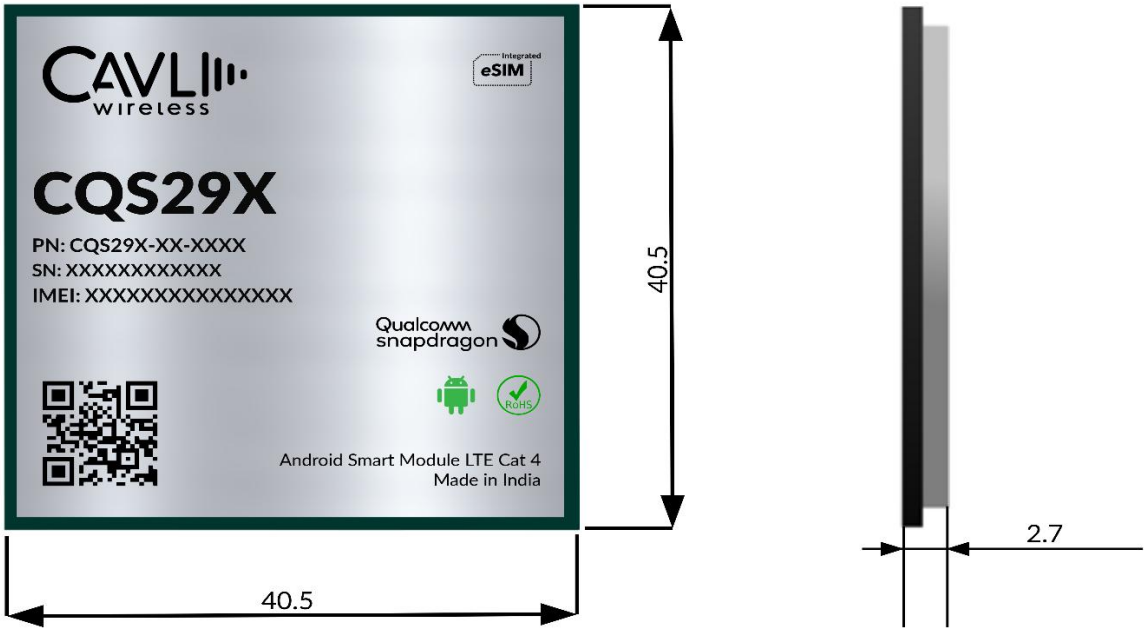


Figure 33 CQS29X module dimensions

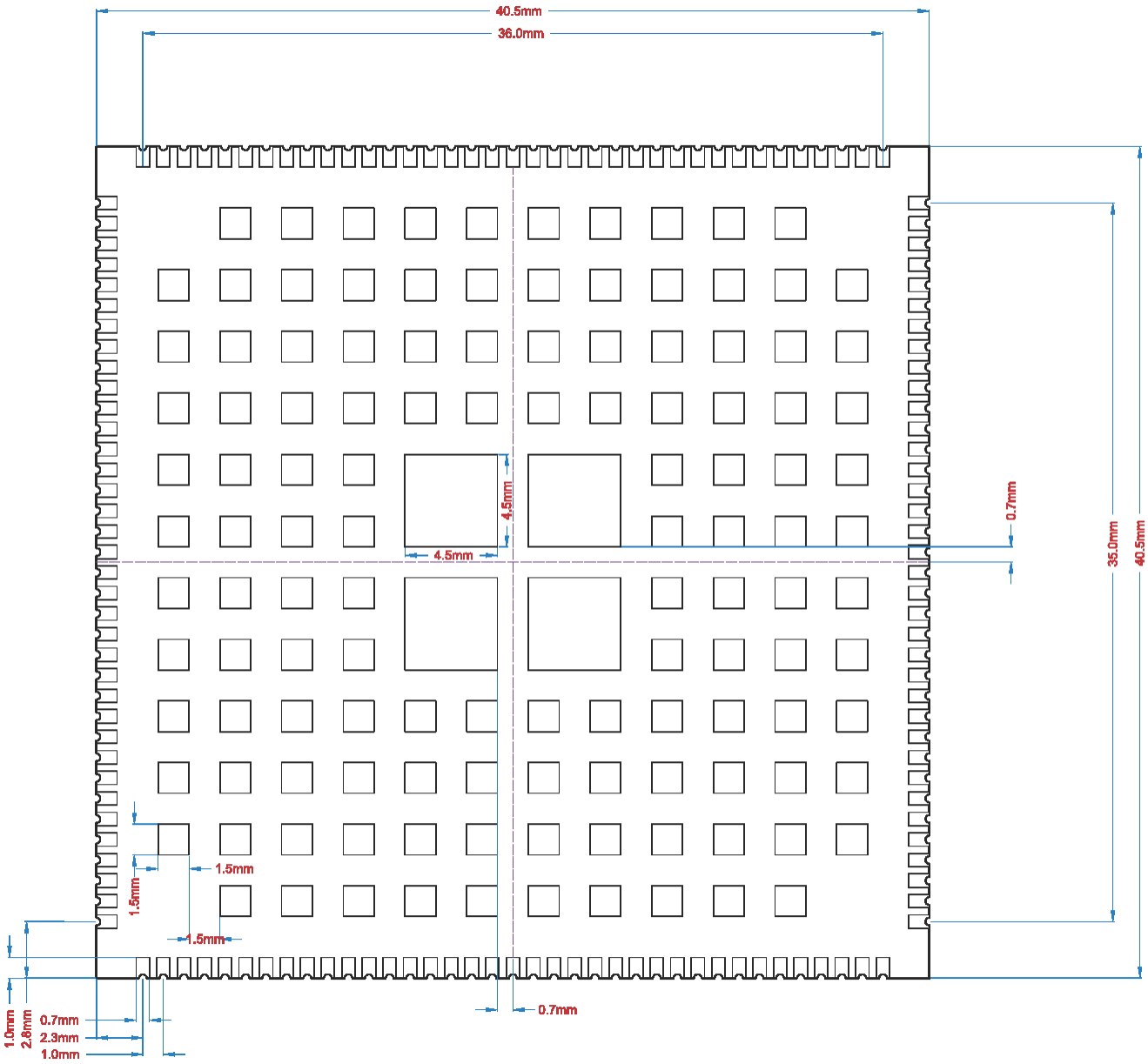


Figure 34 CQS29X module dimensions bottom

6.2 CQS29X Recommended footprint

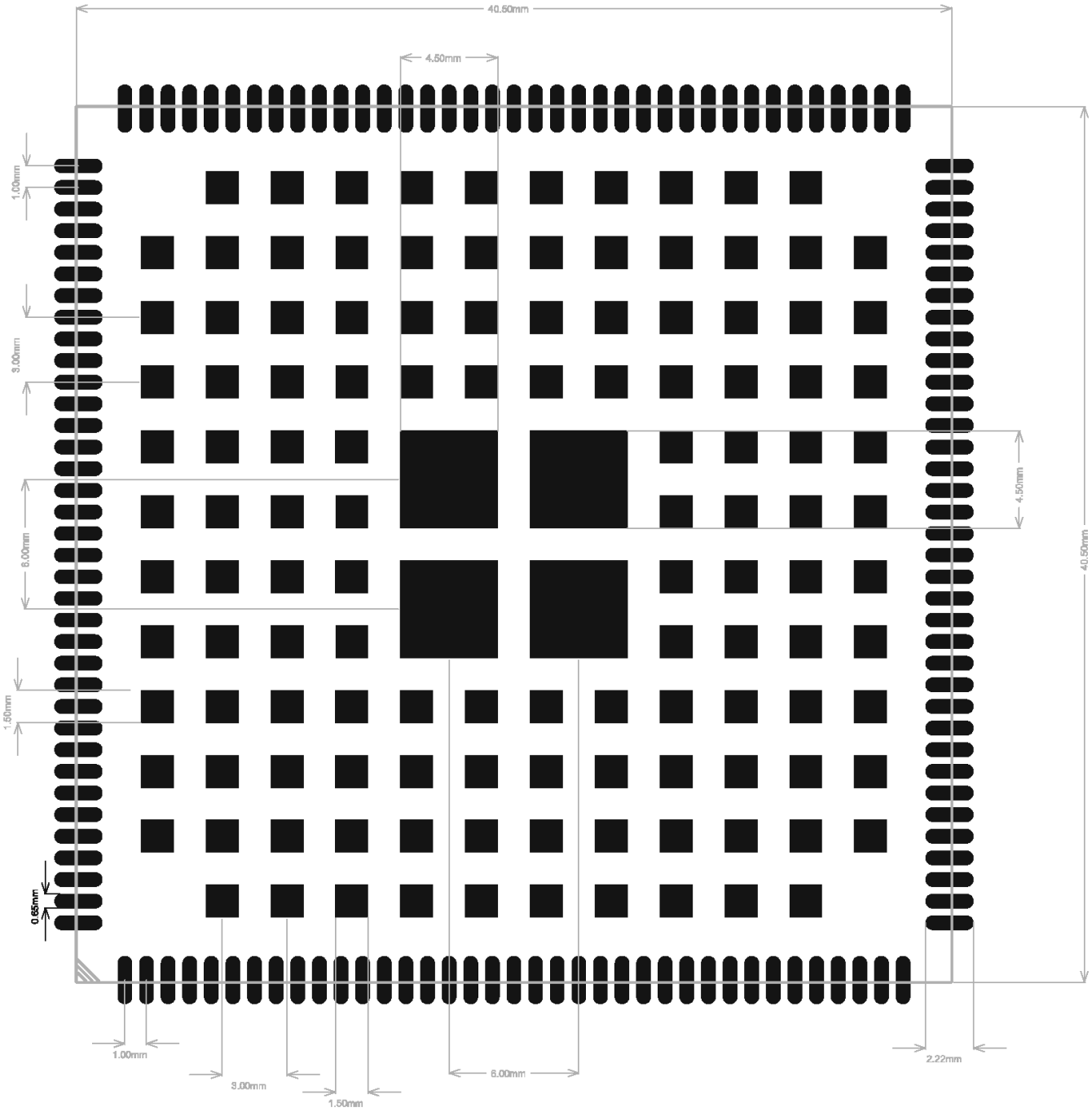


Figure 35 Recommended Footprint

7 Appendix

7.1 Chapter Overview

- ✓ Abbreviations
- ✓ Safety and precautions

7.2 Abbreviations

Abbreviations	Full name
3GPP	Third Generation Partnership Project
AP	Access Point
AMR	Adaptive multi-rate
BER	Bit Error Rate
CCC	China Compulsory Certification
CDMA	Code Division Multiple Access
CE	European Conformity
CSD	Circuit Switched Data
CTS	Clear to Send
DC	Direct Current
DTR	Data Terminal Ready
DL	Down Link
DTE	Data Terminal Equipment
DRX	Discontinuous Reception

EDGE	Enhanced Data Rate for GSM Evolution
EU	European Union
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FCC	Federal Communications Commission
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communication
HSDPA	High-Speed Downlink Packet Access
HSPA	Enhanced High Speed Packet Access
HSUPA	High Speed Up-link Packet Access
IMEI	International Mobile Equipment Identity
LED	Light-Emitting Diode
LTE	Long Term Evolution
NC	Not Connected
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PMU	Power Management Unit
PPP	Point-to-point protocol
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of the Use of Certain Hazardous Substances
SMS	Short Message Service
TIS	Total Isotropic Sensitivity
TVS	Transient Voltage Suppressor

TX	Transmitting Direction
UART	Universal Asynchronous Receiver-Transmitter
UMTS	Universal Mobile Telecommunications System
USIM	Universal Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WWAN	Wireless Wide Area Network

7.3 Safety and Precautions

In order to use the wireless device safely, the terminal device informs the user of the relevant safety information:

- ✓ **Interference:** When the use of wireless devices is prohibited or the use of the device may cause interference and security of the electronic device, turn off the wireless device. Because the terminal will send and receive RF signals when it is powered on. It can interfere with TV, radio, computer or other electrical equipment.
- ✓ **Medical equipment:** In medical and health care facilities where the use of wireless devices is prohibited in the express text, please follow the regulations of the site and turn off the device. Some wireless devices may interfere with the medical device, causing the medical device to malfunction or cause errors. If interference occurs, turn off the wireless device and consult a physician.
- ✓ **Flammable and explosive areas:** In flammable and explosive areas, please turn off your wireless device and follow the relevant label instructions to avoid an explosion or fire. For example; gas stations, fuel zones, chemical products areas, chemical transportation and storage facilities, areas with explosion hazard signs, areas with “turn off radio equipment” signs, etc.
- ✓ **Traffic Safety:** Please comply with local laws or regulations in your country or region regarding the use of wireless devices when driving a vehicle.
- ✓ **Aviation Safety:** When flying, please follow the airline's regulations and regulations regarding the use of wireless devices. Before taking off, turn off the wireless device to prevent wireless signals from interfering with aircraft control signals.
- ✓ **Environmental Protection:** Please comply with local laws regarding the handling of equipment packaging materials, equipment or accessories, and support recycling operations.
- ✓ **Emergency call:** This device uses wireless signals for propagation. Therefore, there is no guarantee that the network can be connected in all situations, so in an emergency this wireless device cannot be used as the only contact method.