Re-imagining Cellular IoT Solutions

Cavli CQ10
LTE CAT 1 / 2G Module

Hardware Manual

External Release Version 1.0

Connect to our website and feel free to contact our technical support team for any assistance.

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Table of Contents

Table of Figures

VERSION HISTORY

Version	Edit	Release Date
Pre-Release Version		
1.0	• Initial Version	01/02/2024
1.1	• Updated the Revised Technical Information • Update the Reference circuits	25/07/2024
External Release Version		
1.0	• Initial Version	17/01/2025

1 Introduction

This document is the **Hardware Manual** of the Cavli Wireless solution product **CQ10 Module**, which describes:

- ✓ The hardware composition and functional features of the module
- ✓ The definition and usage of the application interface
- ✓ The electrical performance and mechanical properties of the module

This document and the other application documents combined will enable users to develop end devices with Cavli Modules.

2 Module Overview

2.1 Module Introduction

CQ10 module integrates an application processing subsystem, a communication subsystem, multimedia, and connectivity peripherals to enable a single chip 4G LTE feature phone solution.

The CQ10 communication subsystem integrates **LTE CAT 1** technology, **GSM** Modem Baseband, and an RF transceiver to cover bands 1/2/3/4/5/7/8/12/13/18/19/20/25/26/28/40/66 and GSM 900/GSM1800 (**W.W**), 2/4/5/12/13/25/66 (**N.A**) , 1/3/5/7/8/18/19/20/26/28/40 and GSM 900/GSM1800 (**EAJ**), 1/3/7/8/20/28 and GSM900/GSM 1800 (**E.U**), 1/3/5/8/40 and GSM900/ GSM1800, 1/3/5/8/18/19/26/28 and GSM900/GSM 1800 (**A.N**), 1/2/3/4/5/7/8 and GSM900/ GSM1800 (**L.A**) and LTE CAT 1 is compliant with 3GPP E-UTRA Release 10.

The application subsystem runs on a single ARM Cortex A7 processor at 1.3GHz with integrated peripherals for connectivity and multimedia.

The CQ10 module can be used in the following applications

- ✓ Vehicle telematics
- ✓ Asset tracking
- ✓ Fleet management
- ✓ Smart city and smart home applications
- ✓ Connected retail applications- point of sale devices, automated teller machines, vending machines etc.
- ✓ Industrial IoT - gateways, remote control & monitoring systems

NOTE

- **E.A.J** – Europe Asia & Japan
- **N.A** – North America
- **A.N** – Australia, New Zealand, Taiwan and South Korea
- **L.A** – Latin America
- **W.W** – Global
- **E.U** – European Union
- **I.N** - India

2.2 Module Characteristics

Table 2.1 Key Features

Characteristics		Description
Physical Characteristics		32 mm x 29 mm
Fixed Way		LGA+LCC package
Operating Voltage		3.6V – 4.5V Typical Voltage 3.8 V
Application Processor		ARM Cortex A7 with 1.3GHz clock with 256KB L2 Cache
Operating System		Linux 4.14
Memory		256 MB RAM, 256/ 512 MB Flash
Pin Count		144
Application Interface	USIM card	Supports 1.8V/2.85V. Supports hot swap function
	USB	✓ USB2.0 (480Mbps) ✓ USB can function as both master and slave ✓ OTG Host mode support
	UART	✓ AT commands and data transfer ✓ The max baud rate is up to 4Mbps. Default is 115200bps.
	PCM	✓ For audio, external codec chip ✓ Support short frame mode. ✓ Support main mode
	SDIO	✓ Compliant with SDIO 3.0 protocol ✓ Comply with IEEE 802.11 standard
	SDC	✓ Compliant with SDIO 3.0 protocol ✓ 4-bit SDC ✓ Can be interfaced with Wi-Fi Transceiver
	I2C	✓ Compliant with I2C bus protocol ✓ High speed mode supports 3.3Mbps rate

	ADC	✓ 2 ADC lines
	Network Indication	✓ STATUS Module status
	GNSS	✓ GPS, GLONASS, BEIDOU, GALILEO, QZSS
	SPI	✓ Standard SPI interface
	Ethernet	✓ SGMII interface
Frequency Band		**WW:** LTE BANDS: 1/2/3/4/5/7/8/12/13/18/19/20/25/26/28/40/66 GSM BANDS: GSM900/ GSM1800 **NA:** LTE BANDS: 2/4/5/12/13/25/66 **EAJ:** LTE BANDS: 1/3/5/7/8/18/19/20/26/28/40 GSM BANDS: GSM900/ GSM1800 **EU:** LTE BANDS: 1/3/7/8/20/28 GSM BANDS: GSM900/ GSM1800 **IN:** LTE BANDS: 1/3/5/8/40 GSM BANDS: GSM900/ GSM1800 **AN:** LTE BANDS: 1/3/5/8/18/19/26/28 GSM BANDS: GSM900/ GSM1800 **LA:** LTE BANDS: 1/2/3/4/5/7/8 GSM BANDS: GSM900/ GSM1800

Data Network	✓ FDD/TDD LTE CAT 1/4G ✓ Peak DL 150 Mbps/ UL 50 Mbps (CAT 4) ✓ Peak DL 236.8Kbps/ UL 236.8 Kbps (2G)
AT Command	✓ Specific AT Query CQ10 AT command set
Network Protocol	TCP/HTTP/MQTT/HTTP/HTTPS/MQTTS/FTP/FTPS/PPP/SNMP /Web Socket protocols
Antenna Interface	✓ MAIN x 1 ✓ GNSS × 1 ✓ Characteristic impedance 50 Ω
Virtual Network Card	Supports USB virtual network card
Temperature Range	Normal working temperature: - 30℃ to +85℃
Humidity	RH5%～RH95%
Module Function Distinction	**M** on the model number represents the multi-mode

NOTE

- *When the temperature is in the range of –30℃ to –20℃ or +75℃ to +85℃, some RF specifications of the CQ10 module may not meet the 3GPP standards.*

2.3 Module Function

CQ10 Module mainly consists of the following circuit units:

- ✓ Baseband processing unit
- ✓ Power Management unit
- ✓ Memory unit
- ✓ RF Transceiver unit
- ✓ RF front-end unit
- ✓ RF Band SAW Duplex array
- ✓ Multi-Band PA
- ✓ Interfaces

The functional block diagram of CQ10 module is shown below：

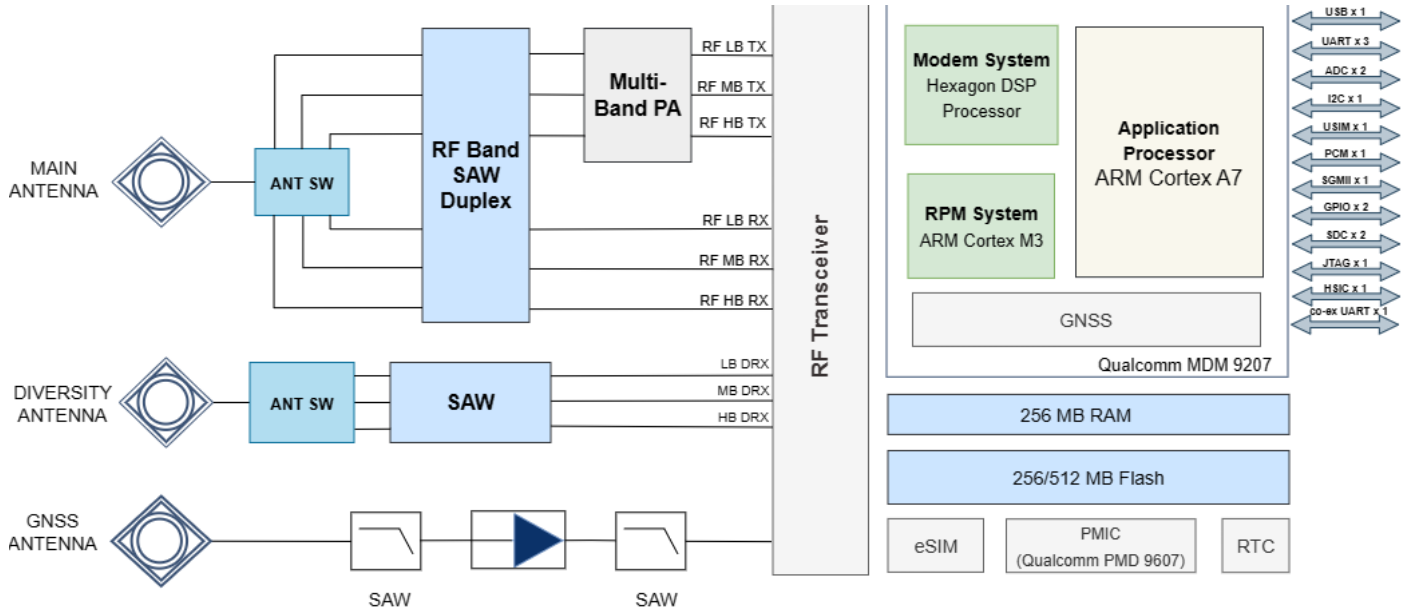

Figure 1 CQ10 Functional Block Diagram

2.4 Module Working Mode

Table 2.2 Working Mode

Working Mode	Description
Turn off the machine	In the case of shutdown, the module is fully powered off.
Flight Mode	The module closes the module RF circuit, unable to interact with the network
Dormancy	The module closes most functions, and it will synchronize with the network.
Ideal State	Turn on the machine and register the network successfully, in the idle state
Data transmission	The module is in working state and has data interaction with the network.

3 Interface Application Description

3.1 Chapter Overview

This chapter mainly describes the interface definition and application of this module. It contains the following sections:

- Module Interface
- Power Interface
- Switching Machine Reset Mode
- USB Interface
- UART Interface
- USIM Interface
- Network Status Indicator Interface
- PCM Digital Voice Interface
- I2C Bus
- ADC interface
- Antenna
- Control Interface
- GNSS Interface
- SPI Interface
- SDIO Interface
- SGMII Interface

3.2 Module Interface

3.2.1 CQ10 Pin Layout

CQ10 pins (Top View) are assigned as follows：

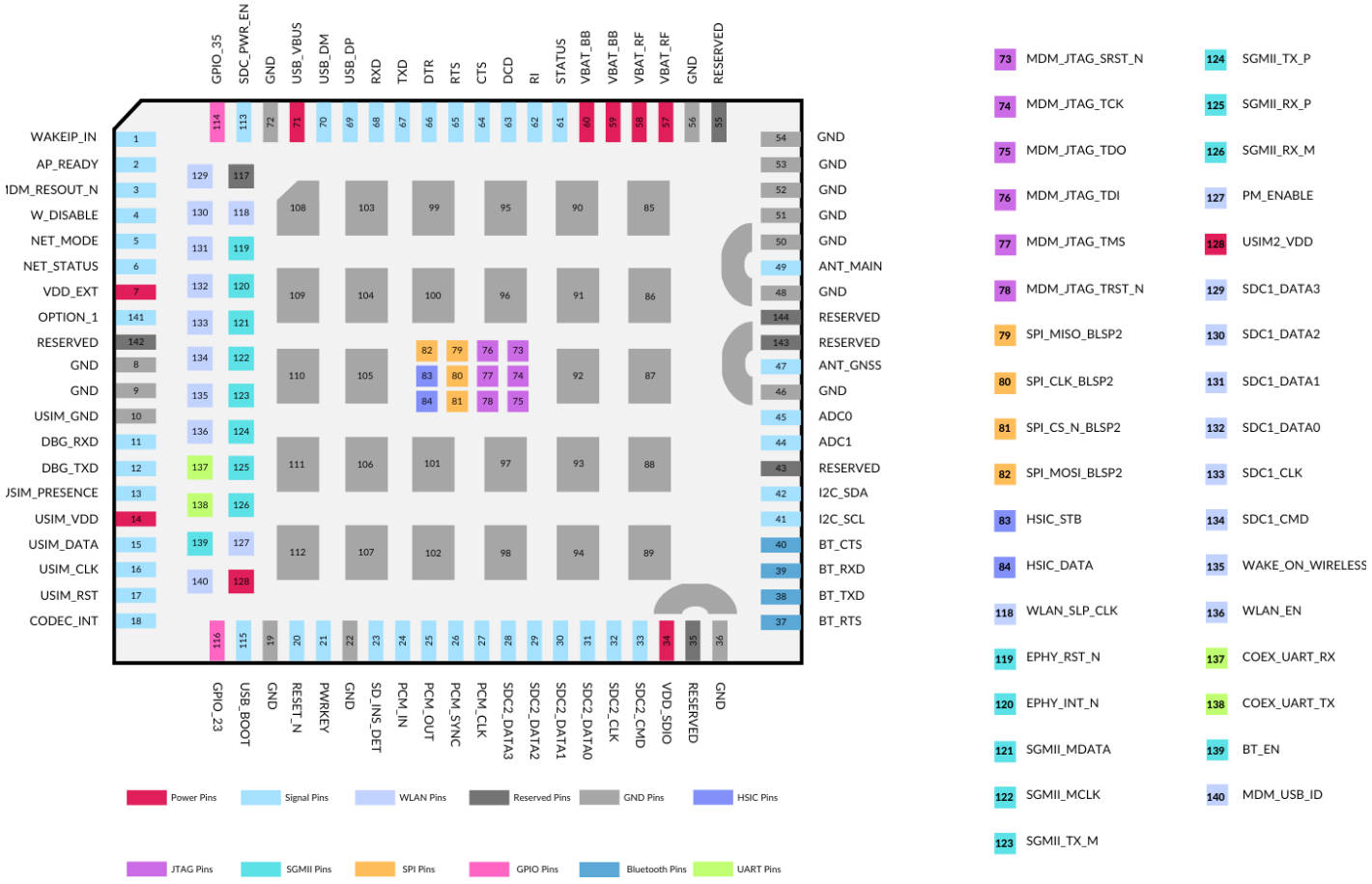

Figure 2 CQ10 module Interface definition (Top view)

NOTE

- *All RESERVED and unused pin feet need to be left floating*

3.2.2 CQ10 Pin Interface

The CQ10 module has the LGA interface. The module interface definition is shown in the following table:

Table 3.1 Pin Description

Pin Type	Description
PAD TYPE	
AI	Analog Input
AO	Analog Output
RF_IO	RF bi-directional signal
RF_I	RF input signal
B	Bidirectional digital with CMOS input
DI	Digital Input (CMOS)
DO	Digital Output (CMOS)
DIO	Digital Input/Output
OD	Open Drain
H	High voltage tolerant
Z	High Impedance output
PI	Power Input
PO	Power Output
PIO	Power Input/Output
Pad pull details	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpupk = default no-pull with programmable option following the colon (:) PD: pdpupk = default pull-down with programmable option following the colon (:) PU: pdpupk = default pull-up with programmable option following the colon (:) KP: pdpupk = default keeper with programmable option following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)

NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device

3.2.3 Absolute maximum ratings

The absolute maximum ratings table reflects the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Operating conditions.

Table 3.2 Absolute Maximum ratings

Pin Type	V_min	V_max
P2	-0.3 V	3.41 V
P3	-0.3 V	2.09 V
P5	-0.3 V	3.41 V
P8	0.3V	1.44V
VB	-0.3 V	4.5 V

3.2.4 Operating Conditions

The operating voltages are listed below.

Table 3.3 Operating Condition

Pin Type	V_min	V_typical	V_max
P2	1.70 V / 2.70V	1.80 V / 2.95V	1.90 V / 3.10V
P3	1.70 V	1.80 V	1.90 V
P5	1.70 V / 2.70V	1.80 V / 2.95V	1.90 V / 3.10V
P8	1.15V	1.2V	1.25V
VB	3.50 V	3.80 V	4.40 V

Table 3.4 Pin Name

Pin No.	Pin Name	Pad type	Voltage definition	Pin Description	Comments	Configurable Function Pad type	Configurable Functions
1	WAKEUP_IN	DI	P3	HW interrupt to wake up from sleep	Active low input for 500ms	DI DO	GNSS_TX_AGGRESSOR QDSS_TRACEDATA_9B
2	AP_READY	DO	P3	Wake up Interrupt	-	DO DO	DR_SYNC QDSS_TRACEDATA_0B
3	MDM_RESOUT_N	DO	P3	Reset Output	-	-	-
4	W_DISABLE	DI	P3	Flight mode	Active low input for 500ms	DO DO	RFFE2_CLK QDSS_TRACEDATA_15B
5	NET_MODE	DO	P3	Indicate the module's network registration mode	-	DO DI	QDSS_TRACEDATA_1A BOOT_CONFIG_1
6	NET_STATUS	DO	P3	Indicate the module's network activity status	-	DO B DO DI	RFE4_CLK SSBI 1 QDSS_TRACEDATA_7B BOOT_CONFIG_11
7	VDD_EXT	PO	-	Provide 1.8V for external circuit	-		
8	GND	GND	-	Ground Pin	-		
9	GND	GND	-	Ground Pin	-		
10	USIM_GND	GND	-	Ground Pin	-		
11	DBG_RXD	DI	P3	Debug UART reception	-	DI DI	UART5_RX SPI_MISO_BLSP5
12	DBG_TXD	DO	P3	Debug UART transmission	-	DO	UART5_TX

						DO	SPI_MOSI_BLSP5
13	USIM_PRESENCE	DI	P3	SIM detect Pin	-	DIO	GPIO_34
14	USIM_VDD	PO	P5	External SIM power	-		
15	USIM_DATA	DIO	P5	External SIM card IO	-	DIO	GPIO_31
16	USIM_CLK	DO	P5	External SIM clock	-	DIO	GPIO_32
17	USIM_RST	DO	P5	External SIM card reset	-	DIO	GPIO_33
18	CODEC_INT	DO	P3	-	-	DO	QDSS_TRACEDATA_14A
19	GND	GND	-	Ground Pin	-		
20	RESET_N	DI	-	Module Reset Control	-		
21	PWRKEY	DI	-	Power key	-		
22	GND	GND	-	Ground Pin	-		
23	SD_INS_DET	DI	P3	SD Card detect pin	-	DIO	GPIO_26
24	PCM_IN	DI	P3	PCM data input	-	B DO DO	MI2S_2_D0 SPI_CS1_N_BLSP3 QDSS_TRACEDATA_2A
25	PCM_OUT	DO	P3	PCM data output	-	B B DO	MI2S_2_D1 SPI_CS1_N_BLSP2 QDSS_TRACEDATA_8A
26	PCM_SYNC	DO	P3	PCM data frame synchronization signal	-	B B DO DI	MI2S_2_WS GP_MN QDSS_TRACEDATA_10A BOOT_CONFIG_7

27	PCM_CLK	DO	P3	PCM clock	-	B DO DO DI	MI2S_2_SCLK SPI_CS1_N_BLSP1 QDSS_TRACEDATA_9A BOOT_CONFIG_8
28	SDC2_DATA3	DIO	P2	SDIO Bus data 3	-	DO DO DO DO	SPI_MOSI_BLSP1 UART1_TX SPI_CS3_N_BLSP3 GP_CLK_2B
29	SDC2_DATA2	DIO	P2	SDIO Bus data 2	-	DI DI DO DO	SPI_MISO_BLSP1 UART1_RX SPI_CS3_N_BLSP2 GP_CLK_3B
30	SDC2_DATA1	DIO	P2	SDIO Bus data 1	-	DO DI B DO	SPI_CS_N_BLSP1 UART1_CTS_N I2C_SDA_BLSP1 GP_CLK_1B
31	SDC2_DATA0	DIO	P2	SDIO Bus data 0	-	DO DO B	SPI_CLK_BLSP1 UART1_RFR_N I2C_SCL_BLSP1
32	SDC2_CLK	DO	P2	SDIO Bus clock	-	DO DO	SPI_MOSI_BLSP4 UART4_TX
33	SDC2_CMD	DIO	P2	SDIO Bus command	-	DI DI	SPI_MISO_BLSP4 UART4_RX

34	VDD_SDIO	PO					
35	RESERVED	-	-	Do not connect	-		
36	GND	GND	-	Ground Pin	-		
37	BT_RTS/UART3_RTS	DI	P3	UART3 Request to send	-	DO B DI	SPI_CLK_BLSP3 I2C_SCL_BLSP3 QDSS_CTI_TRIG1_IN_A
38	BT_TXD/UART3_TX	DO	P3	Data transmission	-	DO B DO	SPI_MOSI_BLSP3 GP_PDM_0B QDSS_TRACEDATA_3A
39	BT_RXD/UART3_RX	DI	P3	Data reception	-	DI B DO	SPI_MISO_BLSP3 GP_PDM_1B QDSS_TRACEDATA_7A
40	BT_CTS/UART3_CTS	DO	P3	UART clear to send	-	DO B B DO	SPI_CS_N_BLSP3 I2C_SDA_BLSP3 GP_PDM_2B QDSS_TRACECLK_A
41	I2C_SCL	DO	P3	I2C clock signal	-	DO DO B DO	UART5_RFR_N SPI_CLK_BLSP5 I2C_SCL_BLSP5 SPI_CS2_N_BLSP2
42	I2C_SDA	DIO	P3	I2C data signal	-	DI DO	UART5_CTS_N SPI_CS_N_BLSP5

						B DO	I2C_SDA_BLSP5 QDSS_TRACEDATA_14B
43	RESERVED	-	-	Do not connect	-		
44	ADC1	AI	P3	Generic ADC	-		
45	ADC0	AI	P3	Generic ADC	-		
46	GND	GND	-	Ground Pin	-		
47	GNSS_ANT	RF_I	-	GNSS Antenna	50Ω impedance		
48	GND	GND	-	Ground Pin	-		
49	ANT_MAIN	RF_IO	-	Main Antenna	50Ω impedance		
50	GND	GND	-	Ground Pin	-		
51	GND	GND	-	Ground Pin	-		
52	GND	GND	-	Ground Pin	--		
53	GND	GND	-	Ground Pin	-		
54	GND	GND	-	Ground Pin	-		
55	RESERVED	-	-	Do not connect	-		
56	GND	GND	-	Do not connect	-		
57	VBAT_RF	PI	-	Power supply for module's RF part	-		
58	VBAT_RF	PI	-	Power supply for module's RF part	-		
59	VBAT_BB	PI	-	Power supply for module's baseband part	-		
60	VBAT_BB	PI	-	Power supply for module's baseband part	-		

61	STATUS	DO	P3	Module ON status	-		
62	UART4_RI	DO	P3	Ring indicator	-	DI DO DI	SD_WRITE_PROTECT QDSS_TRACEDATA_15A BOOT_CONFIG_2
63	UART4_DCD	DO	P3	Data carrier detect	-	B DO	RFFE2_DATA QDSS_TRACEDATA_3B
64	UART4_CTS	DO	P3	Clear to send	-	DO DI B BR DO DO DO	SPI_CS_N_BLSP6 UART6_CTS_N MI2S_1A_D1 I2C_SDA_BLSP6 EBI2_AD_8_B QDSS_TRACEDATA_5A PCM_1_DOUT
65	UART4_RTS	DI	P3	Request to send	-	DO DO B B DO DO DI B	SPI_CLK_BLSP6 UART6_RFR_N MI2S_1A_SCLK I2C_SCL_BLSP6 LCD_CS_N_B QDSS_TRACEDATA_12A BOOT_CONFIG_4 PCM_1_CLK
66	UART4_DTR	DI	P3	Data terminal ready	-	DO DI	SPI_CS_N_BLSP4 UART4_CTS_N

						B DO	I2C_SDA_BLSP4 QDSS_CTI_TRIG1_OUT_A
67	UART4_TXD	DO	P3	Transmit data	-	DO DO B DI DO B DO B	SPI_MOSI_BLSP6 UART6_TX MI2S_1A_WS LCD_TE_B SPI_CS3_N_BLSP1 GP_PDM_0A QDSS_TRACEDATA_13A PCM_1_SYNC
68	UART4_RXD	DI	P3	Receive data	-	DI DI B DO B DO DO DI	SPI_MISO_BLSP6 UART6_RX MI2S_1A_D0 SPI_CS2_N_BLSP1 GP_PDM_1A QDSS_TRACEDATA_4A BACKLIGHT_EN PCM_1_DIN
69	USB_DP	AIO	-	USB differential signal+	-		
70	USB_DM	AIO	-	USB differential signal -	-		
71	USB_VBUS	PI	-	USB power	-		
72	GND	GND	-	Ground Pin	-		
73	MDM_JTAG_SRST_N	DI	P3	JTAG Reset	-		

74	MDM_JTAG_TCK	DI	P3	JTAG Clock input	-		
75	MDM_JTAG_TDO	DO	P3	JTAG Data Output	-		
76	MDM_JTAG_TDI	DI	P3	JTAG Data Input	-		
77	MDM_JTAG_TMS	DIO	P3	JTAG Test Mode	-		
78	MDM_JTAG_TRST_N	DI	P3	JTAG Reset	-		
79	SPI_MISO_BLSP2	DI	P3	SPI Multi In Serial Out	-	DI DI DO	UART2_RX SPI_MISO_BLSP2 QDSS_TRACEDATA_0A
80	SPI_CLK_BLSP2	DO	P3	SPI serial clock	-	DO DO B	UART2_RFR_N SPI_CLK_BLSP2 I2C_SCL_BLSP2
81	SPI_CS_N_BLSP2	DO	P3	SPI Chip select	-	DI DO B DO	UART2_CTS_N SPI_CS_N_BLSP2 I2C_SDA_BLSP2 QDSS_TRACECTL_A
82	SPI_MOSI_BLSP2	DO	P3	SPI Multi Out Serial In	-	DO DO DO	UART2_TX SPI_MOSI_BLSP2 QDSS_TRACEDATA_11A
83	HSIC_STB	B	P8	HSIC strobe	-		
84	HSIC_DATA	B	P8	HSIC data	-		
85	GND	GND	-	Ground Pin	-		
86	GND	GND	-	Ground Pin	-		

87	GND	GND	-	Ground Pin	-		
88	GND	GND	-	Ground Pin	-		
89	GND	GND	-	Ground Pin	-		
90	GND	GND	-	Ground Pin	-		
91	GND	GND	-	Ground Pin	-		
92	GND	GND	-	Ground Pin	-		
93	GND	GND	-	Ground Pin	-		
94	GND	GND	-	Ground Pin	-		
95	GND	GND	-	Ground Pin	-		
96	GND	GND	-	Ground Pin	-		
97	GND	GND	-	Ground Pin	-		
98	GND	GND	-	Ground Pin	-		
99	GND	GND	-	Ground Pin	-		
100	GND	GND	-	Ground Pin	-		
101	GND	GND	-	Ground Pin	-		
102	GND	GND	-	Ground Pin	-		
103	GND	GND	-	Ground Pin	-		
104	GND	GND	-	Ground Pin	-		
105	GND	GND	-	Ground Pin	-		
106	GND	GND	-	Ground Pin	-		
107	GND	GND	-	Ground Pin	-		
108	GND	GND	-	Ground Pin	-		
109	GND	GND	-	Ground Pin	-		
110	GND	GND	-	Ground Pin	-		
111	GND	GND	-	Ground Pin	-		
112	GND	GND	-	Ground Pin	-		
113	SDC_PWR_EN	DO	-	Configurable GPIO	-		

114	GPIO_35	DIO	-	General Purpose IO	-		
115	USB_BOOT	DI	P3	Force USB boot control	-	DI DI	LTE_COEX_RX_UART FORCE_USB_BOOT
116	GPIO_19	DIO	-	General Purpose IO	-		
117	RESERVED	-	-	Do not connect	-		
118	WLAN_SLP_CLK	DO	-	WLAN sleep clock	-		
119	EPHY_RST_N	DO	-	Ethernet PHY reset	-	DO DO DO	UIM2_RESET GP_CLK_3A ETH_RST_N
120	EPHY_INT_N	DI	-	Ethernet PHY Interrupt	-	DI DI	UIM2_DETECT ETH_INT_N
121	SGMII_MDATA	DIO	-	Management Data	-	DO B DO	UIM2_CLK MDIO_DATA GP_CLK_2A
122	SGMII_MCLK	DO	-	Management Data clock reference	-	B DO DO	UIM2_DATA MDIO_CLK GP_CLK_1A
123	SGMII_TX_M	AO	-	SGMII Transmit – Negative	-		
124	SGMII_TX_P	AO	-	SGMII Transmit – Positive	-		
125	SGMII_RX_P	AI	-	SGMII Receive – Positive	-		
126	SGMII_RX_M	AI	-	SGMII Receive – Negative	-		

127	PM_ENABLE	DO	-	External power enable control	-		
128	USIM2_VDD	PO	P5	Power supply for USIM card	-		
129	SDC1_DATA 3	DIO	P2	SDIO data bus (bit 3)	-		
130	SDC1_DATA 2	DIO	P2	SDIO data bus (bit 2)	-		
131	SDC1_DATA 1	DIO	P2	SDIO data bus (bit 1)	-		
132	SDC1_DATA 0	DIO	P2	SDIO data bus (bit 0)	-		
133	SDC1_CLK	DO	P2	SDIO clock signal	-		
134	SDC1_CMD	DIO	P2	SDIO command signal	-		
135	WAKE_ON_ WIRELESS	DI	-	WLAN wake up the module	-	B B DO	RFFE4_DATA SSBI 2 QDSS_TRAC EDATA_12B
136	WLAN_EN	DO	P3	WLAN enable	-	DI DI	QDSS_CTI_T RIG0_IN_A BOOT_CONF IG_12
137	COEX_UART _RX	DI	-	LTE/WLAN& BT coexistence signal	-	DI DI	LTE_COEX_R X_UART FORCE_USB_ BOOT
138	COEX_UART _TX	DO	-	LTE/WLAN& BT coexistence signal	-	DO DI	LTE_COEX_T X_UART 5BOOT_CON FIG_3
139	BT_EN	DO	-	Bluetooth enable control	-		
140	RESERVED	-	-	Do not connect	-		

141	OPTION1	DI	-	Option hardware configuration control	-		
142	RESERVED	-	-	Do not connect	-		
143	RESERVED	-	-	Do not connect	-		
144	RESERVED	-	-	Do not connect	-		

NOTE

- *The module typically has an IO port level of 1.8V (in addition to the SIM, the SIM card port level supports 1.8V).*
- *This module defines the RESERVED pin as a reserved pin. It is recommended to be suspended and must not be used*

3.3 Power interface

The CQ10 module power interface consists of two parts:

- ✓ Two VBAT_RF pins for the module's RF part.
- ✓ Two VBAT_BB pins for module's baseband part

3.3.1 Power Supply Design

The power interface of the CQ10 module is as follows:

Table 3.5 Power Pin Definitions

Power supply							
Pin No.	Definition	IO	Description	Remarks	Min	Typical	Max
57,58	VBAT_RF	PI	Input power pin	Input voltage 3.6~4.5 V	3.6V	3.8V	4.5V

59,60	VBAT_BB	PI	Module input voltage	Input voltage 3.6~4.5 V	3.6V	3.8V	4.5V
7	VDD_EXT	PO	Reference voltage	Output voltage	-	1.8	-

The CQ10 module is powered by a single power supply and the module provides four power supply pins. The power supply range is from 3.6V to 4.5V. It is recommended to use 3.8V power supply. If the module's operating voltage drop causes the VCC supply voltage to be too low or the supply current is insufficient, the module may shut down or restart. Therefore, to reduce the power fluctuation of the module when working, it is necessary to use a low-ESR value of the voltage regulator capacitor, the power pin and the ground pin should be connected and can provide sufficient power supply capability.

Under the premise of ensuring that the VCC power supply is sufficient, two 22uF capacitor can be connected in parallel with the power input, two 0.1uF capacitor (eliminating clock and digital signal interference).

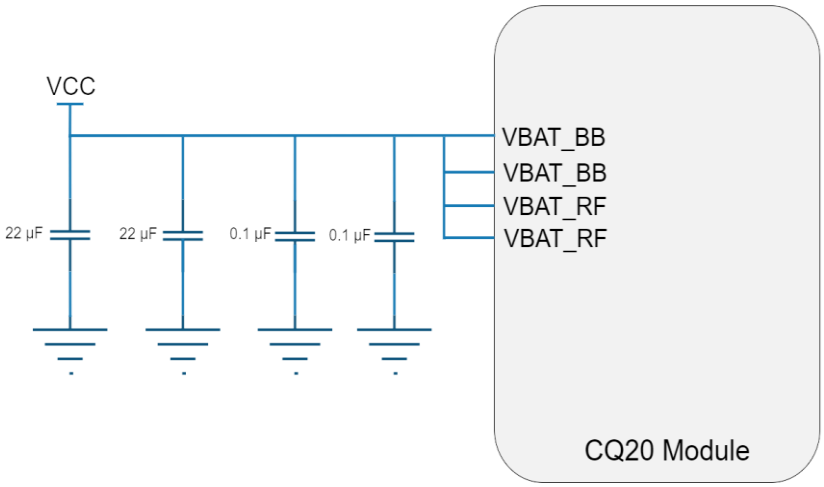

Figure 3 VCC Power Supply

3.3.2 Power Reference Circuit

The power reference circuit is designed with a linear LDO power supply design circuit. The input is filtered with a 22 µF and a 0.1 µF capacitor to minimize noise. The output is smoothed by capacitors (100 µF, 22 µF, and 0.1 µF) to reduce ripple. Both design circuits need to supply enough current. Specific reference to the following circuit design:

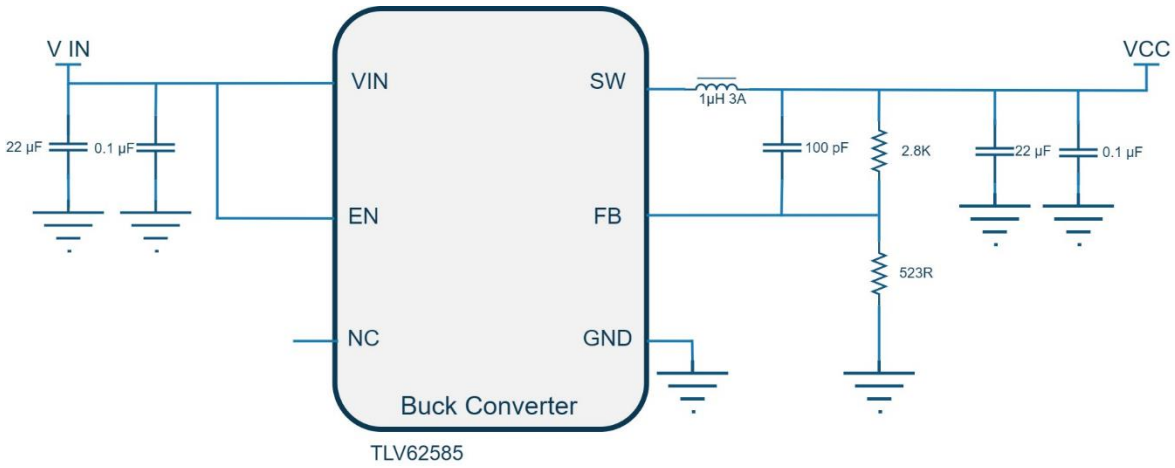

Figure 4 DC Switching Power Supply Reference Circuit

NOTE

- *The minimum operating voltage of the module is 3.6V. Data transmission or calls will generate a current of more than 2, thus a ripple voltage drop will occur on the power supply voltage. Therefore, the actual supply voltage must not be lower than 3.6V.*
- *Due to the large current consumption of the module power pins, it is recommended that the PCB traces be as short as possible. Minimize the equivalent impedance of the VCC trace.*

3.4 Switching Machine Reset Mode

3.4.1 Turn ON Module

The 21nd pin of the CQ10 module is PWRKEY pin. The module can be powered on by pulling down the PWRKEY LOW for at least 500ms.

Table 3.6 Switch Pin Definition

Pin No.	Signal name	I/O	Description
21	PWRKEY	DI	Active Low

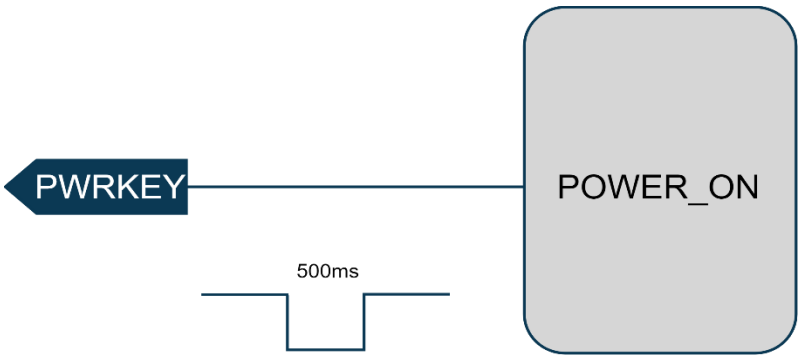

Figure 5 Power-on Reference Circuit

3.4.2 Reset Control

The Pin 20 of CQ10 module Pin is the Reset pin. The application detects that the module is abnormal. When the software does not respond, the module can be reset. Pull the pin low for 100-500ms to reset the module. The RESET pin is sensitive to interference. A 10nF to 0.1uF capacitor can be installed near the signal for signal filtering. Keep away from RF interference signals when routing.

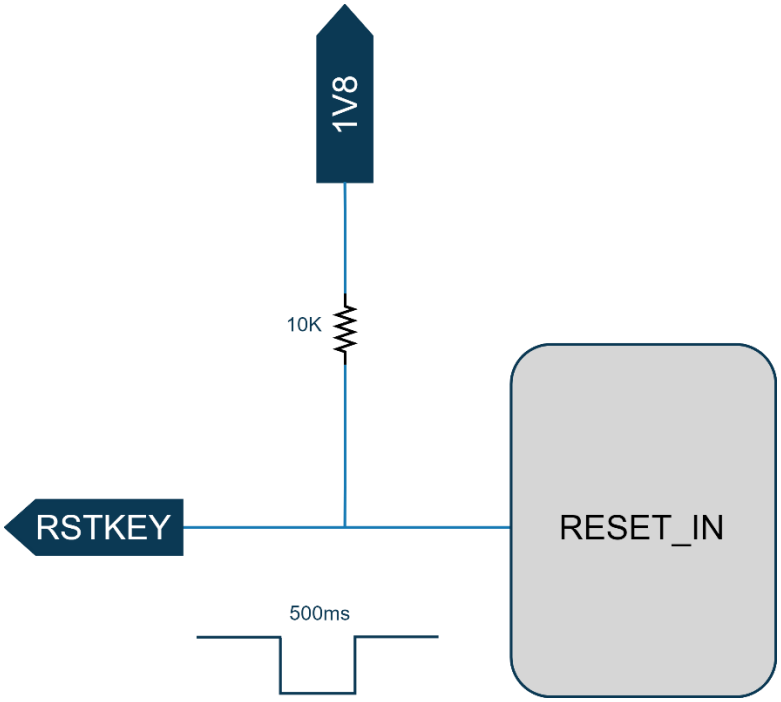

Figure 6 Reset Reference Circuit.

Table 3.7 RESET Pin Parameters

Pin No.	Signal name	I/O	High value	Description
20	RESET_N	DI	VBAT	Module Reset Control

The CQ10 module supports AT command reset, and the AT command is **AT+TRB** to restart the module.

3.5 USB Interface

The CQ10 module USB interface supports *USB2.0* high-speed protocol. The USB interface work as OTG host, therefore it can work as Host and Slave mode and does not support USB charging mode. USB input and output traces must comply with the *USB2.0* Standard. The input power supply of USB_VBUS is 3.3V - 5V. The USB interface is used to update the firmware of the module. The USB interface is defined as follows:

Table 3.8 USB Interface Pin Definition

Pin No.	Signal name	I/O	Description
69	USB_DP	AIO	USB differential signal +
70	USB_DM	AIO	USB differential signal -
71	USB_VBUS	PI	USB power

The module only acts as a USB slave device and supports *USB Sleep* and *Wake-Up* mechanisms. USB interface application reference circuit is as follow:

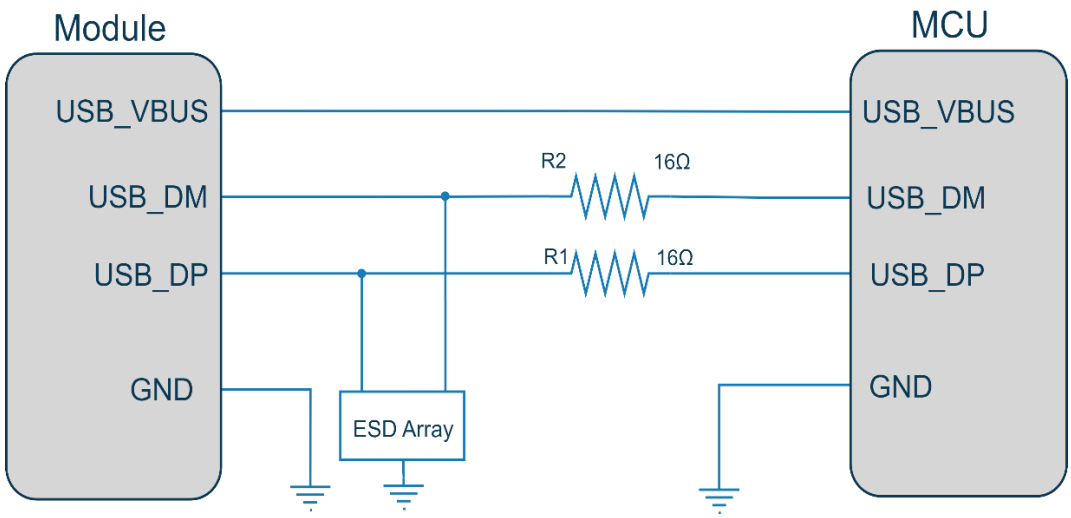

Figure 7 USB connection design circuit diagram

NOTE

- *Required a resistance of 16R for R1/R2.*
- *The USB interface supports high-speed (480Mbps) mode, so the trace design needs to strictly follow the USB2.0 standard protocol requirements, pay attention to the protection of the data line, differential trace, control impedance is 90Ω.*
- *In order to improve the antistatic performance of the USB interface, it is recommended to add an ESD protection device on the data line. The equivalent capacitance of the protection device is less than 2pF.*
- *The USB interface bus supply voltage is provided internally by the module and does not need to be externally supplied. At the same time, since the USB interface of the module does not provide USB bus power, the module can only be used as a slave device of the USB bus device.*

3.6 UART Interface

The CQ10 module provides three sets of UART interfaces. AT port, Debug port and User UART port. The maximum baud rate supported is 4 Mbps.

3.6.1 UART4 (AT UART)

The pins 62, 63, 64,65,66,67 and 68 of the CQ10 module are UART4 serial port pins. Users can use this UART port for communication using AT commands. The default baud rate is 115200 bps. The maximum Baud rate is 4Mbps

The pins are defined as follows ：

Table 3.9 UART4 Serial Port Signal Definition

Pin No.	Signal name	I/O	Description	Voltage		
				V_min	V_Typical	V_max
62	UART4_RI	DO	Ring indicator	1.70 V	1.80 V	1.90 V
63	UART4_DCD	DO	Data carrier detect	1.70 V	1.80 V	1.90 V

64	UART4_CTS	DO	Clear to send	1.70 V	1.80 V	1.90 V
65	UART4_RTS	DI	Request to send	1.70 V	1.80 V	1.90 V
66	UART4_DTR	DO	Data terminal ready	1.70 V	1.80 V	1.90 V
67	UART4_TXD	DO	Transmit data	1.70 V	1.80 V	1.90 V
68	UART4_RXD	DI	Receive data	1.70 V	1.80 V	1.90 V

3.6.2 UART 3 (User UART)

The pins 40,37,38,39 of the module are UART3 serial port pins. The pins are defined as follows:

Table 3.10 UART4 Serial Port Pin Definition

Pin No.	Signal name	I/O	Description	Voltage (V)		
				V_min	V_typical	V_max
37	UART3_RTS/BT_RTS	DI	Request to send	1.70 V	1.80 V	1.90 V
38	UART3_TXD/BT_TXD	DO	Transmit data	1.70 V	1.80 V	1.90 V
39	UART3_RXD/BT_RXD	DI	Receive data	1.70 V	1.80 V	1.90 V
40	UART3_CTS/BT_CTS	DO	Clear to Send	1.70 V	1.80 V	1.90 V

3.6.3 Debug UART

The pins 11 and 12 of the module are UART5 serial port pins. UART5 serial interface can be used for debugging purposes. The default baud rate is 115200 bps. The maximum Baud rate is 4Mbps. The pins are defined as follows:

Table 3.11 Debug UART Serial Port Pin Definition

Pin No.	Signal name	I/O	Description	Voltage		
				V_min	V_typical	V_max
11	DBG_RXD	DI	Transmit data	1.70 V	1.80 V	1.90 V
12	DBG_TXD	DO	Receive data	1.70 V	1.80 V	1.90 V

3.6.4 Serial Port Application Circuit

The serial level is 1.8V.

The module's serial port baud rate can be set to 4800 to 921600bps baud rate and the default is 115200bps.

To use a 2-wire serial port, User may refer to the following serial port design:

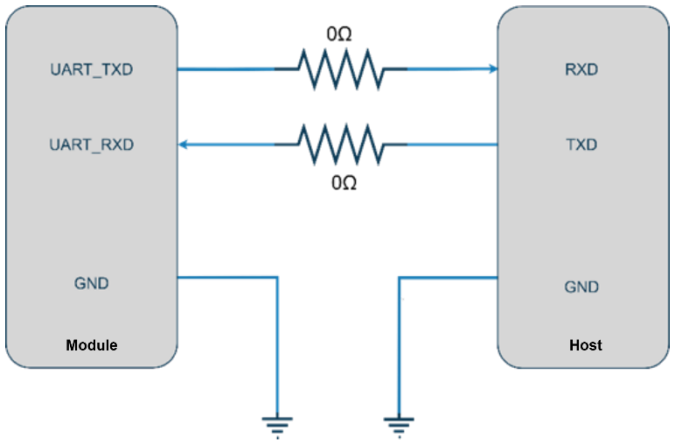

Figure 8 UART Serial Port Design

The serial port of the module is 1.8V level. If the serial port needs to be connected to the MCU of 3.3V level, it is necessary to add a level conversion chip externally to achieve level matching. For the chip connection method, refer to the following circuit, in the schematics we have used an external 1.8V power source for VCCA:

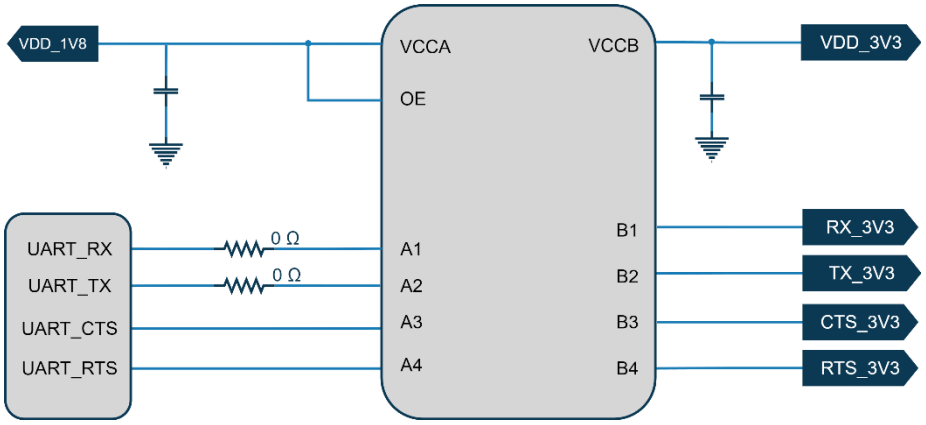

Figure 9 Level Conversion Reference Circuit

3.7 USIM Interface

The CQ10 module provides a USIM card interface compatible with the ISO 7816-3 standard. The USIM card power supply is provided by the module's internal power manager and supports 1.8V/3.0V.

Table 3.12 SIM Card Signal Definition

No	Signal name	I/O	Description	Voltage Level (V)		
				V_min	V_typical	V_max
14	USIM_VDD	PO	External SIM supply	1.70 V / 2.70V	1.80 V / 2.95V	1.90 V / 3.10V
15	USIM_DATA	DIO	External SIM data	1.70 V / 2.70V	1.80 V / 2.95V	1.90 V / 3.10V
16	USIM_CLK	DO	External SIM clock	1.70 V / 2.70V	1.80 V / 2.95V	1.90 V / 3.10V
17	USIM_RST	DO	External SIM reset	1.70 V / 2.70V	1.80 V / 2.95V	1.90 V / 3.10V

13	USIM_PRESENCE	DI	SIM detect Pin	1.70 V / 2.70V	1.80 V / 2.95V	1.90 V / 3.10V
10	USIM_GND	GND	Ground Pin	1.70 V / 2.70V	1.80 V / 2.95V	1.90 V / 3.10V

3.7.1 USIM Card Reference Circuit

The CQ10 module does not come with a USIM card slot. Users need to design a USIM card slot on their own interface board.

The USIM card interface reference circuit is as follows:

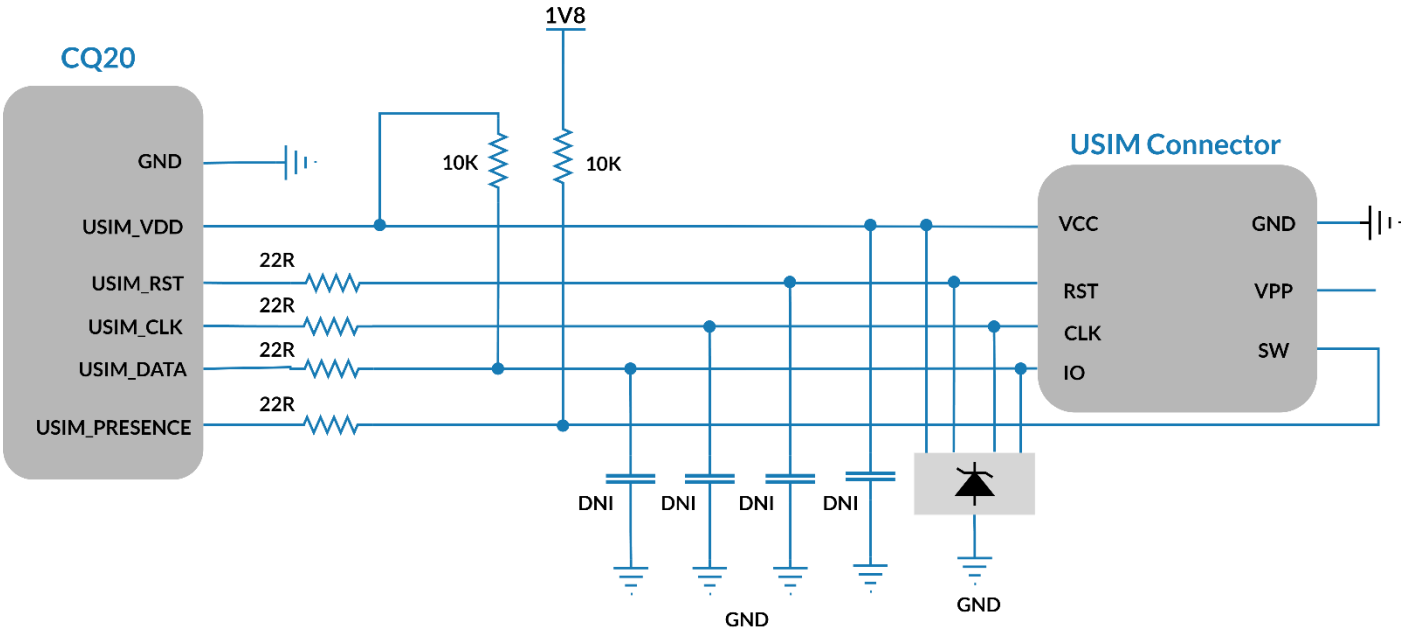

Figure 10 USIM Design Circuit Diagram

NOTE

- *The USIM interface cable is recommended to use ONSEMI's SMF15C device for ESD protection. The peripheral circuit components should be placed close to the card holder. The SIM card holder is close to the module layout.*
- *The USIM card circuit is susceptible to radio frequency interference and does not recognize or drop the card. Therefore, the card slot should be placed as far as possible from the RF radiation of the antenna. The card trace should be as far away as possible from the RF, power supply and high-speed signal lines.*

- *The USIM_DATA has been internally pulled up to 1.8V (only resistor, use an external power source) through a 10K resistor, and no external pull-up is required.*
- *USIM_PRESENCE is high by default. The SIM card status can be detected by this PIN during hot plug application.*
- *To avoid transient voltage overload, the USIM interface requires a 22R resistor in series with each other on the signal line path.*
- *The ground of the USIM deck and the ground of the module should maintain good connectivity.*

3.9 Status Indication Interface

The CQ10 module provides interfaces to indicate module status.

Table 3.13 Definition of Network Indicator Lamp

Pin No.	Signal name	I/O	Description
61	STATUS	DO	Module power on status indication
5	NET_MODE	DO	Indicate the module's network registration status
6	NET_STATUS	DO	Indicate the module's network activity status

Table 3.14 NET_STATUS Indicator State

NETLIGHT Pin	Signal state
Module is not run, or module is not registered	Low
Module registration to network successful	High
Module is scanning for network	Blinking

LED network indicator light reference design chart is as follows:

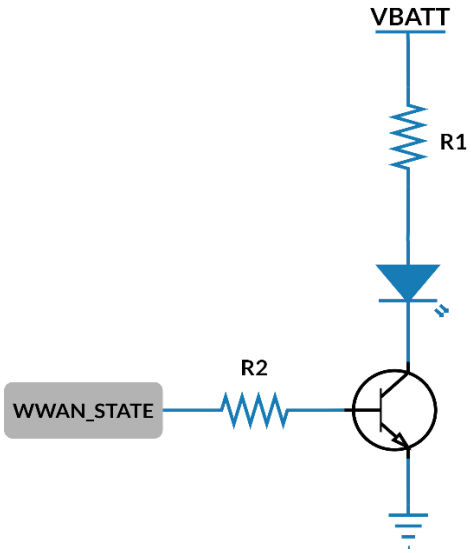

Figure 11 Circuit Diagram of WWAN_STATE pin Indicator

NOTE

- *The resistance value in the circuit diagram of the network indicator can be adjusted according to the LED lamp parameters.*
- *The brightness of the network indicator can be adjusted by adjusting the current limiting resistor R1.*

3.10 PCM digital voice Interface

CQ10 module provides a set of PCM audio interfaces supporting 8-bit A-rate, U-rate and 16-bit linear short frame encoding formats with PCM_SYNC of 8 kHz and PCM_CLK of 2048 kHz.

Table 3.15 PCM Pin Definition

Pin No.	Signal name	I/O	Description	Voltage Level (V)		
				V_min	V_typical	V_max
24	PCM_IN	DI	PCM data input	1.70 V	1.80 V	1.90 V

25	PCM_OUT	DO	PCM data output	1.70 V	1.80 V	1.90 V
26	PCM_SYNC	DIO	PCM frame sync signal	1.70 V	1.80 V	1.90 V
27	PCM_CLK	DIO	PCM clock pulse	1.70 V	1.80 V	1.90 V

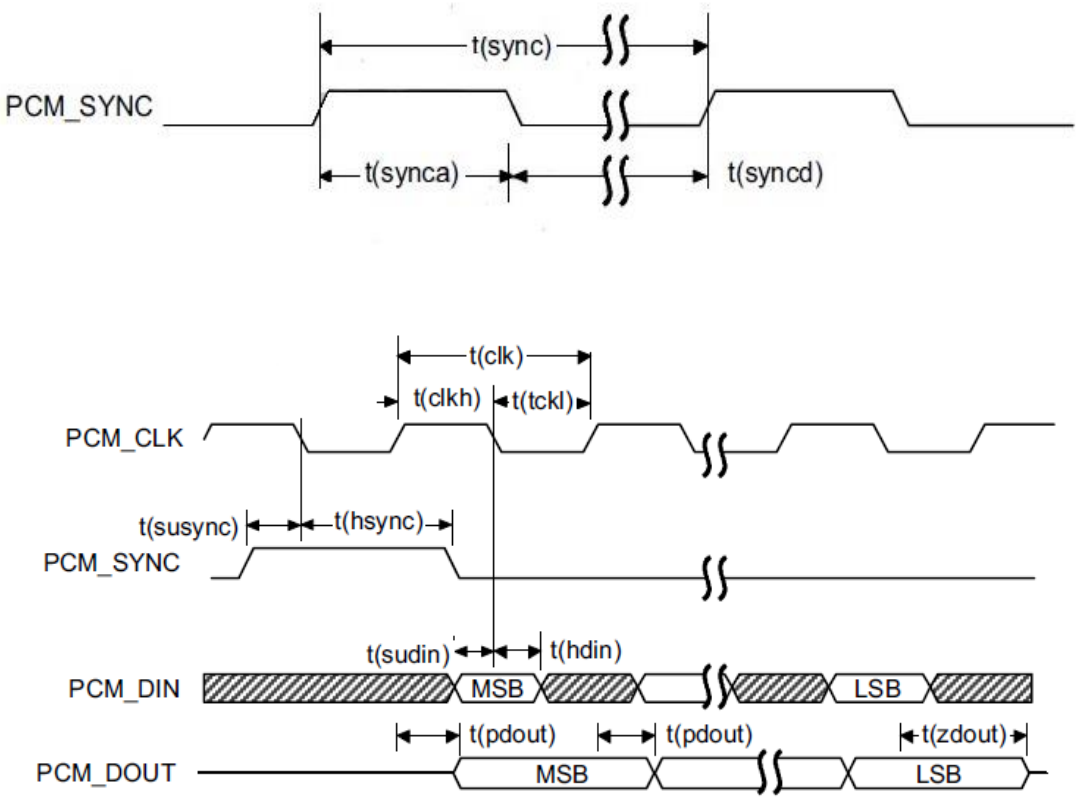

Figure 12 PCM Short Frame Mode Timing Diagram

Table 3.16 PCM Specific Parameters

Characteristic	Description
Encoding format	Linear
Data bit	16bits
Master-slave mode	Master/slave mode

PCM clock	2048kHz
PCM frame synchronization	Short frame
Data Format	MSB

The recommended circuit for PCM to analog voice is as follows:

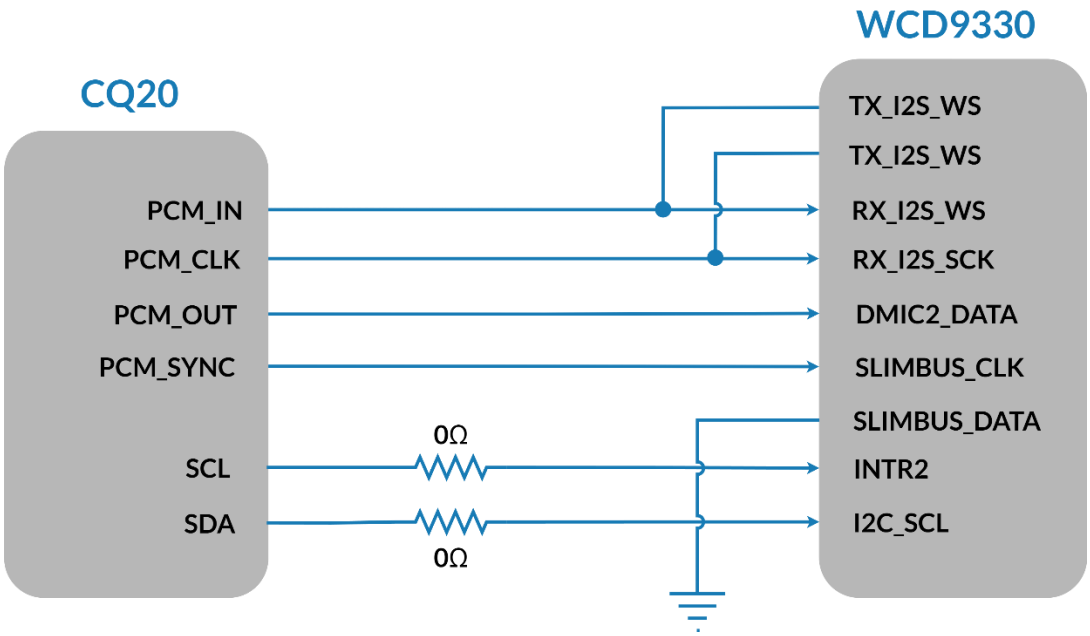

Figure 13 PCM to Analog Voice Map

3.11 I2C Bus

The CQ10 module provides a set of hardware bidirectional serial buses with an I2C interface of 1.8V level, a *5.0 Protocol* interface, and a clock rate of 400 KHz.

Table 3.17 I2C Pin Definition

Pin No.	Signal name	I/O	Description	Level value (V)		
				min	typical	max
41	I2C_SCL	DO	I2C bus clock output	1.70V	1.80V	1.90V

42	I2C_SDA	DIO	I2C bus data input and output	1.70V	1.80V	1.90V

The I2C reference circuit is connected as follows:

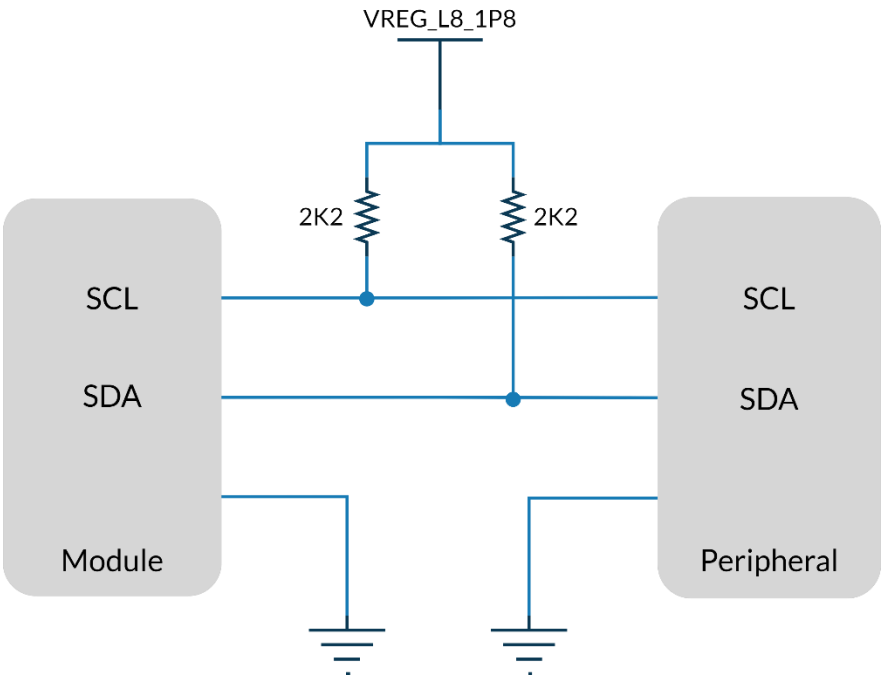

Figure 14 I2C Interface Reference Circuit Diagram

3.12 SDC Interface

CQ10 module provides a set of 4-bit SDC interface, supports SD3.0 protocol, supports two voltage SD cards of 1.8V / 2.95V, clock frequency up to 50MHz, maximum capacity supports 32GB. Provide VREF voltage for SDIO power supply.

Table 3.18 SDC Interface Pin Definitions

Pin No.	Pin name	IO	Definition
31	SDC2_DATA0	DIO	SD card SDIO bus DATA0
30	SDC2_DATA1	DIO	SD card SDIO bus DATA1
29	SDC2_DATA2	DIO	SD card SDIO bus DATA2

28	SDC2_DATA3	DIO	SD card SDIO bus DATA3
32	SDC2_CLK	DO	SD card SDIO bus clock
33	SDC2_CMD	DIO	SD card SDIO bus command
34	VDD_SDIO	PO	SDIO Pull up power source for SD card
23	SD_INS_DET	DI	SD Card detect pin

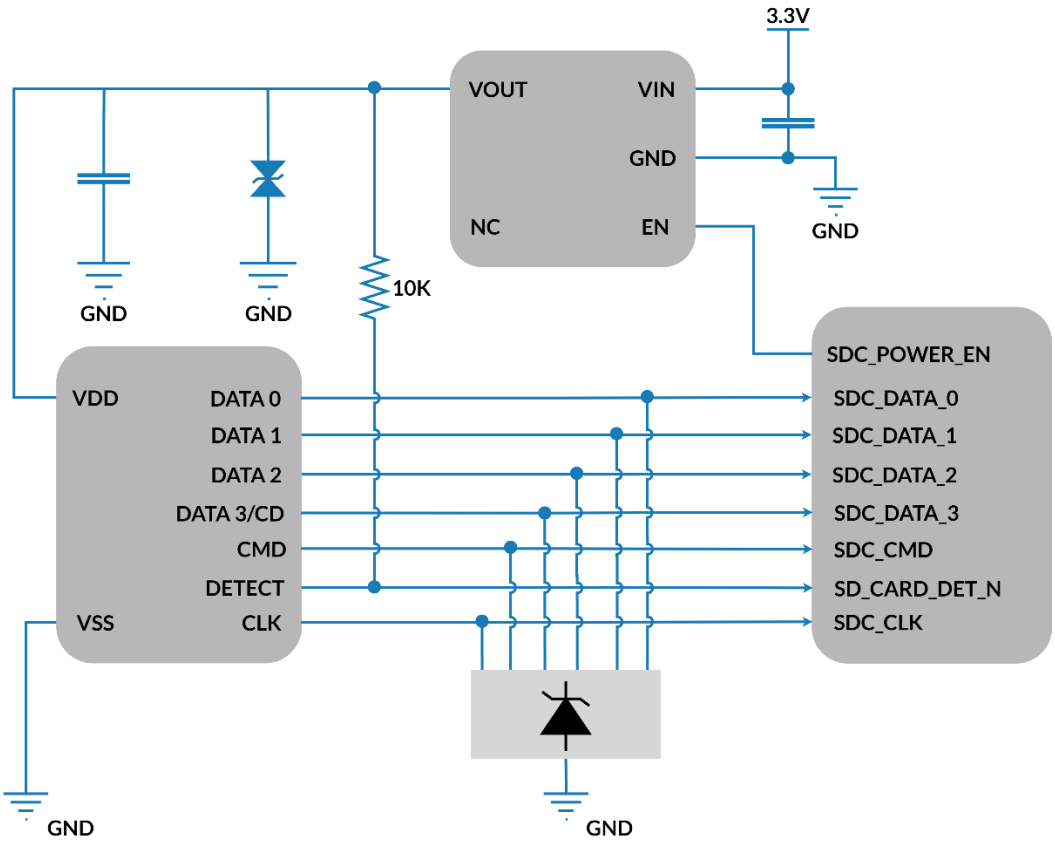

Figure 15 SDC Interface Reference Circuit Diagram

3.13 Antenna

The CQ10 module provides two antenna interfaces, a main antenna interface, which is responsible for the LTE and GSM signals of the transceiver module and a GNSS antenna interface.

The GNSS antenna interface supports **L1**.

The impedance of the antenna interfaces are 50 ohms.

Table 3.19 Antenna Interface Pin Definition

Pin No.	Signal Name	IO	Description	Remarks
49	ANT_MAIN	RF_IO	Main antenna interface	50Ω characteristic impedance
47	GNSS_ANT	RF_I	GNSS L1 antenna interface	50Ω characteristic impedance

The pin-49 of the CQ10 is the main antenna interface

To facilitate the debugging of the antenna, a **π**-type matching circuit needs to be added to the main board, and a 50-ohm impedance line is taken.

Recommended circuit is shown below：

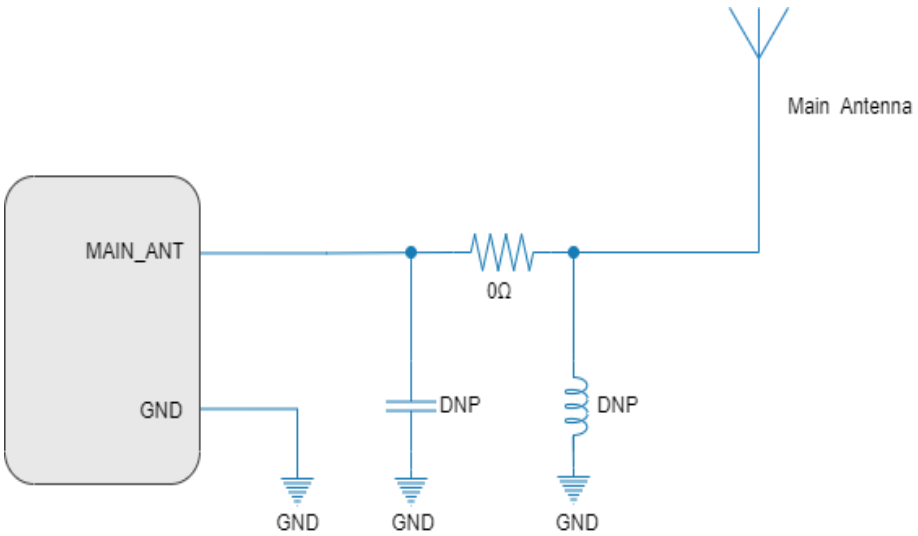

Figure 16 Main Antenna Matching Circuit

The pin 47 of CQ10 is the GNSS antenna interface.

The CQ10 has a dedicated antenna **L1**, it supports GPS, GLONASS, BEIDOU, QZSS, Galileo.

QZSS and SBAS Ranging support available.

In order to facilitate antenna debugging, a **π**-type matching circuit needs to be added to the motherboard and a 50-ohm impedance line is used.

NOTE

- *The GNSS antenna needs to maintain a certain distance from the main antenna.*
- *The GNSS antenna has two antenna connection mode:*

  Passive antenna mode and Active antenna mode
- *External power needs to be provided since the module itself cannot supply power to GNSS Active antenna.*

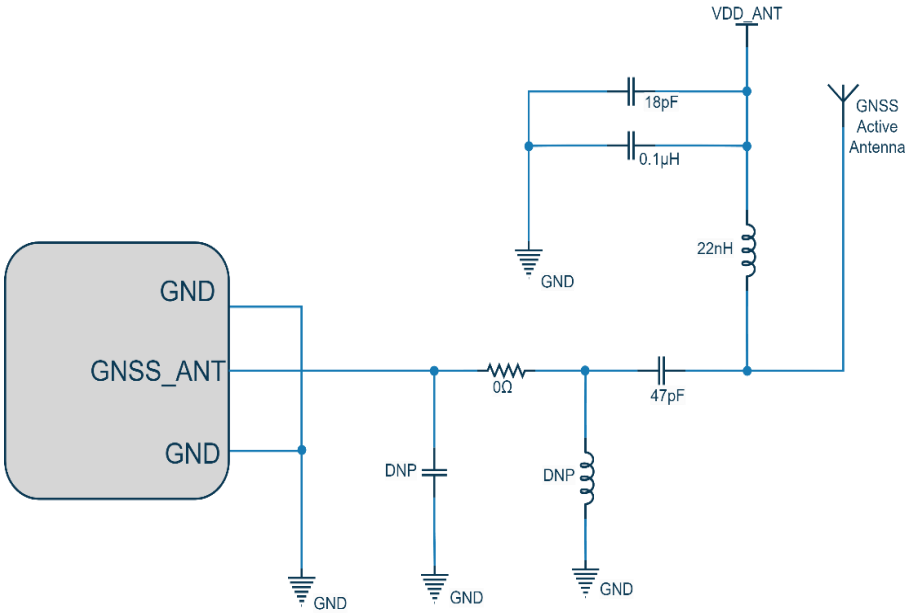

Figure 17 GNSS Active Antenna Matching Circuit

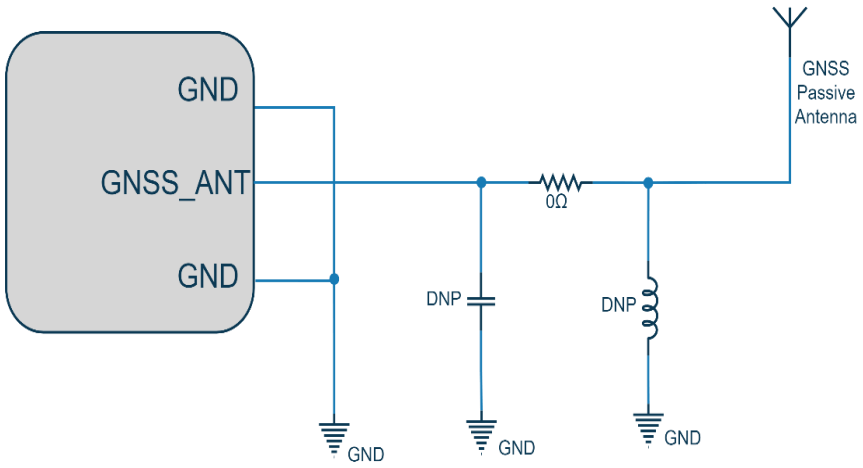

Figure 18 GNSS Antenna Matching Circuit

NOTE

- *An external LDO can be selected to supply power according to the active antenna requirement.*
- *If the module is designed with a passive antenna, then the VDD circuit is not needed.*
- *The LTE_MAIN antenna is distributed reasonably to improve the receiving sensitivity.*
- *In actual use, the antenna board can be debugged and optimized according to the user's circuit board.*
- *Antenna impedance traces need to be away from digital signal lines, power supplies and other interference signals.*
- *The antenna impedance traces need to be three-dimensionally packaged, and the ground holes are added on both sides of the trace to isolate.*

3.13.1 RF Trace Reference

The main set of the CQ10 module are extracted by pad. The antenna pad to the antenna feed point must use microstrip lines or other types of RF traces. The characteristic impedance of the signal line should be controlled at 50Ω.

The impedance of the RF signal line is determined by the material's dielectric constant, trace width (W), ground clearance (S), and reference ground plane height (H). Therefore, the RF trace requires an impedance simulation tool to calculate the impedance of the RF trace.

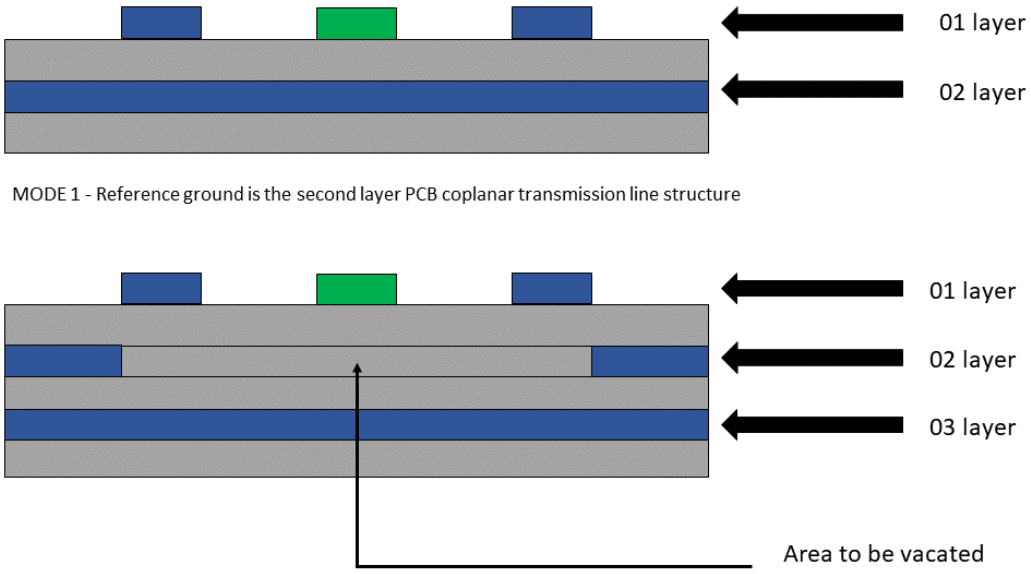

Figure 19 Coplanar Antenna

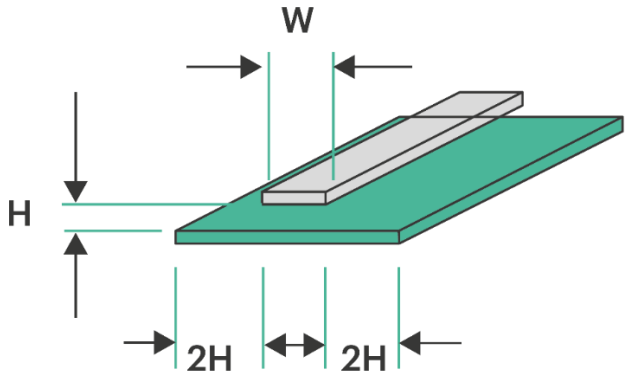

Figure 20 The Complete Structure of the Two-Layer PCB Microstrip Line

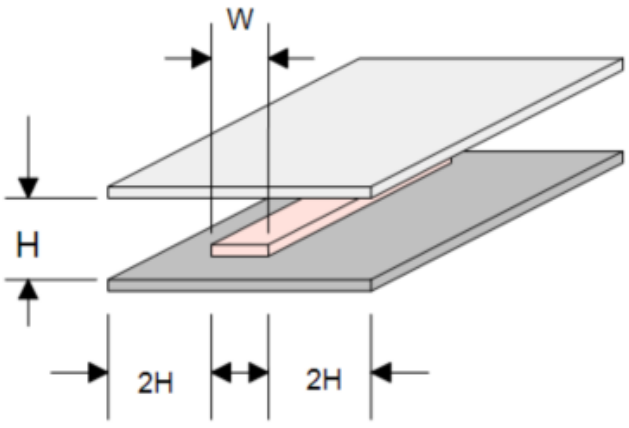

Figure 21 The Complete Structure of the Multilayer PCB Strip Line

NOTE

- *Since Coplanar antennas are having maximum noise immunity, it is preferred.*

3.14 Coexistence and Control Interface

Different module interfaces are available in module.

Table 3.20 Control Interface Pin Definition

Pin No.	Signal name	I/O	Description
127	PM_ENABLE	DO	External power enable control
135	WAKE_ON_WIRELESS	DI	WLAN wake up the module
137	COEX_UART_RX	DI	LTE/WLAN & BT coexistence signal
138	COEX_UART_TX	DO	LTE/WLAN&BT coexistence signal
118	WLAN_SLP_CLK	DO	WLAN sleep clock
1	WAKEUP_IN	DI	Module wake up
61	STATUS	DO	Module power on status indication

WAKEUP_IN:

WAKEUP_IN wakeup the device after entering sleep mode via AT command or by default it goes to sleep mode in some cases.

STATUS:

This pin is used to get the status of the module.

3.15 SGMII Interface

The SGMII interface is a serial interface featuring a low pin count that can be configured for ethernet.

Table 3.21 SGMII Interface Pin Definition

Pin No.	Signal name	I/O	Description
123	SGMII_TX_M	AO	SGMII Transmit - Negative
124	SGMII_TX_P	AO	SGMII Transmit - Positive
125	SGMII_RX_P	AI	SGMII Receive - Positive
126	SGMII_RX_M	AI	SGMII Receive - Negative
119	EPHY_RST_N	DO	Ethernet PHY reset
120	EPHY_INT_N	DI	Ethernet PHY Interrupt
121	SGMII_MDATA	DIO	Management Data
122	SGMII_MCLK	DO	Management Data clock reference

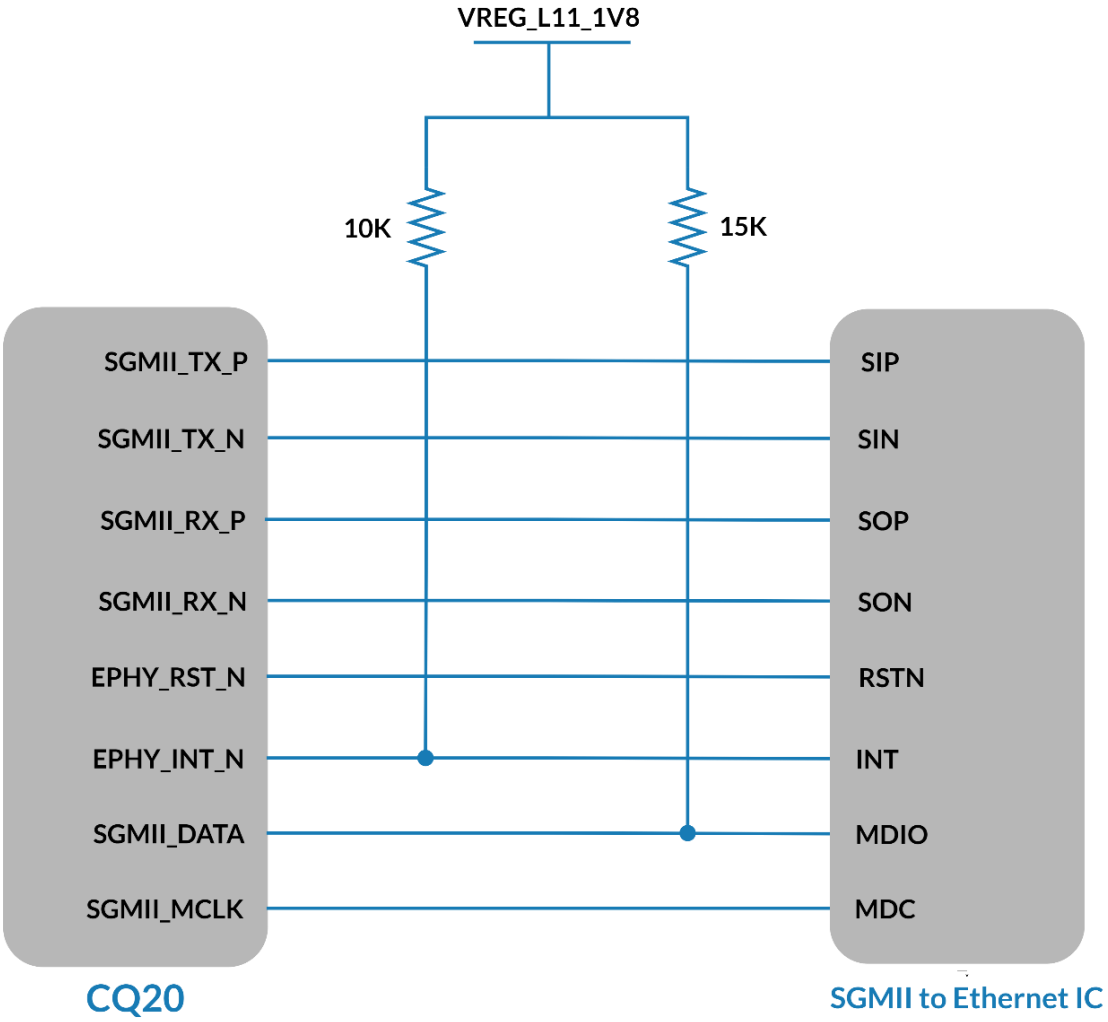

Figure 22 Ethernet (SGMII) Interface Reference Circuit Diagram

3.16 GNSS Interface

Multi – GNSS receiver:

- ✓ **L1** multi-band GNSS receiver
- ✓ Multi-Constellation GPS/GLONASS/Galileo/Bei Dou/QZSS.

Table 3.22 GNSS Antenna Pin Definition

Pin No.	Signal name	I/O	Description
47	GNSS_ANT	AI	GNSS L1 antenna interface

3.17 ADC interface

ADC interface converts the analog signals to digital signals which can be understood by the device. The module provides 2 Analog to Digital Converter interface.

Table 3.23 ADC Interface Pin Definition

Pin No.	Signal name	I/O	Description
45	ADC 0	AI	Generic ADC
44	ADC 1	AI	Generic ADC

3.18 JTAG interface

The JTAG interface is used to troubleshoot the device and evaluate its functionality.

Table 3.24 WLAN Interface Pin Definition

Pin No.	Signal name	I/O	Description
74	MDM_JTAG_TCK	DO	Test clock
77	MDM_JTAG_TMS	DI	Test mode select

76	MDM_JTAG_TDI	DI	Test data input
75	MDM_JTAG_TDO	DO	Test data output
73	MDM_JTAG_SRST_N	DI	System Reset
78	MDM_JTAG_TRST_N	DI	Test Reset

3.19 GPIO interface

The CQ10 module contains two general purpose control signals. The interface is defined as follows

Table 3.25 WLAN Interface Pin Definition

Pin No.	Signal name	I/O	Description
114	GPIO_35	DIO	General Purpose Pin
116	GPIO_19	DIO	General Purpose Pin

3.20 WLAN and Bluetooth Applications Interfaces

The following table shows the pin definition of WLAN application interfaces.

Table 3.26 WLAN Interface Pin Definition

Pin No.	Signal name	I/O	Description
129	SDC1_DATA3	DIO	SDIO data bus (bit 3)
130	SDC1_DATA2	DIO	SDIO data bus (bit 2)
131	SDC1_DATA1	DIO	SDIO data bus (bit 1)
132	SDC1_DATA0	DIO	SDIO data bus (bit 0)
133	SDC1_CLK	DO	SDIO clock signal
134	SDC1_CMD	DIO	SDIO command signal
136	WLAN_EN	DO	WLAN function enable

The following table shows the pin definition of Bluetooth application interfaces for interfacing an external Bluetooth chipset.

Table 3.27 Bluetooth Interface Pin Definition

Pin No.	Signal name	I/O	Description
37	BT_RTS	DI	Request to send
38	BT_TXD	DO	Transmit Data
39	BT_RXD	DI	Receive Data
40	BT_CTS	DO	Clear to send
24	PCM_IN	DI	PCM data input
25	PCM_OUT	DO	PCM data output
26	PCM_SYNC	DIO	PCM data frame synchronization signal
27	PCM_CLK	DIO	PCM clock pulse
139	BT_EN	DO	Bluetooth function enable

4 Overall Technical Indicators

4.1 Chapter Overview

The CQ10 module RF overall specifications include the following sections:

- ✓ Working frequency
- ✓ Antenna requirements

4.2 Working Frequency

Table 4.1 RF Frequency Table

Frequency band	Uplink frequency	Downstream frequency	Mode
LTE B1	1920 MHz–1980 MHz	2110 MHz–2170 MHz	FDD
LTE B2	1850 MHz– 1910 MHz	1930 MHz– 1990 MHz	FDD
LTE B3	1710 MHz–1785 MHz	1805 MHz–1880 MHz	FDD
LTE B4	1710 MHz– 1755 MHz	2110 MHz– 2155 MHz	FDD
LTE B5	824 MHz–849 MHz	869 MHz–894 MHz	FDD
LTE B7	2500MHz – 2570MHz	2620MHz – 2690MHz	FDD

LTE B8	880 MHz–915 MHz	925 MHz–960 MHz	FDD
LTE B12	698 MHz-716 MHz	728 MHz-746 MHz	FDD
LTE B13	777 MHz – 787 MHz	746 MHz – 756 MHz	FDD
LTE B18	815 MHz - 830 MHz	860 MHz - 875 MHz	FDD
LTE B19	830 MHz - 845 MHz	875 MHz - 890 MHz	FDD
LTE B20	832 MHz– 862 MHz	791 MHz– 821 MHz	FDD
LTE B25	1850 MHz – 1915 MHz	1930 MHz – 1995 MHz	FDD
LTE B26	814 MHz – 849 MHz	859 MHz – 894 MHz	FDD
LTE B28	703 MHz - 748 MHz	758 MHz - 803 MHz	FDD
LTE B40	1880 MHz-1920 MHz	1880 MHz-1920 MHz	TDD
LTE B66	2110 MHz – 2200MHz	1710 MHz – 1780 MHz	FDD
GSM 900	880 MHz-915 MHz	925 MHz-960 MHz	GSM
GSM 1800	1710 MHz-1785 MHz	1805 MHz-1880 MHz	GSM

4.3 Antenna Requirements

CQ10 Module Antenna Design Requirements:

Table 4.2 Antenna Indicator Requirements

Frequency band	Standing wave ratio	Antenna gain	Effectiveness	TRP	TIS
B1 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B2 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B3 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B4 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B5 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88

B7 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B8 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B12 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B13 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B18 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B19 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B20 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B25 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B26 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B28 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B40 TDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B66 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
GSM 900	<2:1	〉-2.5dbi	〉40%	>29	<-102
GSM 1800	<2:1	〉-2.5dbi	〉40%	>26	<-102

5 Interface Electrical Characteristics

5.1 Chapter Overview

- Working storage temperature
- Electrostatic property
- Module IO level
- Power supply
- Power consumption characteristics

5.2 Working Storage Temperature

Table 5.1 CQ10 Module Working Storage Temperature

Parameter	Minimum	Typical	Maximum
Device operating temperature	-30°C	25°C	+85°C
3GPP2-mode operating temperature (ambient)	-30°C	25°C	60°C
3GPP-mode operating temperature (ambient)	-20°C	25°C	60°C

5.3 Electrostatic Property

There is no overvoltage protection inside the CQ10 module.

The ESD protection is required when the module is used to ensure product quality.

ESD design recommendations:

✓ The USB port needs to add TVS on VDD, D+, D- for protection, and the TVS parasitic capacitance on D+/D- is <2pF

- ✓ The module's USIM card external pin needs to be protected by TVS, and the parasitic capacitance requirement is <10pF
- ✓ The PCB layout of the protective device should be as close as possible to the "V" line to avoid the "T" line
- ✓ The ground plane around the module guarantees integrity and should not be split
- ✓ ESD control of the surrounding environment and operators is required during module production, assembly and laboratory testing

Table 5.2 CQ10 ESD Features

Test port	Contact discharge	Air discharge	Unit
USB interface	±4	±8	KV
USIM interface	±4	±8	KV
VBAT power supply	±4	±8	KV

5.4 Module IO Level

The CQ10 module IO levels are as follows:

Table 5.3 Electrical Characteristics of CQ10 Module

Parameter	Description	Minimum	Maximum
VIH	High level input voltage	0.65*VIO	VIO+0.3V
VIL	Low level input voltage	0.3V	0.35*VIO
VOH	High level output voltage	VIO-0.45V	VIO
VOL	Low level output voltage	0	0.45V

5.5 Power Supply

The CQ10 module input power requirements are as follows:

Table 5.4 CQ10 module Operating Voltage

Parameter	Minimum value	Typical value	Maximum value
Input Voltage	3.6V	3.8V	4.5V

The power-on time of any interface of the module must not be earlier than the boot time of the module, otherwise the module may be abnormal or damaged.

6 Structural and Mechanical Properties

6.1 CQ10 module mechanical size

The figure below shows the top and bottom view of the module.

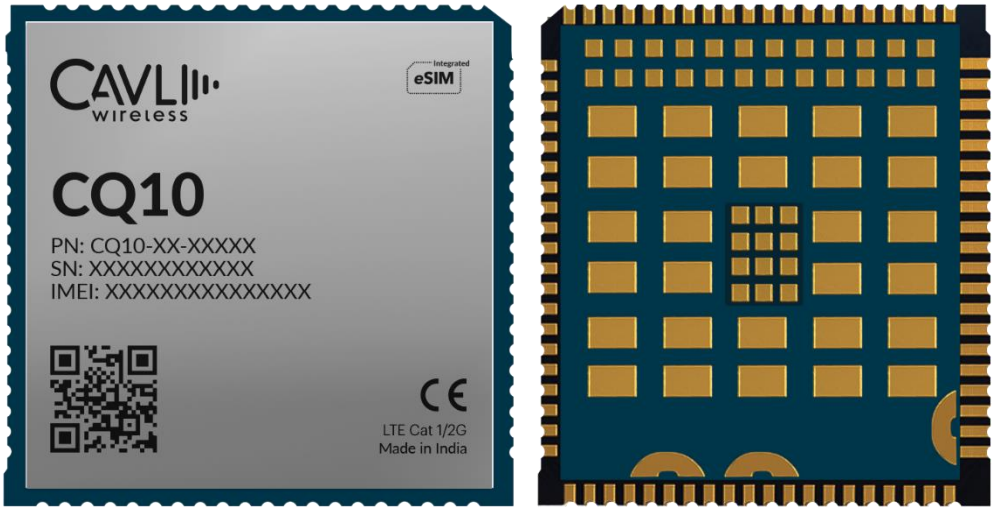

Figure 23 Top View and Bottom View of The Module

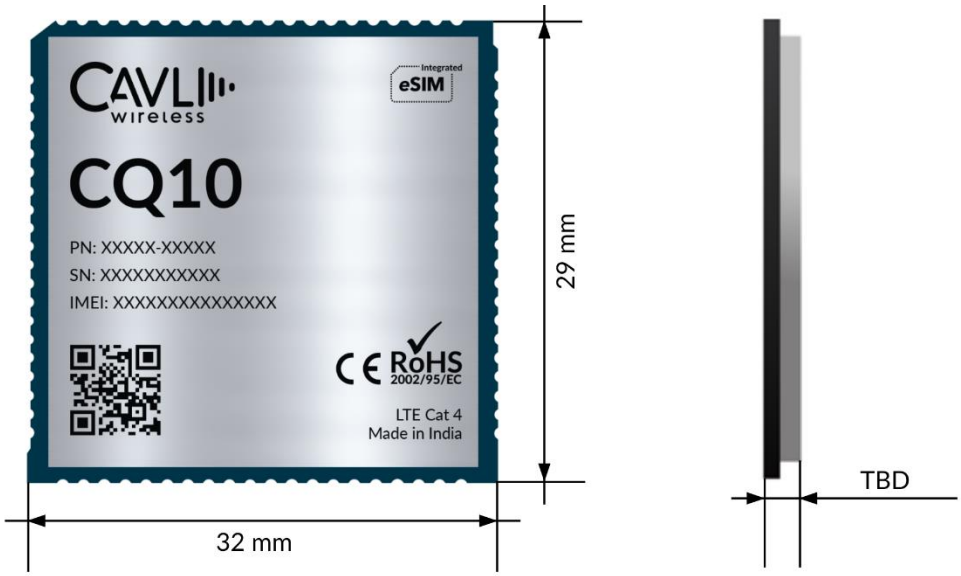

Figure 24 CQ10 Module Dimensions

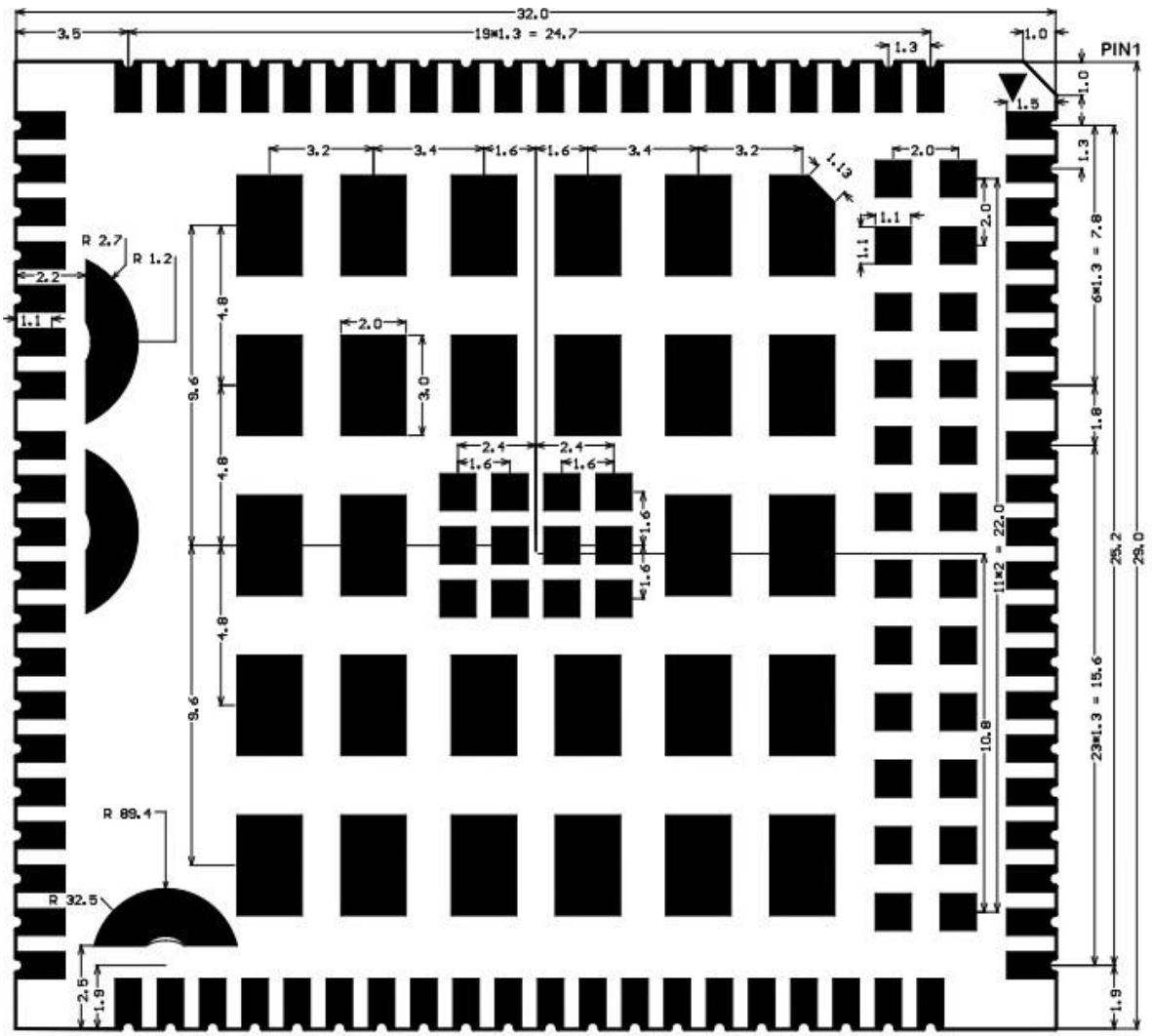

Figure 25 Pad Dimensions (Bottom view)

7 Appendix

7.1 Chapter Overview

- ✓ Abbreviations
- ✓ Safety and precautions

7.2 Abbreviations

Table 7.1 Abbreviations

Abbreviations	Full name
3GPP	Third Generation Partnership Project
AP	Access Point
AMR	Adaptive multi-rate
BER	Bit Error Rate
CCC	China Compulsory Certification
CDMA	Code Division Multiple Access
CE	European Conformity
CSD	Circuit Switched Data
CTS	Clear to Send
DC	Direct Current
DTR	Data Terminal Ready
DL	Down Link

DTE	Data Terminal Equipment
DRX	Discontinuous Reception
EDGE	Enhanced Data Rate for GSM Evolution
EU	European Union
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FCC	Federal Communications Commission
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communication
HSDPA	High-Speed Downlink Packet Access
HSPA	Enhanced High Speed Packet Access
HSUPA	High Speed Up-link Packet Access
IMEI	International Mobile Equipment Identity
LED	Light-Emitting Diode
LTE	Long Term Evolution
NC	Not Connected
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PMU	Power Management Unit
PPP	Point-to-point protocol
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of the Use of Certain Hazardous Substances
SMS	Short Message Service

TIS	Total Isotropic Sensitivity
TVS	Transient Voltage Suppressor
TX	Transmitting Direction
UART	Universal Asynchronous Receiver-Transmitter
UMTS	Universal Mobile Telecommunications System
USIM	Universal Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WWAN	Wireless Wide Area Network

7.3 Safety and Precautions

In order to use the wireless device safely, the terminal device informs the user of the relevant safety information:

- ✓ **Interference:** When the use of wireless devices is prohibited or the use of the device may cause interference and security of the electronic device, turn off the wireless device. Because the terminal will send and receive RF signals when it is powered on. It can interfere with TV, radio, computer or other electrical equipment.
- ✓ **Medical equipment:** In medical and health care facilities where the use of wireless devices is prohibited in the express text, please follow the regulations of the site and turn off the device. Some wireless devices may interfere with the medical device, causing the medical device to malfunction or cause errors. If interference occurs, turn off the wireless device and consult a physician.
- ✓ **Flammable and explosive areas:** In flammable and explosive areas, please turn off your wireless device and follow the relevant label instructions to avoid an explosion or fire. For example; gas stations, fuel zones, chemical products areas, chemical transportation and storage facilities, areas with explosion hazard signs, areas with “turn off radio equipment” signs, etc.
- ✓ **Traffic Safety:** Please comply with local laws or regulations in your country or region regarding the use of wireless devices when driving a vehicle.
- ✓ **Aviation Safety:** When flying, please follow the airline's regulations and regulations regarding the use of wireless devices. Before taking off, turn off the wireless device to prevent wireless signals from interfering with aircraft control signals.
- ✓ **Environmental Protection:** Please comply with local laws regarding the handling of equipment packaging materials, equipment or accessories, and support recycling operations.
- ✓ **Emergency call:** This device uses wireless signals for propagation. Therefore, there is no guarantee that the network can be connected in all situations, so in an emergency this wireless device cannot be used as the only contact method.