Re-imagining Cellular IoT Solutions

Cavli C20QM
LTE CAT 4 /2G Module

Hardware Manual

External Release Version 2.2

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Version	Edit	Release Date
1.0	• Initial Version	16-08-2023
1.1	• Updated reference circuits ○ VCC Power Supply ○ DC Switching Power Supply Reference Circuit ○ Power-on Reference Circuit ○ Reset Reference Circuit ○ USIM Design Circuit Diagram ○ Circuit Diagram of Network Indicator ○ I2C Interface Reference Circuit Diagram ○ USB connection design circuit diagram • Added Reference Circuits ○ SDC Interface Reference Circuit Diagram ○ Main Antenna Matching Circuit Diagram ○ Ethernet Interface Reference Circuit Diagram ○ LCD Interface Reference Circuit Diagram	29-09-2023
1.2	• Updated Pin Interface Table	17-10-2023
1.3	• Changes in diagrams of UART, Power reference circuit	13-11-2023
1.4	• Updated Pad dimensions	17-11-2023
1.5	• Updated uSIM Card reference circuit	12-12-2023
1.6	• Updated Pin Interface Table	09-12-2024
1.7	• Updated Pin alternate functions	07-05-2024

1.8	• Updated power consumption details and GNSS performance details	08-05-2024
1.9	• Updated the power consumption characteristics	21-08-2024
2.0	• Updated module information	29-08-2024
2.1	• Updated band list	11-12-2024
2.2	• Updated band list	03-01-2025

1 Introduction

This document is the **Hardware Manual** of the Cavli Wireless solution product **C20QM Module**, which describes:

- ✓ The hardware composition and functional features of the module
- ✓ The definition and usage of the application interface
- ✓ The electrical performance and mechanical properties of the module

This document and the other application documents combined will enable users to develop end devices with Cavli Modules.

2 Module Overview

2.1 Module Introduction

C20QM module integrates an application processing subsystem, a communication subsystem, multimedia, and connectivity peripherals to enable a single chip 4G LTE feature phone solution.

The C20QM communication subsystem integrates **LTE CAT 4** technology, **GSM** Modem Baseband, and an RF transceiver to cover bands B2 /B4 /B5 /B12 /B13 /B17 /B25 /B66 /GSM 900/ GSM 1800 (**N.A**), B1 / B3 /B5 /B7 /B8 /B18 /B19 /B20 /B26 /B28 /B38 /B40 /B41 /GSM 900/ GSM 1800 (**EAJ**), B1/ B3/ B7/ B8/ B20/ B28 /GSM 900/ GSM 1800 (**E.U**) , B1/ B3/ B5/ B8/ B40/ B41/ GSM 900/ GSM 1800 (**I.N**), B1/ B3/ B5/ B8/ B18/ B19/ B26/ B28 /GSM 900/ GSM 1800 (**A.N**)for world-wide roaming. LTE CAT 4 is compliant with 3GPP E-UTRA Release 10.

The application subsystem runs on a single ARM Cortex A7 processor at 1.3GHz with integrated peripherals for connectivity and multimedia.

The C20QM module can be used in the following applications

- ✓ Vehicle telematics
- ✓ Asset tracking
- ✓ Fleet management
- ✓ Smart city and smart home applications
- ✓ Connected retail applications- point of sale devices, automated teller machines, vending machines etc.
- ✓ Industrial IoT - gateways, remote control & monitoring systems

2.2 Module Characteristics

Table 2.1 Key Features

Characteristics		Description
Physical Characteristics		37mm x 21.8mm x 2.8mm
Fixed Way		LGA package, patch mount
Operating Voltage		3.4V – 4.5V Typical Voltage 3.8 V
Application Processor		ARM Cortex A7 with 1.3GHz clock with 256KB L2 Cache
Operating System		Linux 4.14
Memory		256 MB RAM, 256/ 512 MB Flash
Pin Count		233
Application Interface	USIM card	Supports 1.8V/2.85V. Supports hot swap function
	USB	✓ USB2.0 (480Mbps) ✓ USB can function as both master and slave ✓ OTG Host mode support
	UART	✓ UART3(4 line), UART4(2 line) and UART5(2 line) ✓ AT commands and data transfer ✓ The max baud rate is up to 4Mbps. Default is 115200bps.
	PCM	✓ For audio, external codec chip ✓ Support short frame mode. ✓ Support main mode
	SDIO	✓ Compliant with SDIO 3.0 protocol ✓ Comply with IEEE 802.11 standard
	SDC	✓ Compliant with SDIO 3.0 protocol ✓ 4-bit SDC ✓ Can be interfaced with Wi-Fi Transceiver
	I2C	✓ Compliant with I2C bus protocol ✓ High speed mode supports 3.3Mbps rate

	ADC	✓ 2 ADC lines
	Network Indication	✓ WWAN_STATE network status indication ✓ STATUS Module status
	GPIO	✓ 9 GPIO Interfaces
	LCD	✓ 1 MIPI_DBI LCD interface
	GNSS	✓ GPS, GLONASS, BEIDOU, GALILEO, QZSS
	SPI	✓ Standard SPI interface
	Ethernet	✓ SGMII interface
Frequency Band		**N.A:** LTE BANDS: B2/B4/B5/B12/B13/B17/B25/B66 GSM BANDS: GSM900/ GSM1800 **E.U:** LTE BANDS: B1/B3/B7/B8/B20/B28 GSM BANDS: GSM900/ GSM1800 **E.A.J:** LTE BANDS: B1/B3/B5/B7/B8/B18/B19/B20/B26/B28/B38/B40/B41 GSM BANDS: GSM 900/ GSM 1800 **I.N:** LTE BANDS: B1/B3/B5/B8/B40/B41 GSM BANDS: GSM 900/ GSM 1800 **A.N:** LTE BANDS: B1/B3/B5/B8/B18/B19/B26/B28 GSM BANDS: GSM 900/ GSM 1800

Data Network	✓ FDD/TDD LTE CAT 4/2G ✓ Peak DL 150Mbps/ UL 50Mbps (CAT 4) ✓ Peak DL 236.8Kbps/ UL 236.8 Kbps (2G)
AT Command	✓ Specific AT Query C20QM AT command set
Network Protocol	TCP/HTTP/MQTT/HTTP/HTTPS/MQTTS/FTP/FTPS/PPP/SNMP /Web Socket protocols
Antenna Interface	✓ MAIN x 1 ✓ GNSS × 1 ✓ DIV x 1 ✓ Characteristic impedance 50 Ω
Virtual Network Card	Supports USB virtual network card
Temperature Range	Normal working temperature: - 30℃ to +85℃
Humidity	RH5%～RH95%
Module Function Distinction	**M** on the model number represents the multi-mode

NOTE

- When the temperature is in the range of −30°C to −20°C or +75°C to +85°C, some RF specifications of the C20QM module may not meet the 3GPP standards.

2.3 Module Function

C20QM Module mainly consists of the following circuit units:

- ✓ Baseband processing unit
- ✓ Power Management unit
- ✓ Memory unit
- ✓ RF Transceiver unit
- ✓ RF front-end unit
- ✓ RF Band SAW Duplex array
- ✓ Multi-Band PA

✓ Interfaces

The functional block diagram of C20QM module is shown below：

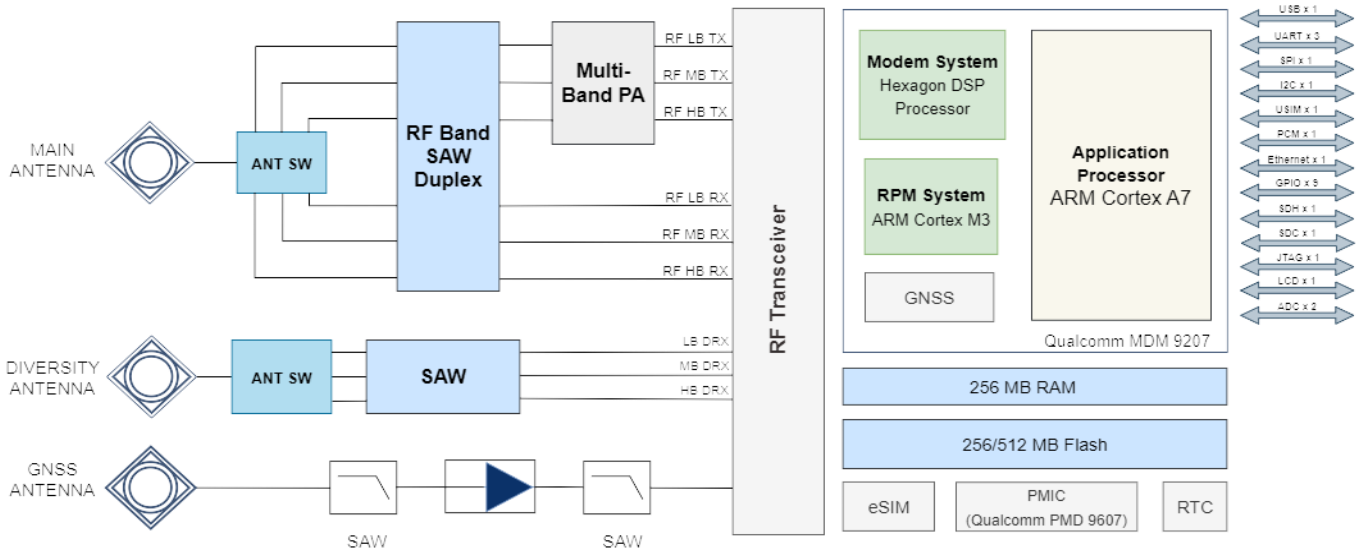


Figure 1 C20QM Functional Block Diagram

2.4 Module Working Mode

Table 2.2 Working Mode

Working Mode	Description
Turn off the machine	In the case of shutdown, the module is fully powered off.
Flight Mode	The module closes the module RF circuit, unable to interact with the network
Dormancy	The module closes most functions, and it will synchronize with the network.
Ideal State	Turn on the machine and register the network successfully, in the idle state
Data transmission	The module is in working state and has data interaction with the network.

3 Interface Application Description

3.1 Chapter Overview

This chapter mainly describes the interface definition and application of this module. It contains the following sections:

- Module Interface
- Power Interface
- Switching Machine Reset Mode
- USB Interface
- UART Interface
- USIM Interface
- GPIO Interface
- Network Status Indicator Interface
- PCM Digital Voice Interface
- I2C Bus
- ADC interface
- JTAG Interface
- Antenna
- Control Interface
- GNSS Interface
- SPI Interface
- SDIO Interface
- SGMII Interface
- LCD Interface

3.2 Module Interface

3.2.1 C20QM Pin Layout

C20QM pins (Top View) are assigned as follows：

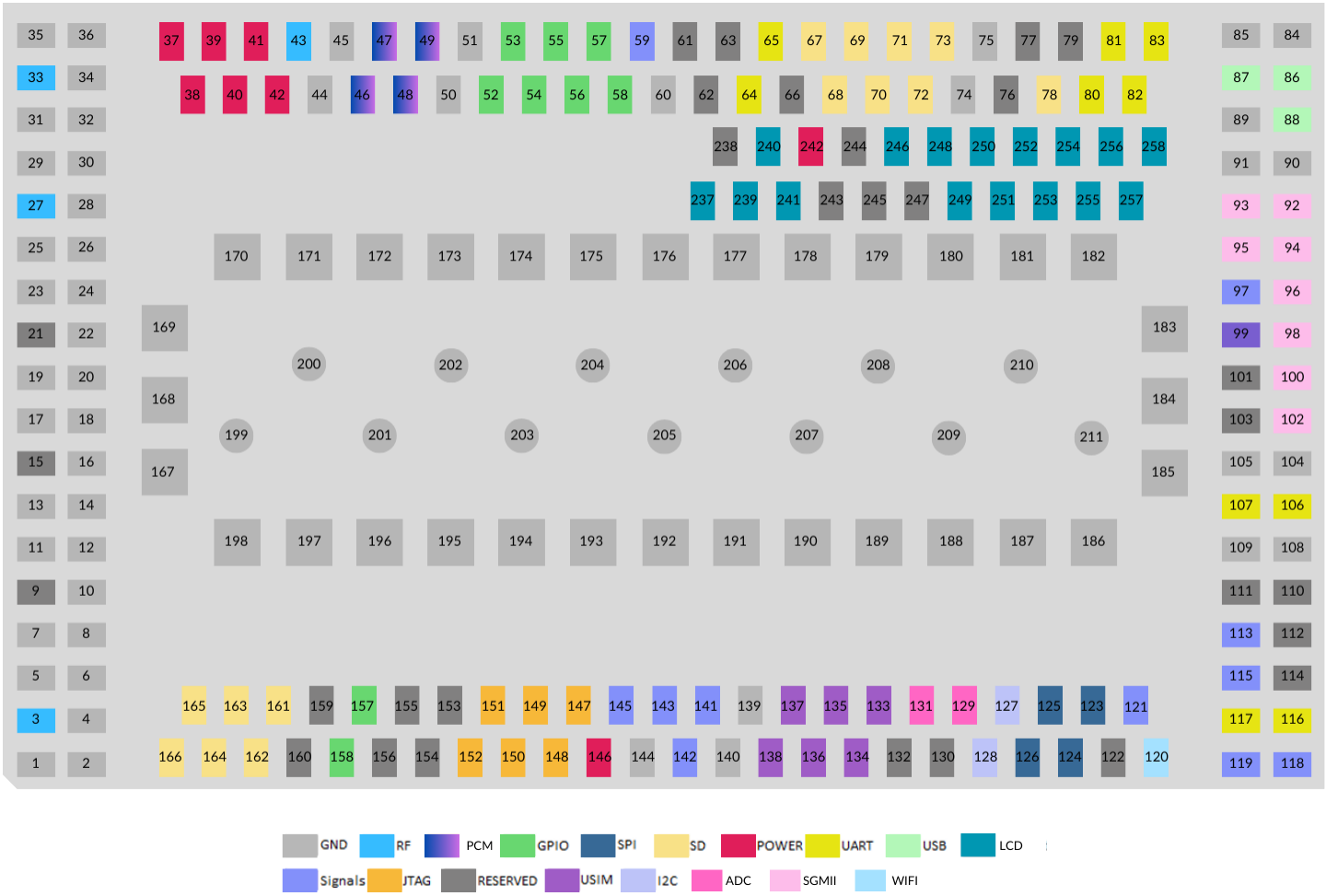


Figure 2 C20QM module Interface definition (Top view)

NOTE

- All RESERVED and unused pin feet need to be left floating

3.2.2 C20QM Pin Interface

The C20QM module has the LGA interface. The module interface definition is shown in the following table:

Table 3.1 Pin Description

Pin Type	Description
PAD TYPE	
AI	Analog Input
AO	Analog Output
B	Bidirectional digital with CMOS input
DI	Digital Input (CMOS)
DO	Digital Output (CMOS)
DIO	Digital Input/Output
OD	Open Drain
H	High voltage tolerant
Z	High Impedance output
PI	Power Input
PO	Power Output
PIO	Power Input/Output
Pad pull details	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpupk = default no-pull with programmable option following the colon (:) PD: pdpupk = default pull-down with programmable option following the colon (:) PU: pdpupk = default pull-up with programmable option following the colon (:) KP: pdpupk = default keeper with programmable option following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device

3.2.3 Absolute maximum ratings

The absolute maximum ratings table reflects the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Operating conditions.

Table 3.2 Absolute Maximum ratings

Pin Type	V_min	V_max
P2	-0.3 V	3.41 V
P3	-0.3 V	2.09 V
P5	-0.3 V	3.41 V
P6	-0.3 V	3.25 V
VB	-0.3 V	4.5 V

3.2.4 Operating Conditions

The operating voltages are listed below.

Table 3.3 Operating Condition

Pin Type	V_min	V_typical	V_max
P2	1.70 V / 2.70V	1.80 V / 2.95V	1.90 V / 3.10 V
P3	1.70 V	1.80 V	1.90 V
P5	1.70 V / 2.70 V	1.80 V / 2.95V	1.90 V / 3.10 V
P6	1.6 V/ 2.75 V	1.80 V / 2.85V	1.93 V / 3.04 V
VB	3.40 V	3.80 V	4.50 V

3.2.5 Pin Descriptions

Table 3.4 Pin Name

Pin No.	Pin Name	IO Type	Configurable Functions	Voltage Definition	Pin Description	Comments
1	GND	GND		-	Ground Pin	-
2	GND	GND		-	Ground Pin	-
3	ANT_MAIN	IO		-	Main Antenna	50Ω impedance
4	GND	GND		-	Ground Pin	-
5	GND	GND		-	Ground Pin	-
6	GND	GND		-	Ground Pin	-
7	GND	GND		-	Ground Pin	-
8	GND	GND		-	Ground Pin	-
9	RESERVED	-		-	Do not connect	-
10	GND	GND		-	Ground Pin	-
11	GND	GND		-	Ground Pin	-
12	GND	GND		-	Ground Pin	-
13	GND	GND		-	Ground Pin	-
14	GND	GND		-	Ground Pin	-
15	RESERVED	-		-	Do not connect	-
16	GND	GND		-	Ground Pin	-
17	GND	GND		-	Ground Pin	-
18	GND	GND		-	Ground Pin	-
19	GND	GND		-	Ground Pin	-
20	GND	GND		-	Ground Pin	-
21	RESERVED	-		-	Do not connect	-

22	GND	GND		-	Ground Pin	-
23	GND	GND		-	Ground Pin	-
24	GND	GND		-	Ground Pin	-
25	GND	GND		-	Ground Pin	-
26	GND	GND		-	Ground Pin	-
27	ANT_DIV	IO		-	Diversity Antenna	50 Ω impedance
28	GND	GND		-	Ground Pin	-
29	GND	GND		-	Ground Pin	-
30	GND	GND		-	Ground Pin	-
31	GND	GND		-	Ground Pin	-
32	GND	GND		-	Ground Pin	-
33	GNSS_L1	AI		-	GNSS Antenna	50Ω impedance
34	GND	GND		-	Ground Pin	-
35	GND	GND		-	Ground Pin	-
36	GND	GND		-	Ground Pin	-
37	VCC1	PI		VB	Module input power supply	-
38	VCC2	PI		VB	Module input power supply	-
39	VCC3	PI		VB	Module input power supply	-
40	VCC4	PI		VB	Module input power supply	-
41	VCC5	PI		VB	Module input power supply	-
42	VCC6	PI		VB	Module input power supply	-

43	RESERVED	-		-	Do not connect	-
44	GND	GND		-	Ground Pin	-
45	GND	GND		-	Ground Pin	-
46	PCM_SYNC	IO	GPIO_79	P3	PCM data frame synchronization signal	Pin should not be high before completing bootup.
47	PCM_DIN	DI	GPIO_76 SPI3_CS1_N	P3	PCM data input	-
48	PCM_DOUT	DO	GPIO_77 SPI2_CS1_N	P3	PCM data output	-
49	PCM_CLK	IO	GPIO_78 SPI1_CLK SPI1_CS1_N	P3	PCM Clock	Pin should not be high before completing bootup
50	GND	GND		-	Ground Pin	-
51	GND	GND		-	Ground Pin	-
52	GPIO_42	DIO	SPI1_CS_N	P3	Configurable I/O Pin	--
53	GPIO_43	DIO	SPI1_MISO	P3	Configurable I/O Pin	Pin should not be high before completing bootup
54	GPIO_44	DIO	SPI1_MOSI	P3	Configurable I/O Pin	Pin should not be high before completing bootup
55	GPIO_45	DIO	SP4_MOSI	P3	Configurable I/O Pin	-
56	GPIO_46	DIO	SPI4_MISO	P3	Configurable I/O Pin	-
57	GPIO_47	DIO	SPI2_MOSI	P3	Configurable I/O Pin	-

58	GPIO_52	DIO	SPI3_CS2_N	P3	Configurable I/O Pin	-
59	WAKEUP_IN	DI		P3	Hardware interrupt to wake up from sleep	Active low input for 500ms
60	RESERVED	-		-	Do not connect	-
61	RESERVED	-		-	Do not connect	-
62	RESERVED	-		-	Do not connect	-
63	RESERVED	-		-	Do not connect	-
64	UART3_RX	DI	GPIO_1 SPI3_MISO	P3	UART3 reception	-
65	UART3_TX	DO	GPIO_0 SPI3_MOSI	P3	UART3 transmission	-
66	RESERVED	-		-	Do not connect	-
67	SDH_D0	IO	GPIO_15 UART1_RTS_N SPI1_CLK I2C1_SCL	P3	SDIO data 0	-
68	SDH_D1	IO	GPIO_14 UART1_CTS_N SPI1_CS_N I2C1_SDA	P3	SDIO data 1	-
69	SDH_D2	IO	GPIO_13 UART1_RX SPI1_MISO SPI2_CS3_N	P3	SDIO data 2	-
70	SDH_D3	IO	GPIO_12 UART1_TX SPI1_MOSI SPI3_CS3_N	P3	SDIO data 3	-
71	SDH_CLK	DO	GPIO_16 UART4_TX SPI4_MOSI	P3	SDIO bus clock	-
72	SDH_CMD	IO	GPIO_17 UART4_RX SPI4_MISO	P3	SDIO bus command	-

73	SDH_PWR_EN	PO		P3	SDIO bus pull up power	-
74	GND	GND		-	Ground Pin	-
75	GND	GND		-	Ground Pin	-
76	RESERVED	-		-	Do not connect	-
77	RESERVED	-		-	Do not connect	-
78	SD_CARD_DET_N	DI	GPIO_26 SPI3_CS2_N	P3	SD CARD Insertion detect	Default pullup to 1.8
79	RESERVED	-		-	Do not connect	-
80	UART3_RTS	DI	GPIO_3 SPI3_CLK I2C3_SCL	P3	UART3 Request to send	-
81	UART3_CTS	DO	GPIO_2 SPI3_CS_N I2C3_SDA	P3	UART3 Clear to send	-
82	DBG_UART_RX	DI		P3	Debug UART reception	-
83	DBG_UART_TX	DO		P3	Debug UART transmission	-
84	GND	GND		-	Ground Pin	-
85	GND	GND		-	Ground Pin	-
86	USB_HS_P	IO		-	Differential Data bus (+)	-
87	MDM_USB_ID	AI		-	ID pin for USB	Connected to ID pin of Micro USB slot (Pull up for slave mode)
88	USB_HS_N	IO		-	Differential Data bus (-)	-
89	GND	GND		-	Ground Pin	-

90	GND	GND		-	Ground Pin	-
91	GND	GND		-	Ground Pin	-
92	MDIO_CLK	DO	GPIO_27	P6	SGMII MDIO Clock	-
93	EPHY_INT_N	DI	GPIO_30	P3	Ethernet PHY interrupt	-
94	MDIO_DATA	IO	GPIO_28	P6	SGMII MDIO data	-
95	EPHY_RST_N	DO	GPIO_29	P6	Ethernet PHY reset	-
96	SGMII_RX_N	AI		-	SGMII reception (-)	-
97	WLAN_EN	DO	GPIO_38	P3	WLAN enable	-
98	SGMII_RX_P	AI		-	SGMII reception (+)	-
99	CODEC_INT	DO	GPIO_75	P3	Codec Initialization	-
100	SGMII_TX_N	AO		-	SGMII Transmission (-)	-
101	RESERVED	-		-	Do not connect	-
102	SGMII_TX_P	AO		-	SGMII transmission (+)	-
103	RESERVED	-		-	Do not connect	-
104	GND	GND		-	Ground Pin	-
105	GND	GND		-	Ground Pin	-
106	UART4_RX	DI		P3	UART4 Reception	-
107	UART4_TX	DO		P3	UART4 Transmission	-
108	GND	GND		-	Ground Pin	-
109	GND	GND		-	Ground Pin	-

110	RESERVED	-		-	Do not connect	-
111	RESERVED	-		-	Do not connect	-
112	RESERVED	-		-	Do not connect	-
113	STATUS	DO		P3	Module status indication Pin	Outputs High signal
114	RESERVED	-		-	Do not connect	-
115	FLIGHT	DI	GPIO_41	P3	Hardware interrupt for Flight mode	Active low input for 500ms
116	BOOT_USB_N	DI	GPIO_37 LTE_COEX_RX_UART	P3	Interrupt for EDL	Pin should not be high before completing bootup
117	COEX_UART_TX	DO	GPIO_36	P3	Coex UART transmission	-
118	WIFI_EXT_PWR_EN	DO		P3	Wifi external power enable	-
119	BT_EN	DO		P3	Bluetooth enable	-
120	WIFI_SLEEP_CLK	DO		P3	Wifi sleep clock	-
121	WAKE_ON_WIRELESS	DO	GPIO_59	P3	Wakeup signal	-
122	RESERVED	-		-	Do not connect	-
123	SPI_CS	DO	GPIO_6 UART2_CTS I2C2_SDA	P3	SPI Chip select	-
124	SPI_MOSI	DO	GPIO_4 UART2_TX	P3	SPI Multi Out Serial In	-
125	SPI_MISO	DI	GPIO_5 UART2_RX	P3	SPI Multi In Serial Out	-
126	SPI_SCLK	DO	GPIO_7 UART2_RTS	P3	SPI serial clock	-

127	I2C_SCL	OD	GPIO_11 UART5_RTS SPI5_CLK SPI2_CS2_N	P3	I2C clock signal	-
128	I2C_SDA	OD	GPIO_10 UART5_CTS_N SPI5_CS_N	P3	I2C data signal	-
129	ADC1	AI		P3	Generic ADC	-
130	RESERVED	-		-	Do not connect	-
131	ADC2	AI		P3	Generic ADC	-
132	RESERVED	-		-	Do not connect	-
133	UIM1_POWER	PO		P5	USIM card power supply	-
134	UIM1_DATA	IO	GPIO_31	P5	USIM Data	-
135	UIMI_CLK	DO	GPIO_32	P5	USIM clock	-
136	UIM1_RESET	DO	GPIO_33	P5	USIM reset	-
137	UIM1_PRESENT	DI	GPIO_34	P3	USIM detection	-
138	USIM_SELECT	DO	GPIO_35	P3	USIM selection	-
139	GND	GND		-	Ground Pin	-
140	GND	GND		-	Ground Pin	-
141	WWAN_STATE	DO		P3	Network registration status	-
142	POWER_ON_IN	DI		-	Module power key	500ms pull down
143	RESET_OUT_N	DO		P3	Reset output	-
144	RESERVED	-		-	Do not connect	-
145	RESET_IN	DI		-	Module reset key	-
146	VREF_OUT_1V8	DI		P3	Module output voltage	-

147	JTAG_TCK	DI		P3	JTAG Clock Input	-
148	JTAG_TMS	IO		P3	JTAG Mode select input	-
149	JTAG_TDI	DI		P3	JTAG Data input	-
150	JTAG_TDO	DO		P3	JTAG Data output	-
151	MDM_JTAG_SRST_N	DI		P3	JTAG Reset for debug	-
152	MDM_JTAG_TRST_N	DI		P3	JTAG Reset	-
153	RESERVED	-		-	Do not connect	-
154	RESERVED	-		-	Do not connect	-
155	RESERVED	-		-	Do not connect	-
156	RESERVED	-		-	Do not connect	-
157	GPIO_24	DIO		P3	Configurable I/O Pin	Pin should not be high before completing bootup
158	GPIO_25	DIO		P3	Configurable I/O Pin	Pin should not be high before completing bootup
159	RESERVED	-		-	Do not connect	-
160	RESERVED	-		-	Do not connect	-
161	SDC2_CLK	DO		P2	SDIO Bus clock	-
162	SDC2_CMD	IO		P2	SDIO Bus command	-
163	SDC2_DATA_0	IO		P2	SDIO Bus data 0	-
164	SDC2_DATA_1	IO		P2	SDIO Bus data 1	-

165	SDC2_DATA_2	IO		P2	SDIO Bus data 2	-
166	SDC2_DATA_3	IO		P2	SDIO Bus data 3	-
167	GND	GND		-	Ground Pin	-
168	GND	GND		-	Ground Pin	-
169	GND	GND		-	Ground Pin	-
170	GND	GND		-	Ground Pin	-
171	GND	GND		-	Ground Pin	-
172	GND	GND		-	Ground Pin	-
173	GND	GND		-	Ground Pin	-
174	GND	GND		-	Ground Pin	-
175	GND	GND		-	Ground Pin	-
176	GND	GND		-	Ground Pin	-
177	GND	GND		-	Ground Pin	-
178	GND	GND		-	Ground Pin	-
179	GND	GND		-	Ground Pin	-
180	GND	GND		-	Ground Pin	-
181	GND	GND		-	Ground Pin	-
182	GND	GND		-	Ground Pin	-
183	GND	GND		-	Ground Pin	-
184	GND	GND		-	Ground Pin	-
185	GND	GND		-	Ground Pin	-
186	GND	GND		-	Ground Pin	-
187	GND	GND		-	Ground Pin	-
188	GND	GND		-	Ground Pin	-
189	GND	GND		-	Ground Pin	-

190	GND	GND		-	Ground Pin	-
191	GND	GND		-	Ground Pin	-
192	GND	GND		-	Ground Pin	-
193	GND	GND		-	Ground Pin	-
194	GND	GND		-	Ground Pin	-
195	GND	GND		-	Ground Pin	-
196	GND	GND		-	Ground Pin	-
197	GND	GND		-	Ground Pin	-
198	GND	GND		-	Ground Pin	-
199	GND	GND		-	Ground Pin	-
200	GND	GND		-	Ground Pin	-
201	GND	GND		-	Ground Pin	-
202	GND	GND		-	Ground Pin	-
203	GND	GND		-	Ground Pin	-
204	GND	GND		-	Ground Pin	-
205	GND	GND		-	Ground Pin	-
206	GND	GND		-	Ground Pin	-
207	GND	GND		-	Ground Pin	-
208	GND	GND		-	Ground Pin	-
209	GND	GND		-	Ground Pin	-
210	GND	GND		-	Ground Pin	-
211	GND	GND		-	Ground Pin	-
237	LCD_LIGHT_EN	DO	GPIO_19 UART4_RTS_N SPI4_CLK I2C4_SCL	P3	Configurable I/O Pin	-
238	RESERVED	-		-	Do not connect	-

239	LCD_TE_B	DO	GPIO_18 UART4_CTS_N SPI4_CS_N I2C4_SDA	P3	LCD Tear effect	-
240	LCD_CS	DO	GPIO_23 UART6_RTS_N	P3	LCD Chip Select	-
241	LCD_DS	DO	GPIO_22 UART6_CTS_N SPI6_CS_N I2C6_SDA	P3	LCD Data Select	-
242	VREG_L11_1P8	PO		P3	Module Output Voltage	-
243	RESERVED	-		-	Do not connect	-
244	RESERVED	-		-	Do not connect	-
245	RESERVED	-		-	Do not connect	-
246	LCD_RESET_N	DO	GPIO_74	P3	Reset LCD	-
247	RESERVED	-		-	Do not connect	-
248	LCD_D_4	DO		P3	LCD Data line 4	-
249	LCD_D_7	DO		P3	LCD Data line 7	-
250	LCD_D_5	DO		P3	LCD Data line 5	-
251	LCD_D_6	DO		P3	LCD Data line 6	-
252	LCD_OE_N	DO		P3	LCD output enable negative	-
253	LCD_RS	DO		P3	LCD Register Select	-
254	LCD_WE_N	DO		P3	LCD write enable negative	-
255	LCD_D_3	DO		P3	LCD Data line 3	-
256	LCD_D_2	DO		P3	LCD Data line 2	-
257	LCD_D_0	DO		P3	LCD Data line 0	-
258	LCD_D_1	DO		P3	LCD Data line 1	-

NOTE

- The module typically has an IO port level of 1.8V (in addition to the SIM, the SIM card port level supports 1.8V).
- GPIO_24, GPIO_25, GPIO_43, GPIO_44 have boot config function so a high signal before completing the bootup will have undesired effect.
- This module defines the RESERVED pin as a reserved pin. It is recommended to be suspended and must not be used

3.3 Power interface

The C20QM module power interface consists of three parts:

- ✓ VCC1, VCC2, VCC3, VCC4, VCC5 and VCC6 are the module working power supply.
- ✓ UIM1_POWER is the working power supply for SIM card.
- ✓ VREG_OUT_1V8

3.3.1 Power Supply Design

The power interface of the C20QM module is as follows:

Table 3.5 Power Pin Definitions

Power supply							
Pin No.	Definition	IO	Description	Remarks	Min	Typical	Max
37	VCC1	PI	Module input voltage	-	3.4V	3.8V	4.5V
38	VCC2	PI	Module input voltage	-	3.4V	3.8V	4.5V
39	VCC3	PI	Module input voltage	-	3.4V	3.8V	4.5V
40	VCC4	PI	Module input voltage	-	3.4V	3.8V	4.5V

41	VCC5	PI	Module input voltage	-	3.4V	3.8V	4.5V
42	VCC6	PI	Module input voltage	-	3.4V	3.8V	4.5V
133	USIM_VCC	PO	SIM card power supply	-	0	1.8V/ 2.85V	1.98/ 3.3V
146	VREF_OUT	PO	Reference voltage	-		1.8V	

The C20QM module is powered by a single power supply and the module provides six power supply pins. The power supply range is from 3.4V to 4.5V. It is recommended to use 3.8V power supply. If the module's operating voltage drop causes the VCC supply voltage to be too low or the supply current is insufficient, the module may shut down or restart. Therefore, to reduce the power fluctuation of the module when working, it is necessary to use a low-ESR value of the voltage regulator capacitor, the power pin and the ground pin should be connected and can provide sufficient power supply capability.

Under the premise of ensuring that the VCC power supply is sufficient, one 22uF tantalum capacitor can be connected in parallel with the power input, 10uF in parallel, two 0.1uF capacitor (eliminating clock and digital signal interference) and 33nF (eliminating low frequency RF interference) ceramic capacitors.

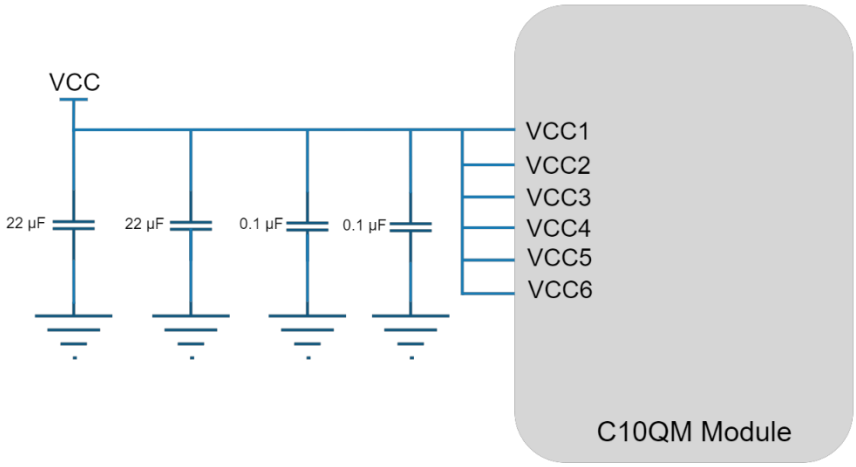


Figure 3 VCC Power Supply

3.3.2 Power Reference Circuit

In actual design, the power circuit can be designed using a switching DC power supply or a linear LDO power supply, and then the PMOS transistor is used to control the power supply input so that the power supply can be completely cut off. Both design circuits need to supply enough current.

Specific reference to the following circuit design:

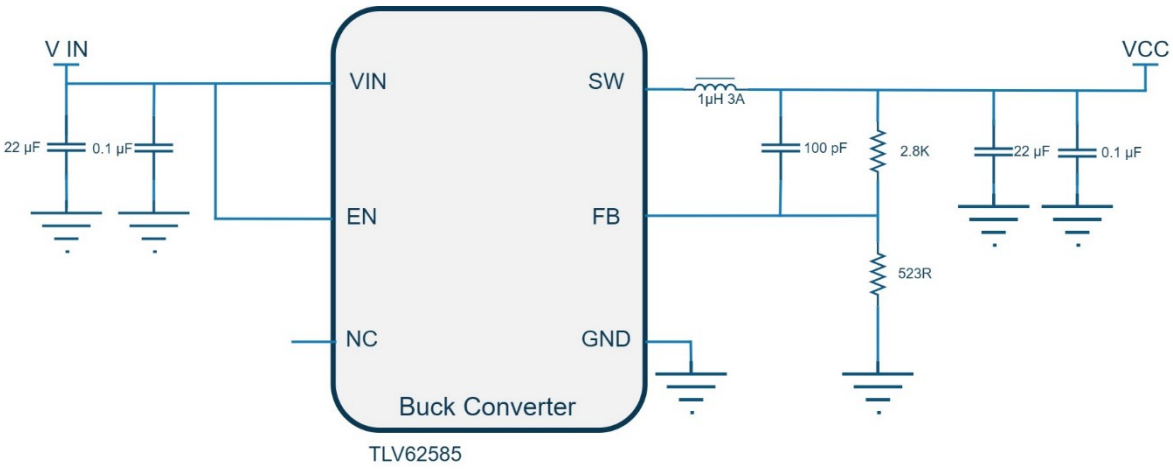


Figure 4 DC Switching Power Supply Reference Circuit

NOTE

- To prevent damage to the module from surges and over voltages, it is recommended to connect a 5.1V/500mW Zener diode to the VCC pin of the module.
- It is recommended to add 3 ceramic capacitors (33pF, 10pF, 100nF) to the power pin input and place them near the VCC pin.
- The minimum operating voltage of the module is 3.4V. Data transmission or calls will generate a current of more than 2, thus a ripple voltage drop will occur on the power supply voltage. Therefore, the actual supply voltage must not be lower than 3.4V.
- Due to the large current consumption of the module power pins, it is recommended that the PCB traces be as short as possible. Minimize the equivalent impedance of the VCC trace.

3.3.3 VREF 1.8 Voltage Output

The C20QM module outputs 1.8V through VREF for internal digital circuitry. This voltage is the logic level voltage of the module. After normal power-on, the 146th pin will output 1.8V and the current load will be 50mA. The external master can read the voltage of VREF to determine if the module is powered on. VREF can also be used as an external power supply, such as a level shifting chip, but maximum load should be within 50mA.

Table 3.6 VREF pin definition

Pin No.	Signal name	I/O	High value	Description
146	VREF_OUT	PO	1.8V	Power on

3.4 Switching Machine Reset Mode

3.4.1 Turn ON Module

The 142nd pin of the C20QM module is POWER_ON pin. The module can be powered on by pulling down the POWER_KEY LOW for at least 500ms. The user can check whether the module is powered on by querying the high and low levels of the VDD_EXT pin.

Table 3.7 Switch Pin Definition

Pin No.	Signal name	I/O	High value	Description
142	POWER_ON	PI	VBAT	Active Low pin

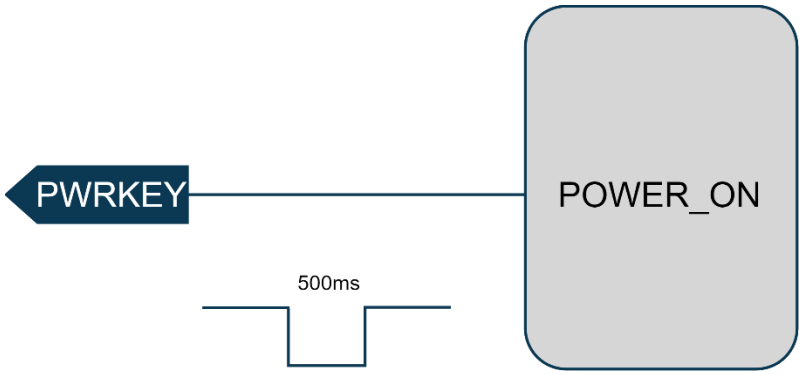


Figure 5 Power-on Reference Circuit

3.4.2 Reset Control

The Pin 145 of C20QM module Pin is the Reset pin. The application detects that the module is abnormal. When the software does not respond, the module can be reset. Pull the pin low for 100-600ms to reset the module. The RESET pin is sensitive to interference. A 10nF to 0.1uF capacitor can be installed near the signal for signal filtering. Keep away from RF interference signals when routing.

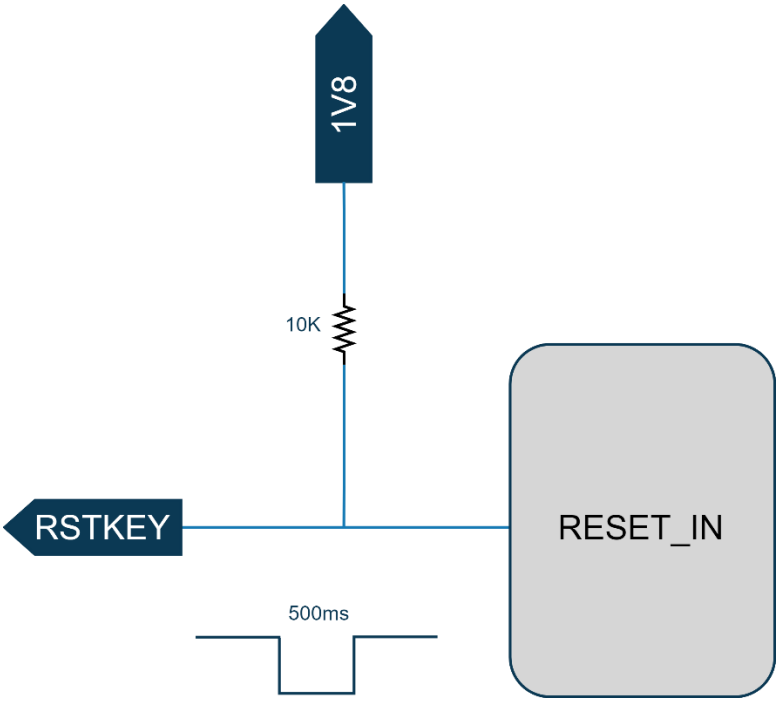


Figure 6 Reset Reference Circuit.

Table 3.8 RESET Pin Parameters

Pin No.	Signal name	I/O	High value	Description
145	RESET_IN	DI	VBAT	Module Reset Control

The C20QM module supports AT command reset, and the AT command is **AT+TRB** to restart the module. Detailed instructions can be found in the C20QM AT Command Set Manual.

3.5 USB Interface

The C20QM module USB interface supports *USB2.0* high-speed protocol. The USB interface work as OTG host, therefore it can work as Host and Slave mode and does not support USB charging mode. USB input and output traces must comply with the *USB2.0* feature. The input power supply of USB_VBUS is 3.3V - 5V. The USB interface is used to update the firmware of the module. The USB interface is defined as follows:

Table 3.9 USB Interface Pin Definition

Pin No.	Signal name	I/O	Description
86	USB_DP	IO	USB differential signal +

87	USB_ID	DI	USB ID detect
88	USB_DM	IO	USB differential signal -

The module only acts as a USB slave device and supports *USB Sleep* and *Wake-Up* mechanisms. USB interface application reference circuit is as follow:

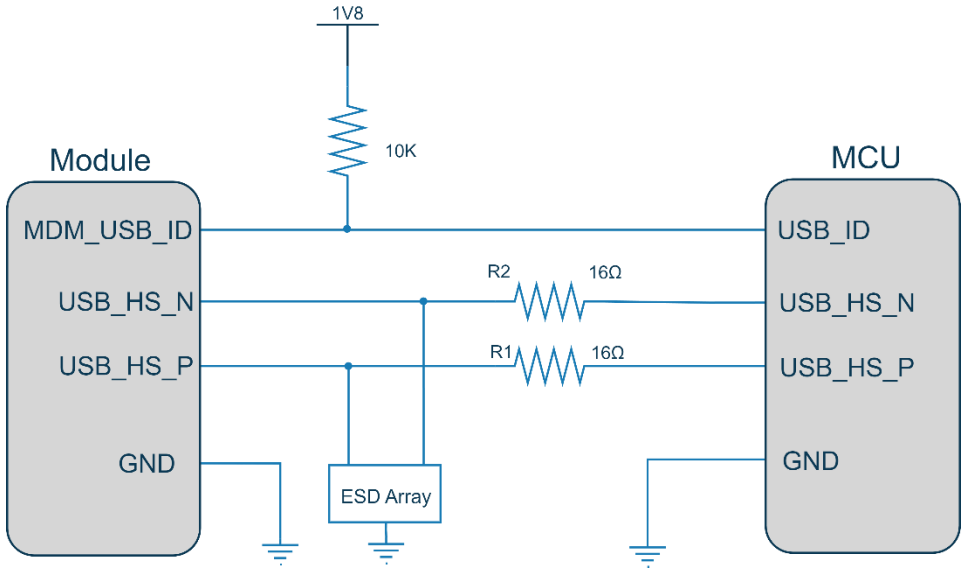


Figure 7 USB connection design circuit diagram with ID Pulled up

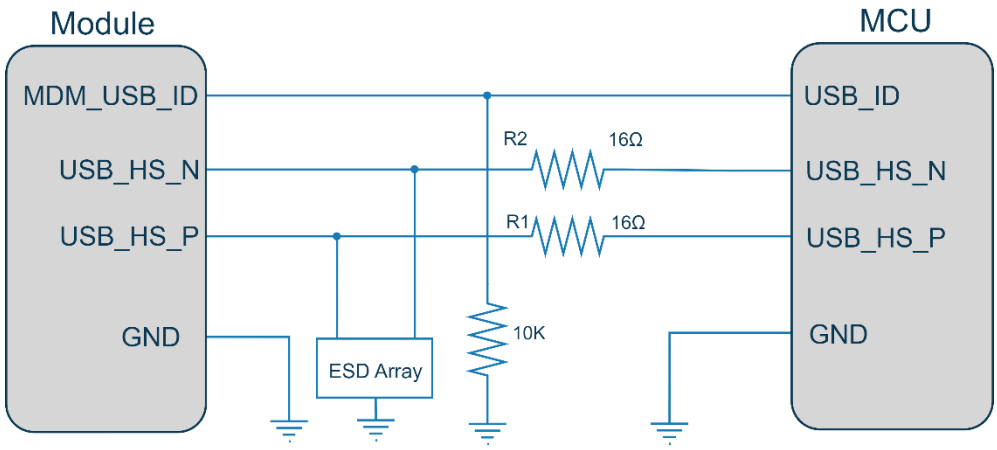


Figure 8 USB connection design circuit diagram with ID Pulled down

NOTE

- Required a resistance of 16R for R1/R2.
- The USB interface supports high-speed (480Mbps) and full-speed (12Mbps) modes, so the trace design needs to strictly follow the USB2.0 protocol requirements, pay attention to the protection of the data line, differential trace, control impedance is 90Ω.
- In order to improve the antistatic performance of the USB interface, it is recommended to add an ESD protection device on the data line. The equivalent capacitance of the protection device is less than 2pF.
- The USB interface bus supply voltage is provided internally by the module and does not need to be externally supplied. At the same time, since the USB interface of the module does not provide USB bus power, the module can only be used as a slave device of the USB bus device.

3.6 UART Interface

The C20QM module provides three sets of UART interfaces. AT port, Debug port and User UART port. The maximum baud rate supported is 4 Mbps.

3.6.1 UART3 Serial Port

The pins 64, 65, 80 and 81 of the C20QM module are UART3 serial port pins. UART3 serial interface can be used to interact with peripheral devices. The pins are defined as follows：

Table 3.10 UART3 Serial Port Signal Definition

Pin No.	Signal name	I/O	Description	Parameter	Level value (V)			Remark
					min	typical	max	
64	UART3_RX	DI	Data reception	VOH	1.3	1.8	1.9	
				VOL	-0.3		0.6	
65	UART3_TX	DO	Data transmission	VIH	1.3	1.8	1.9	
				VIL	0		0.45	
80	UART3_RTS	DO	Request to send	-	-	-	-	-

81	UART3_CTS	DI	Clear to Send	-	-	-	-	-

3.6.2 UART4 Serial Port (AT UART)

The pins 106 and 107 of the module are UART4 serial port pins. UART4 serial interface is configured as the AT port. Users can use this UART port for communication using AT commands. The default baud rate is 115200 bps. The maximum Baud rate is 4Mbps. The pins are defined as follows:

Table 3.11 UART4 Serial Port Pin Definition

Pin No.	Signal name	I/O	Description	Parameter	Level value (V)			Remark
					min	typical	max	
106	UART4_RX	DI	Data reception	VIH	1.3	1.8	1.9	1.8V voltage domain
				VIL	-0.3		0.6	
107	UART4_TX	DO	Data transmission	VOH	1.3	1.8	1.9	1.8V voltage domain
				VOL	0		0.45	

3.6.3 UART5 Serial Port (Debug UART)

The pins 82 and 83 of the module are UART5 serial port pins. UART5 serial interface can be used for debugging purposes. The default baud rate is 115200 bps. The maximum Baud rate is 4Mbps. The pins are defined as follows:

Table 3.12 UART5 Serial Port Pin Definition

Pin No.	Signal name	I/O	Description	Parameter	Level value (V)			Remark
					min	typical	max	
82	DBG_UART5_RX	DI	Data reception	VIH	1.3	1.8	1.9	1.8V voltage domain
				VIL	-0.3		0.6	
83	DBG_UART5_TX	DO		VOH	1.3	1.8	1.9	

			Data transmission	VOL	0		0.45	1.8V voltage domain

3.6.5 Serial Port Application Circuit

The serial level is 1.8V.

The module's serial port baud rate can be set to 4800 to 921600bps baud rate and the default is 115200bps.

To use a 2-wire serial port, User may refer to the following serial port design:

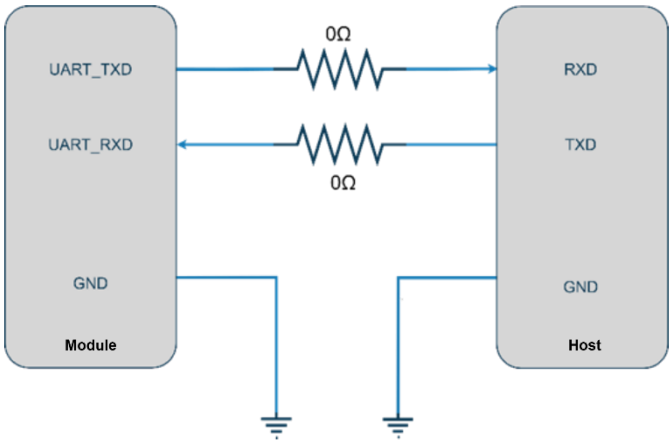


Figure 9 UART Serial Port Design

The serial port of the module is TTL 1.8V level. If the serial port needs to be connected to the MCU of 3.3V level, it is necessary to add a level conversion chip externally to achieve level matching. Use an external 1.8V power source for VCCA. For the chip connection method, refer to the following circuit:

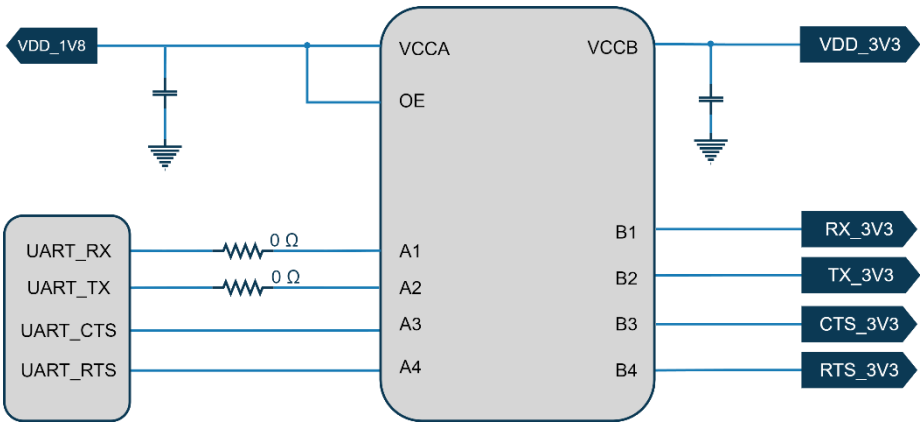


Figure 10 Level Conversion Technique

3.7 uSIM Interface

The C20QM module provides a USIM card interface compatible with the ISO 7816-3 standard. The USIM card power supply is provided by the module's internal power manager and supports 1.8V/3.0V

Table 3.13 SIM Card Signal Definition

No	Signal name	I/O	Description
133	USIM_VDD	PO	USIM card power supply
134	USIM_DATA	IO	USIM card data
135	USIM_CLK	DO	USIM card clock
136	USIM_RESET	DO	USIM card reset
137	USIM_PRESENT	DI	Sim detect
138	USIM_SELECT	DO	Sim Select

3.7.1 uSIM Card Reference Circuit

The C20QM module does not come with a uSIM card slot. Users need to design a USIM card slot on their own interface board.

The USIM card interface reference circuit is as follows:

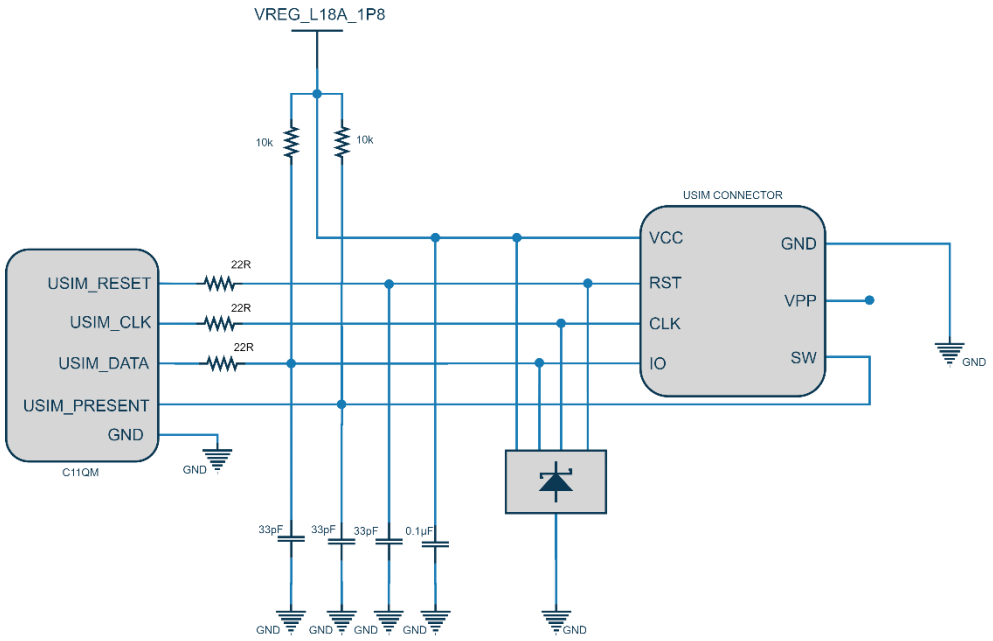


Figure 11 USIM Design Circuit Diagram

NOTE

- The USIM interface cable is recommended to use ONSEMI's SMF15C device for ESD protection. The peripheral circuit components should be placed close to the card holder. The SIM card holder is close to the module layout.
- The USIM card circuit is susceptible to radio frequency interference and does not recognize or drop the card. Therefore, the card slot should be placed as far as possible from the RF radiation of the antenna. The card trace should be as far away as possible from the RF, power supply and high-speed signal lines.
- The USIM_DATA has been internally pulled up to 1.8V (only resistor, use an external power source) through a 47K resistor, and no external pull-up is required.
- USIM_PRESENCE is high by default. The SIM card status can be detected by this PIN during hot plug application.
- To avoid transient voltage overload, the USIM interface requires a 22R resistor in series with each other on the signal line path.
- The ground of the USIM deck and the ground of the module should maintain good connectivity.

3.8 General Purpose GPIO Interface

The C20QM module contains nine general purpose control signals. The interface is defined as follows:

Table 3.14 General GPIO Pin Definitions

Pin No.	Definition	I/O	Functional description
52	GPIO_42	DIO	General Purpose Pin 42
53	GPIO_43	DIO	General Purpose Pin 43
54	GPIO_44	DIO	General Purpose Pin 44
55	GPIO_45	DIO	General Purpose Pin 45
56	GPIO_46	DIO	General Purpose Pin 46

57	GPIO_47	DIO	General Purpose Pin 47
58	GPIO_52	DIO	General Purpose Pin 52
157	GPIO_157	DIO	General Purpose Pin 157
158	GPIO_158	DIO	General Purpose Pin 158

3.9 Network Status Indication Interface

The C10GS module provides one GPIO pins to indicate module status.

Table 3.15 Definition of Network Indicator Lamp

Pin No.	Signal name	I/O	Description
141	WWAN_STATE	DO	Network indication

Table 3.16 Network Indicator State

Pin	Signal state
Module is not run, or module is not registered	Low
Module registration to network successful	High
Module is scanning for network	Blinking

LED network indicator light reference design chart is as follows:

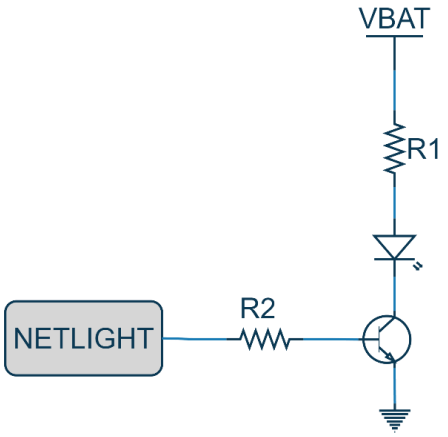


Figure 12 Circuit Diagram of Network Indicator

NOTE

- The resistance value in the circuit diagram of the network indicator can be adjusted according to the LED lamp parameters.
- The brightness of the network indicator can be adjusted by adjusting the current limiting resistor R1.

3.10 PCM digital voice interface

C20QM module provides a set of PCM audio interfaces supporting 8-bit A-rate, U-rate and 16-bit linear short frame encoding formats with PCM_SYNC of 8 kHz and PCM_CLK of 2048 kHz.

Table 3.17 PCM Pin Definition

Pin No.	Signal name	I/O	Description	Parameter	Level value (V)		
					min	typical	max
47	PCM_DIN	DI	PCM data input	VIH	1.3	1.8	1.9
				VIL	-0.3		0.6
48	PCM_DOUT	DO	PCM data output	VOH	1.3	1.8	1.9
				VOL	0		0.45

46	PCM_SYNC	DO	PCM frame sync signal	VOH	1.3	1.8	1.9
				VOL	0		0.45
49	PCM_CLK	DO	PCM clock pulse	VOH	1.3	1.8	1.9
				VOL	0		0.45
99	CODEC_INT	DI	-	-	-	-	-

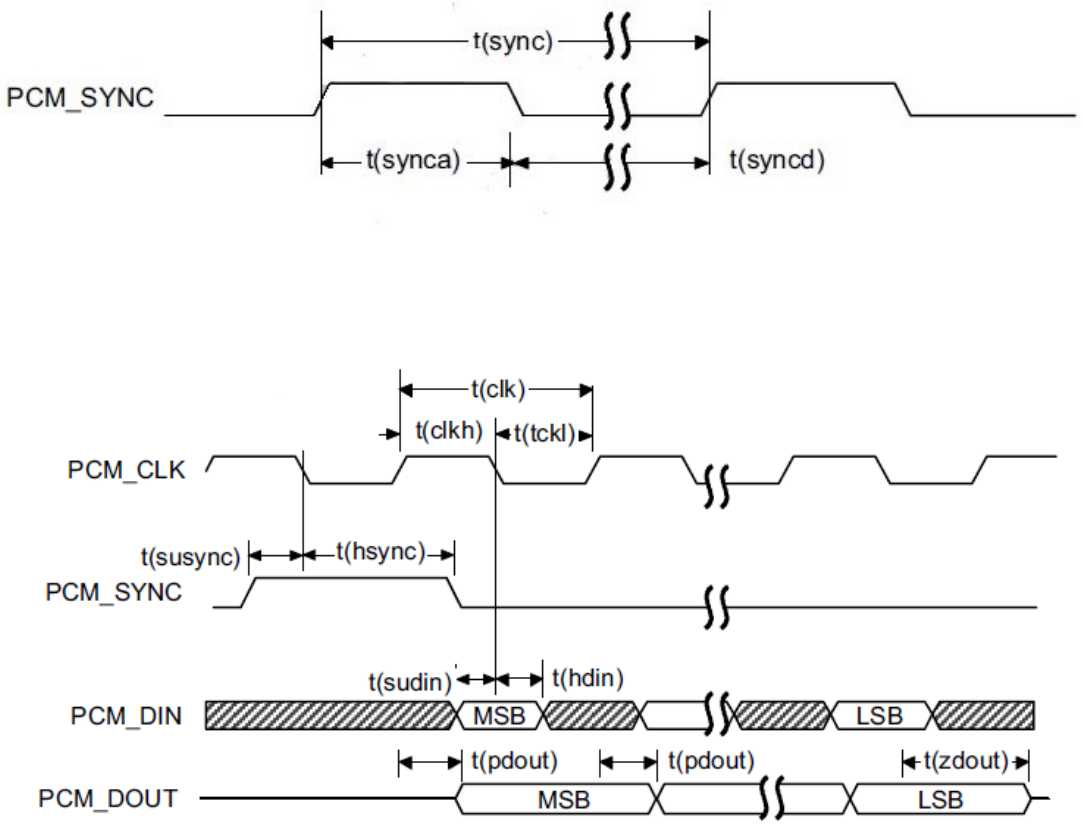


Figure 13 PCM Short Frame Mode Timing Diagram

Table 3.18 PCM Specific Parameters

Characteristic	Description
Encoding format	Linear
Data bit	16bits
Master-slave mode	Master/slave mode
PCM clock	2048kHz
PCM frame synchronization	Short frame
Data Format	MSB

The recommended circuit for PCM to analog voice is as follows:

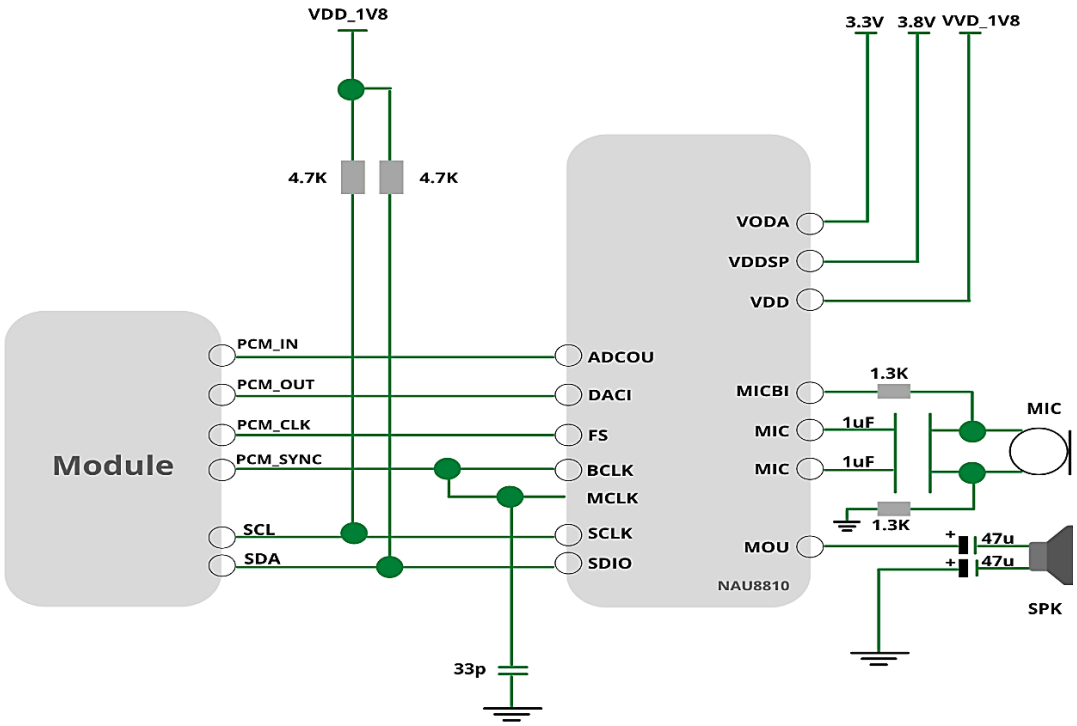


Figure 14 PCM to Analog Voice Map

3.11 I2C Bus

The C20QM module provides a set of hardware bidirectional serial buses with an I2C interface of 1.8V level, a *5.0 Protocol* interface, and a clock rate of 400 KHz.

Table 3.19 I2C Pin Definition

Pin No.	Signal name	I/O	Description	Parameter	Level value (V)		
					min	typical	max
127	I2C_SCL	DO	I2C bus clock output	VOH	1.3	1.8	1.9
				VOL	0		0.45
128	I2C_SDA	DIO		VOH	1.3	1.8	1.9
				VOL	0		0.45

			I2C bus data input and output	VIH	1.3	1.8	1.9
				VIL	-0.3		0.6

The I2C reference circuit is connected as follows:

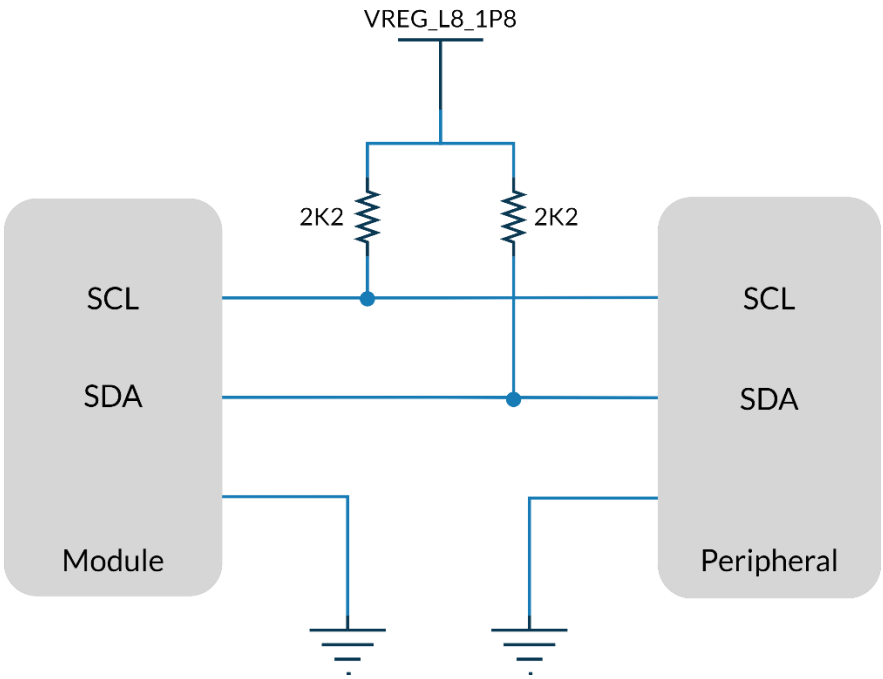


Figure 15 I2C Interface Reference Circuit Diagram

3.12 SD Host Interface

C20QM module provides a set of 4-bit SD / MMC interfaces, supports SD3.0 protocol, supports two voltage SD cards of 1.8V / 2.95V, clock frequency up to 50MHz, maximum capacity supports 32GB. Provide VREF voltage for SDIO power supply.

Table 3.20 SD Host Interface Pin Definitions

Pin No.	Pin name	IO	Definition
67	SDH_D0	IO	SD card SDIO bus DATA0
68	SDH_D1	IO	SD card SDIO bus DATA1
69	SDH_D2	IO	SD card SDIO bus DATA2

70	SDH_D3	IO	SD card SDIO bus DATA3
71	SDH_CLK	DO	SD card SDIO bus clock
72	SDH_CMD	IO	SD card SDIO bus command
73	VDD_SDIO	DO	Reference voltage for SD Card, Bluetooth module and Wi-Fi module.
78	SD_CARD_DET_N	IO	SD Card detect pin

NOTE

- The SDIO bus speed is fast, and the Layout trace must conform to the SDIO3.0 specification.
- The maximum output current of the module power supply VDD_SD is 400mA.
- The reference voltage for SDC is 3.3V, if the Bluetooth and Wi-Fi module is of 1.8V a translator is required.
- SD card clock frequency is up to 200MHZ. SDC bus is a high-speed signal line and the characteristic impedance of the PCB design needs to be controlled at about 50 ohms.
- The length of the signal line should be less than 25mm, and the distance between the signal lines should be 2 times the line width, and the ground should be as far away as possible from other possible interference lines.
- The SDC signal line needs a 0-ohm resistor in series to facilitate signal quality adjustment.
- In order to ensure good ESD performance, it is recommended to add a TVS tube to the SD card pin and place it near the pin.

3.13 SDC Interface

C20QM module provides a set of 4-bit SDC interface, supports SD3.0 protocol, supports two voltage SD cards of 1.8V / 2.95V, clock frequency up to 50MHz, maximum capacity supports 32GB. Provide VREF voltage for SDIO power supply.

Table 3.21 SDC Interface Pin Definitions

Pin No.	Pin name	IO	Definition
163	SDC2_D0	IO	SD card SDIO bus DATA0
164	SDC2_D1	IO	SD card SDIO bus DATA1
165	SDC2_D2	IO	SD card SDIO bus DATA2
166	SDC2_D3	IO	SD card SDIO bus DATA3
161	SDC2_CLK	DO	SD card SDIO bus clock
162	SDC2_CMD	IO	SD card SDIO bus command

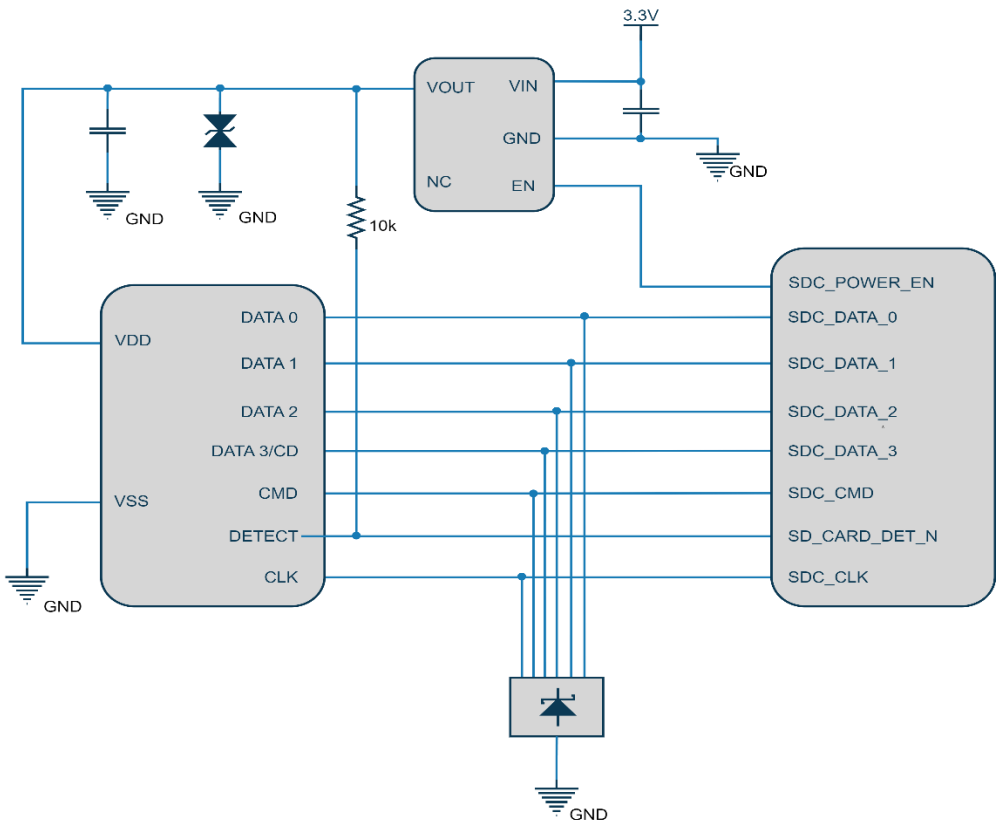


Figure 16 SDC Interface Reference Circuit Diagram

3.14 Antenna

The C20QM module provides three antenna interfaces, Main and diversity antenna interface, which is responsible for the LTE and GSM signals of the transceiver module and a GNSS antenna interface.

The GNSS antenna interface is **L1.**

The impedance of the antenna interfaces are 50 ohms.

Table 3.22 Antenna Interface Pin Definition

Pin No.	Signal Name	IO	Description	Remarks
3	ANT_MAIN	IO	Main antenna interface	50Ω characteristic impedance
33	GNSS_L1	AI	GNSS L1 antenna interface	50Ω characteristic impedance
27	ANT_DIV	IO	Diversity antenna interface	50Ω characteristic impedance

The pin-3 of the C20QM is the main antenna interface and pin-27 is the Diversity antenna interface.

To facilitate the debugging of the antenna, a **π**-type matching circuit needs to be added to the main board, and a 50-ohm impedance line is taken.

Recommended circuit is shown below：

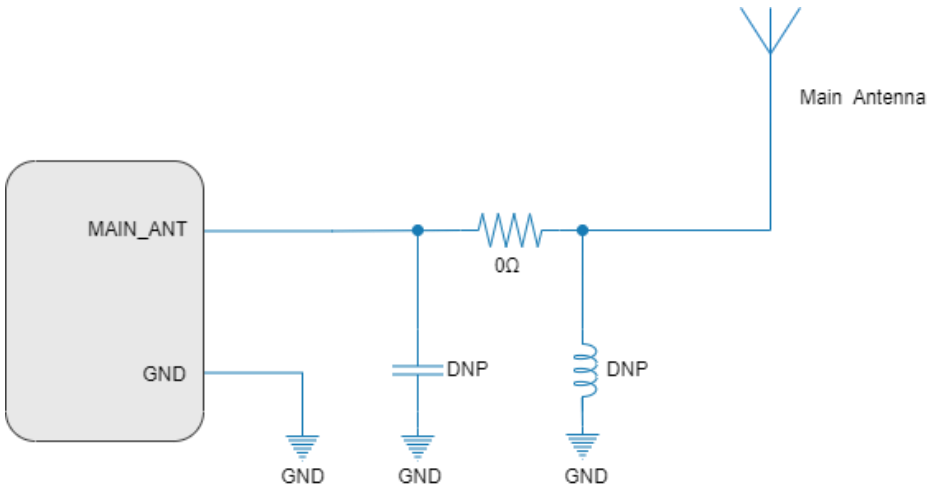


Figure 17 Main Antenna Matching Circuit

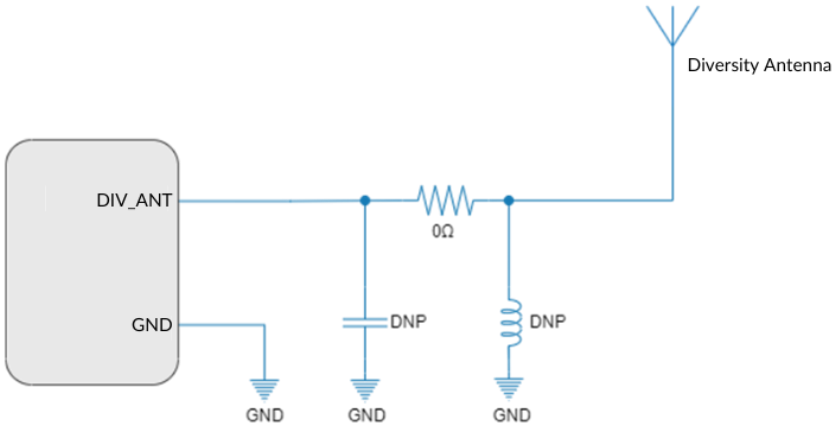


Figure 18 Diversity antenna matching circuit

The pin 33 of C20QM is the GNSS antenna interface.

The C20QM has a dedicated antenna **L1**, it supports GPS, GLONASS, BEIDOU, QZSS, Galileo.

QZSS and SBAS Ranging support available.

In order to facilitate antenna debugging, a **π**-type matching circuit needs to be added to the motherboard and a 50-ohm impedance line is used.

NOTE

- The GNSS antenna needs to maintain a certain distance from the main antenna.
- The GNSS antenna has two antenna connection mode:
  Passive antenna mode and Active antenna mode
- External power needs to be provided since the module itself cannot supply power to GNSS Active antenna.

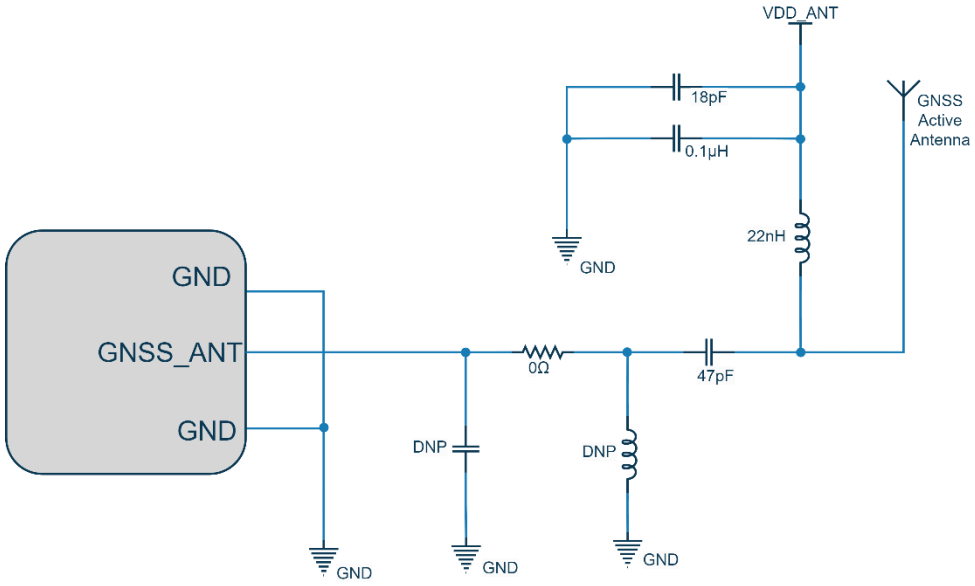


Figure 19 GNSS Active Antenna Matching Circuit

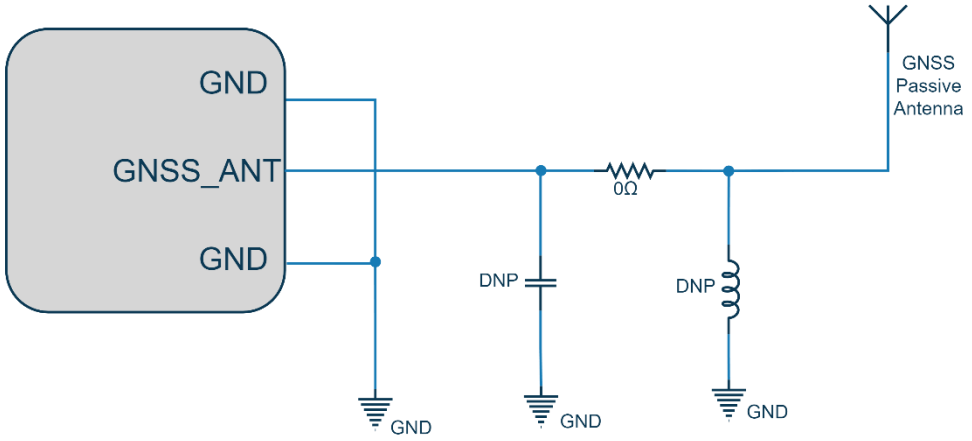


Figure 20 GNSS Passive Antenna Matching Circuit

NOTE

- An external LDO can be selected to supply power according to the active antenna requirement.
- If the module is designed with a passive antenna, then the VDD circuit is not needed.
- The LTE_MAIN antenna is distributed reasonably to improve the receiving sensitivity.
- In actual use, the antenna board can be debugged and optimized according to the user's circuit board.
- Antenna impedance traces need to be away from digital signal lines, power supplies and other interference signals.
- The antenna impedance traces need to be three-dimensionally packaged, and the ground holes are added on both sides of the trace to isolate.

3.14.1 RF Trace Reference

The main set of the C20QM module are extracted by pad. The antenna pad to the antenna feed point must use microstrip lines or other types of RF traces. The characteristic impedance of the signal line should be controlled at 50Ω.

The impedance of the RF signal line is determined by the material's dielectric constant, trace width (W), ground clearance (S), and reference ground plane height (H). Therefore, the RF trace requires an impedance simulation tool to calculate the impedance of the RF trace.

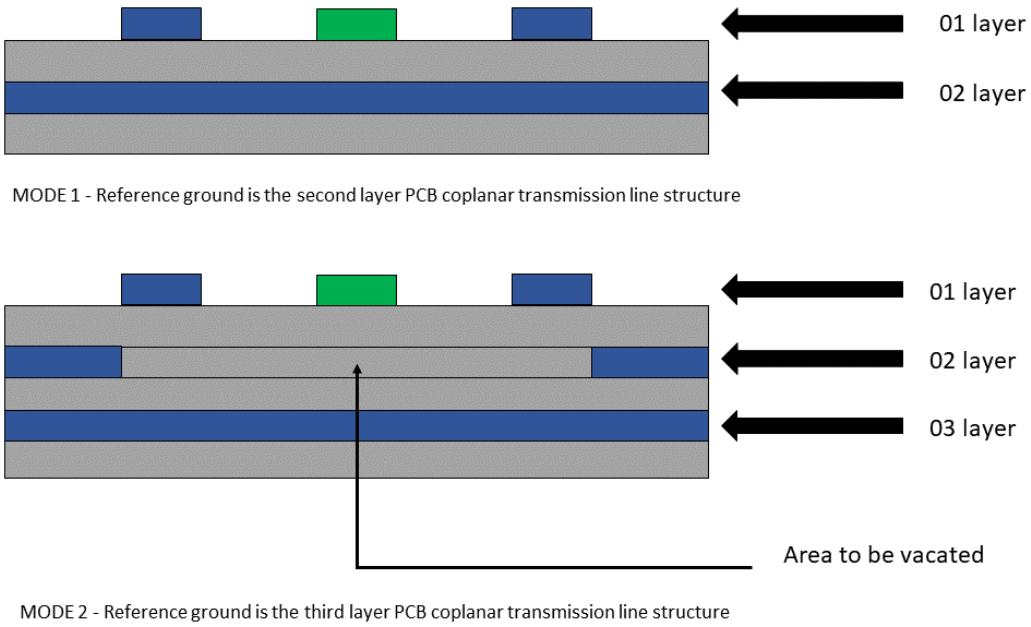


Figure 21 Coplanar Antenna

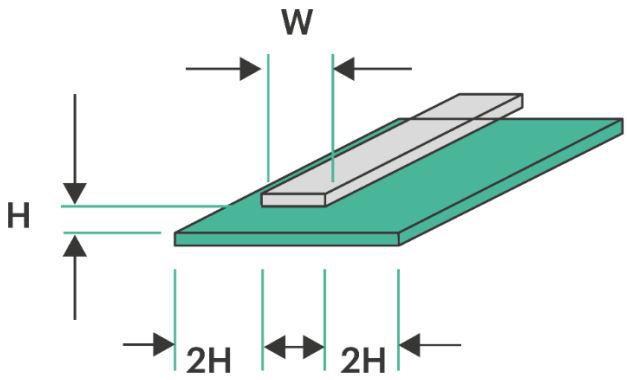


Figure 22 The Complete Structure of the Two-Layer PCB Microstrip Line

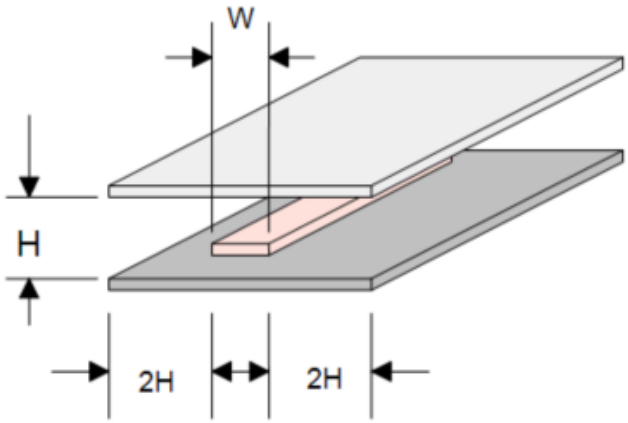


Figure 23 The Complete Structure of the Multilayer PCB Strip Line

NOTE

- Since Coplanar antennas are having maximum noise immunity, it is preferred.

3.15 Control Interface

Different module interfaces are available in module.

Table 3.23 Control Interface Pin Definition

Pin No.	Signal name	I/O	Description
59	WAKEUP_IN	DI	Module wake up
113	STATUS	DO	Module status
115	FLIGHT_MODE	DI	Module flight mode

WAKEUP_IN:

WAKEUP_IN wakeup the device after entering sleep mode via AT command or by default it goes to sleep mode in some cases.

STATUS:

This pin is used to get the status of the module.

FLIGHT_MODE:

This pin is used to disable RF transmission.

3.16 SGMII Interface

The SGMII interface is a serial interface featuring a low pin count that can be configured for ethernet.

Table 3.24 SGMII Interface Pin Definition

Pin No.	Signal name	I/O	Description
92	MDIO_CLK	DO	Management Data clock reference
93	EPHY_INT_N	DI	Ethernet PHY Interrupt
94	MDIO_DATA	DIO	Management Data
95	EPHY_RST_N	DO	Ethernet PHY reset
96	SGMII_RX_N	AI	SGMII Receive - Negative
98	SGMII_RX_P	AI	SGMII Receive - Positive
100	SGMII_TX_N	AO	SGMII Transmit - Negative
102	SGMII_TX_P	AO	SGMII Transmit - Positive

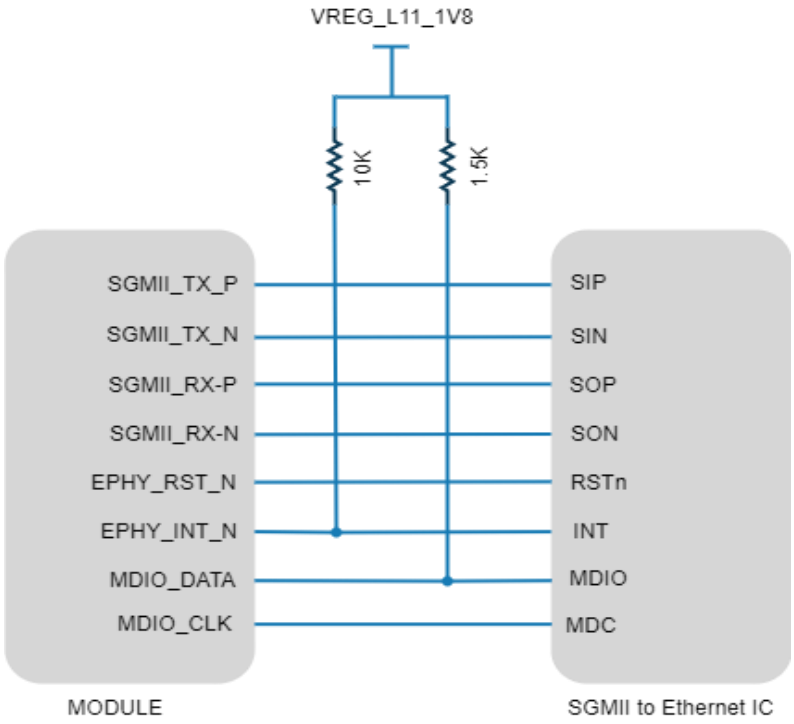


Figure 24 Ethernet (SGMII) Interface Reference Circuit Diagram

3.17 GNSS Interface

Multi – GNSS receiver:

- ✓ **L1** multi-band GNSS receiver
- ✓ Multi-Constellation GPS/GLONASS/Galileo/Bei Dou/QZSS.

Table 3.25 GNSS Antenna Pin Definition

Pin No.	Signal name	I/O	Description
33	GNSS_L1	AI	GNSS L1 antenna interface

3.18 JTAG Interface

The JTAG interface is used to troubleshoot the device and evaluate its functionality.

Table 3.26 JTAG Interface Pin Definition

Pin No.	Signal name	I/O	Description
147	JTAG_TCK	DO	Test clock (Not for customer)
148	JTAG_TMS	DI	Test mode select (Not for customer)
149	JTAG_TDI	DI	Test data input (Not for customer)
150	JTAG_TDO	DO	Test data output (Not for customer)
151	MDM_JTAG_SRST_N	DI	System Reset
152	MDM_JTAG_TRST_N	DI	Test Reset

3.19 SPI interface

C20QM supports an SPI interface which is master only. It communicates between module and peripherals through synchronous full duplex. The max clock rate is 50 MHz.

Table 3.27 SPI Interface Pin Definition

Pin No.	Signal name	I/O	Description
123	SPI_CS	DO	Slave select
124	SPI_MOSI	DO	Master output slave input
125	SPI_MISO	DI	Master input slave output
126	SPI_SCLK	DO	Clock

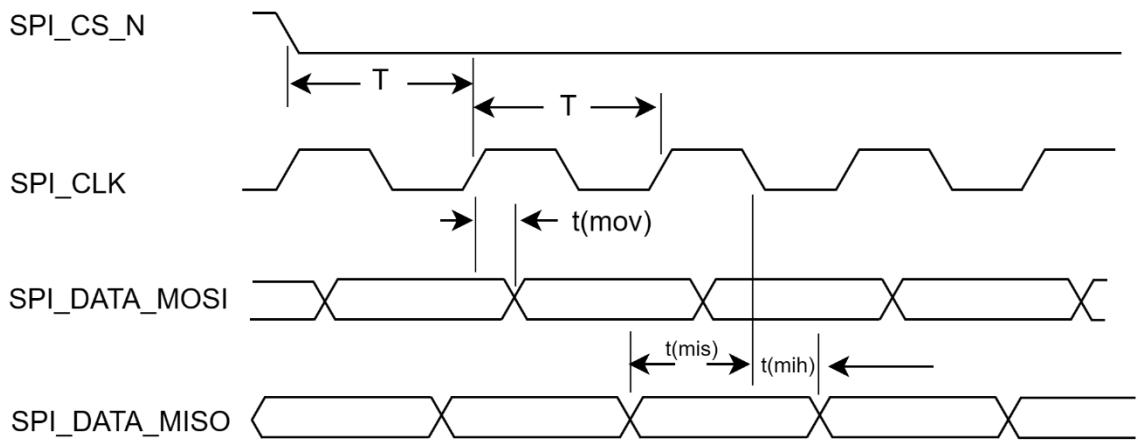


Figure 25 SPI Interface Timing Diagram

Table 3.28 SPI Master Timing Characteristics at 50 Mhz

Parameter	Definition	Min	Typ	Max	Unit
T	SPI clock period: 50 MHz max	20.0	-	-	ns
t (mov)	Master output valid	-5.0	-	5.0	ns
t (mis)	Master input setup	5.0	-	-	ns
t (mih)	Master input hold	1.0	-	-	ns

3.20 ADC interface

ADC interface converts the analog signals to digital signals which can be understood by the device. The module provides 2 Analog to Digital Converter interface.

Table 3.29 ADC Interface Pin Definition

Pin No.	Signal name	I/O	Description
129	ADC 1	AI	Generic ADC
131	ADC 2	AI	Generic ADC

3.21 LCD interface

LCD interface is enabled via MIPI DBI 8-bit interface.

Table 3.20 LCD Interface Pin Definition

Pin No.	Signal name	I/O	Description
237	LCD_BACKLIGHT	DO	LCD Backlight Control
239	LCD_TE	DI	LCD tearing effect signal
240	LCD_CS	DO	Chip Select
241	LCD_DS	DO	Data/Command select
242	VREG_L11_1P8	PO	LCD_VIN
246	LCD_RESET_N	DO	LCD_RESET
248	LCD_D_4	DO	LCD _Data_4
249	LCD_D_7	DO	LCD _Data_7
250	LCD_D_5	DO	LCD _Data_5
251	LCD_D_6	DO	LCD _Data_6

252	LCD_OE_N	DO	LCD Output Enable
253	LCD_RS	DO	LCD Register Select
254	LCD_WE_N	DO	LCD Write Enable
255	LCD_D_3	DO	LCD _Data_3
256	LCD_D_2	DO	LCD _Data_2
257	LCD_D_0	DO	LCD _Data_0
258	LCD_D_1	DO	LCD _Data_1

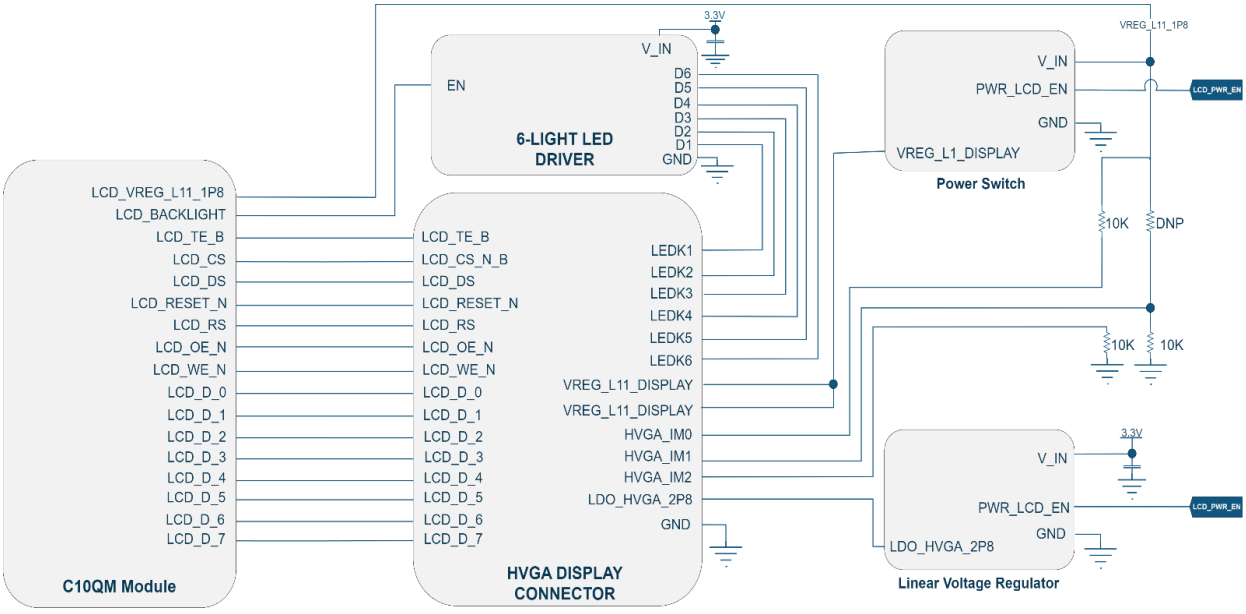


Figure 26 LCD (DBI) Interface Reference Circuit Diagram

4 Overall Technical Indicators

4.1 Chapter Overview

The C20QM module RF overall specifications include the following sections:

- ✓ Working frequency
- ✓ GNSS Performances
- ✓ Antenna requirements

4.2 Working Frequency

Variant	Frequency band	Uplink frequency	Downstream frequency	Mode
IN Bands	LTE B1	1920 MHz–1980 MHz	2110 MHz–2170 MHz	FDD
	LTE B3	1710 MHz–1785 MHz	1805 MHz–1880 MHz	FDD
	LTE B5	824 MHz–849 MHz	869 MHz–894 MHz	FDD
	LTE B8	880 MHz–915 MHz	925 MHz–960 MHz	FDD
	LTE B40	2300 MHz – 2400 MHz	2300 MHz – 2400 MHz	TDD
	LTE B41	2496 MHz-2590 MHz	2620 MHz-2690 MHz	TDD
	GSM 900	880 MHz-915 MHz	925 MHz-960 MHz	GSM
	GSM 1800	1710 MHz-1785 MHz	1805 MHz-1880 MHz	GSM
EU Bands	LTE B1	1920 MHz–1980 MHz	2110 MHz–2170 MHz	FDD
	LTE B3	1710 MHz–1785 MHz	1805 MHz–1880 MHz	FDD
	LTE B7	2500 MHz– 2570 MHz	2620 MHz – 2690 MHz	FDD
	LTE B8	880 MHz–915 MHz	925 MHz–960 MHz	FDD
	LTE B20	832 MHz– 862 MHz	791 MHz– 821 MHz	FDD

	LTE B28	703 MHz– 748 MHz	758 MHz – 803 MHz	FDD
	GSM 900	880 MHz-915 MHz	925 MHz-960 MHz	GSM
	GSM 1800	1710 MHz-1785 MHz	1805 MHz-1880 MHz	GSM
NA Bands	LTE B2	1850 MHz– 1910 MHz	1930 MHz– 1990 MHz	FDD
	LTE B4	1710 MHz– 1755 MHz	2110 MHz– 2155 MHz	FDD
	LTE B5	824 MHz– 849 MHz	869 MHz– 894 MHz	FDD
	LTE B12	698 MHz-716 MHz	728 MHz-746 MHz	FDD
	LTE B13	777 MHz – 787 MHz	746 MHz – 756 MHz	FDD
	LTE B17	704 MHz – 716 MHz	734MHz – 746 MHz	FDD
	LTE B25	1850 MHz – 1915 MHz	1930 MHz – 1995 MHz	FDD
	LTE B66	1710 MHz – 1780 MHz	2110 MHz – 2200 MHz	FDD
	GSM 900	880 MHz-915 MHz	925 MHz-960 MHz	GSM
	GSM 1800	1710 MHz-1785 MHz	1805 MHz-1880 MHz	GSM
EAJ Bands	LTE B1	1920 MHz–1980 MHz	2110 MHz–2170 MHz	FDD
	LTE B3	1710 MHz–1785 MHz	1805 MHz–1880 MHz	FDD
	LTE B5	824 MHz– 849 MHz	869 MHz– 894 MHz	FDD
	LTE B7	2500 MHz– 2570 MHz	2620 MHz – 2690 MHz	FDD
	LTE B8	880 MHz–915 MHz	925 MHz–960 MHz	FDD
	LTE B18	815 MHz – 830 MHz	860 MHz – 875 MHz	FDD
	LTE B19	830 MHz – 845 MHz	875 MHz – 890 MHz	FDD
	LTE B20	832 MHz– 862 MHz	791 MHz– 821 MHz	FDD
	LTE B26	814 MHz – 849 MHz	859 MHz – 894 MHz	FDD

	LTE B28	703 MHz - 748 MHz	758 MHz - 803 MHz	FDD
	LTE B38	2570 MHz– 2620 MHz	2570 MHz– 2620 MHz	TDD
	LTE B40	2300 MHz – 2400 MHz	2300 MHz – 2400 MHz	TDD
	LTE B41	2496 MHz-2590 MHz	2620 MHz-2690 MHz	TDD
	GSM 900	880 MHz-915 MHz	925 MHz-960 MHz	GSM
	GSM 1800	1710 MHz-1785 MHz	1805 MHz-1880 MHz	GSM
AN Bands	LTE B1	1920 MHz–1980 MHz	2110 MHz–2170 MHz	FDD
	LTE B3	1710 MHz–1785 MHz	1805 MHz–1880 MHz	FDD
	LTE B5	824 MHz–849 MHz	869 MHz–894 MHz	FDD
	LTE B8	880 MHz–915 MHz	925 MHz–960 MHz	FDD
	LTE B18	815 MHz – 830 MHz	860 MHz – 875 MHz	FDD
	LTE B19	830 MHz – 845 MHz	875 MHz – 890 MHz	FDD
	LTE B26	814 MHz – 849 MHz	859 MHz – 894 MHz	FDD
	LTE B28	703 MHz - 748 MHz	758 MHz - 803 MHz	FDD
	GSM 900	880 MHz-915 MHz	925 MHz-960 MHz	GSM
	GSM 1800	1710 MHz-1785 MHz	1805 MHz-1880 MHz	GSM

4.3 GNSS Performance

C20QM Module GNSS performance parameters:

Table 4-2 GNSS performance parameters

Features	Description
Receiving Bands	✓ GPS L1/ Galileo E1 C/A: 1575.42 MHz ✓ GLONASS L1 C/A: 1602.5625 MHz ✓ BD2 B1 C/A: 1561.098 MHz
Positioning Accuracy:	Autonomous: <2.0 m CEP50
TTFF@-130dBm	✓ Cold Start <28s ✓ Hot Start <1s
Sensitivity:	✓ Acquisition: -159 dBm ✓ Tracking: -163 dBm ✓ Reacquisition: -147 dBm

4.4 Antenna Requirements

C20QM Module Antenna Design Requirements:

Table 4.2 Antenna Indicator Requirements

Frequency band	Standing wave ratio	Antenna gain	Effectiveness	TRP	TIS
B1 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B2 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B3 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B4 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B5 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B7 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88

B8 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B12 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B13 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B17 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B18 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B19 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B20 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B25 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B26 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B40 TDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B41 TDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
B66 FDD	<2:1	〉-2.5dbi	〉40%	>16.5	<-88
GSM 900	<2:1	〉-2.5dbi	〉40%	>29	<-102
GSM 1800	<2:1	〉-2.5dbi	〉40%	>26	<-102

5 Interface Electrical Characteristics

5.1 Chapter Overview

- Working storage temperature
- Electrostatic property
- Module IO level
- Power supply
- Power consumption characteristics

5.2 Working Storage Temperature

Table 5.1 C20QM Module Working Storage Temperature

Parameter	Minimum	Typical	Maximum
Device operating temperature	-30°C	25°C	85°C
3GPP2-mode operating temperature (ambient)	-30°C	25°C	60°C
3GPP-mode operating temperature (ambient)	-20°C	25°C	60°C

5.3 Electrostatic Property

There is no overvoltage protection inside the C20QM module.

The ESD protection is required when the module is used to ensure product quality.

ESD design recommendations:

- ✓ The USB port needs to add TVS on VDD, D+, D- for protection, and the TVS parasitic capacitance on D+/D- is <2pF
- ✓ The module's USIM card external pin needs to be protected by TVS, and the parasitic capacitance

requirement is <10pF

- ✓ The PCB layout of the protective device should be as close as possible to the "V" line to avoid the "T" line
- ✓ The ground plane around the module guarantees integrity and should not be split
- ✓ ESD control of the surrounding environment and operators is required during module production, assembly and laboratory testing

Table 5.2 C20QM ESD Features

Test port	Contact discharge	Air discharge	Unit
USB interface	±4	±8	KV
USIM interface	±4	±8	KV
VBAT power supply	±4	±8	KV

5.4 Module IO Level

The C20QM module IO levels are as follows:

Table 5.3 Electrical Characteristics of C20QM Module

Parameter	Description	Minimum	Maximum
VIH	High level input voltage	0.65*VIO	VIO+0.3V
VIL	Low level input voltage	0.3V	0.35*VIO
VOH	High level output voltage	VIO-0.45V	VIO
VOL	Low level output voltage	0	0.45V

5.5 Power Supply

The C20QM module input power requirements are as follows:

Table 5.4 C20QM module Operating Voltage

Parameter	Minimum value	Typical value	Maximum value
Input Voltage	3.4V	3.8V	4.5V

The power-on time of any interface of the module must not be earlier than the boot time of the module, otherwise the module may be abnormal or damaged.

5.6 Power Consumption Characteristics

Table 5.5 LTE power consumption

Mode	Band	Rx CINR @ 80dBm	Sensitivity (dBm)	Current consumption @ 23dBm and @ 4 V			
				Typical	Tx Idle	Peak Tx @ Centre frequency	Unit
CAT 4	Band 1	15	-98	-	56	769	mA
	Band 3	15	-97	-	56	790	mA
	Band 5	15	-97	-	56	627	mA
	Band 7	15	-97	-	57	756	mA
	Band 8	15	-96	-	55	648	mA
	Band 18	15	-97	-	56	692	mA
	Band 19	15	-97	-	56	637	mA
	Band 20	15	TBD	-	55	614	mA
	Band 26	15	-97	-	56	605	mA
	Band 28	TBD	TBD	-	56	645	mA

	Band 40	16	-97	-	56	393	mA
	Band 38	TBD	TBD	-	55	506.9	mA
	Band 41	TBD	TBD	-	56	437	mA
2G	900 MHz	-	-	-	-	259	mA
	1800 MHz	-	-	-	-	247	mA
AT+CFUN=0				31.8	-	-	mA
SLEEP				1.2	-	-	mA
SHUTDOWN				15	-	-	μA
MODULE PEAK				-	-	1	mA

6 Structural and Mechanical Properties

6.1 C20QM module mechanical size

The figure below shows the top and bottom view of the module.

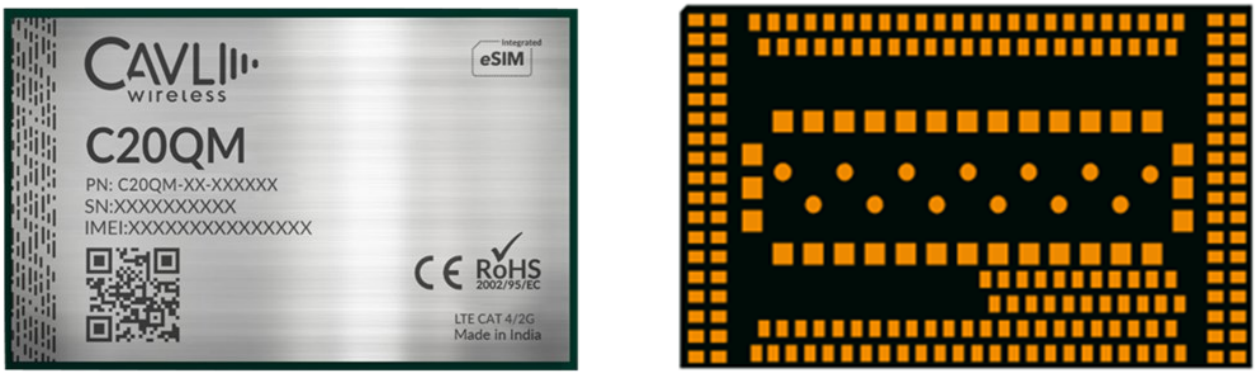


Figure 27 Top View and Bottom View of The Module

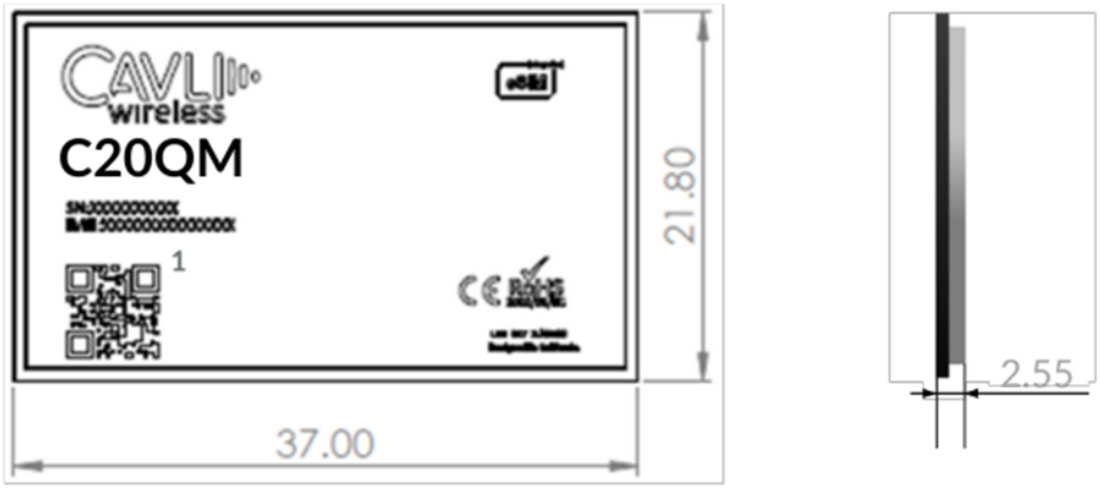


Figure 28 C20QM Module Dimensions

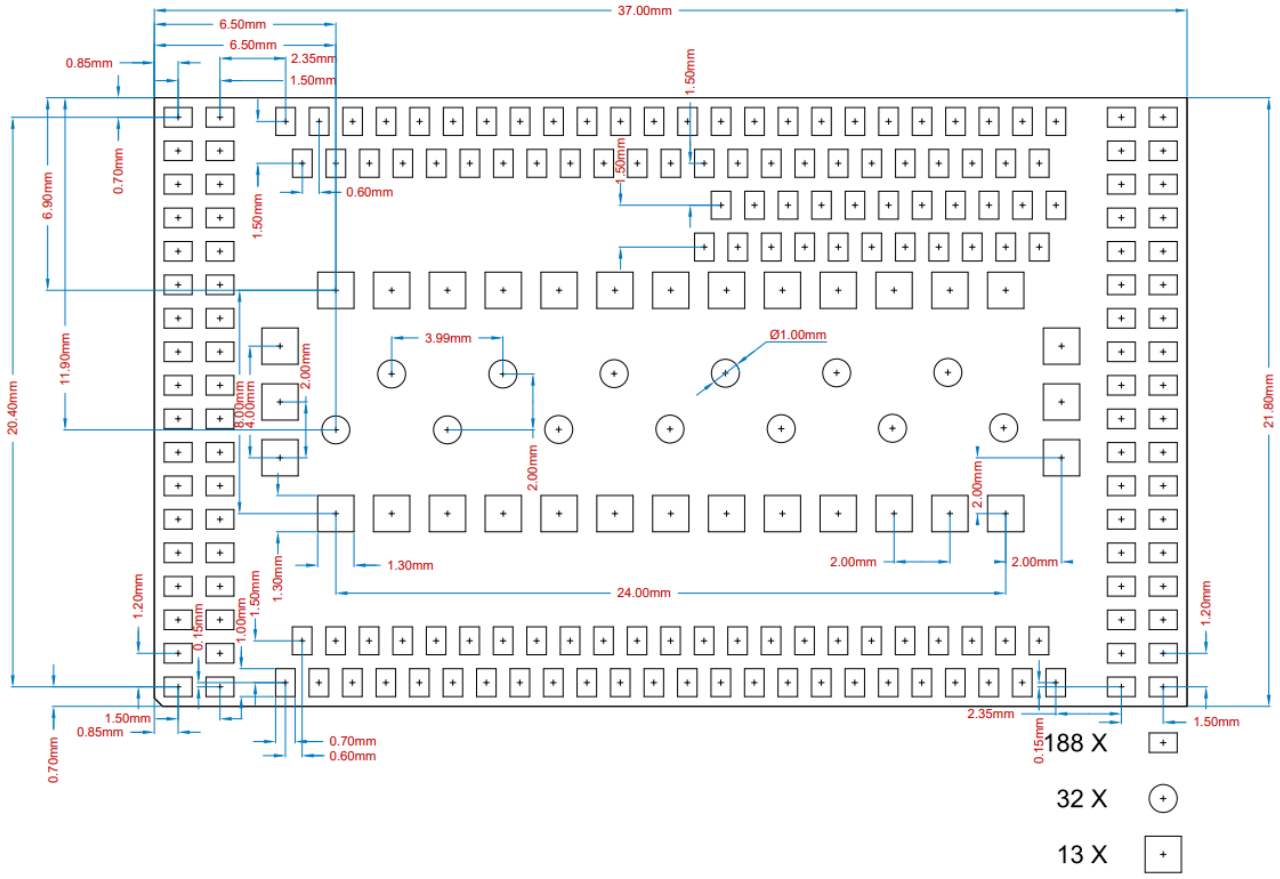
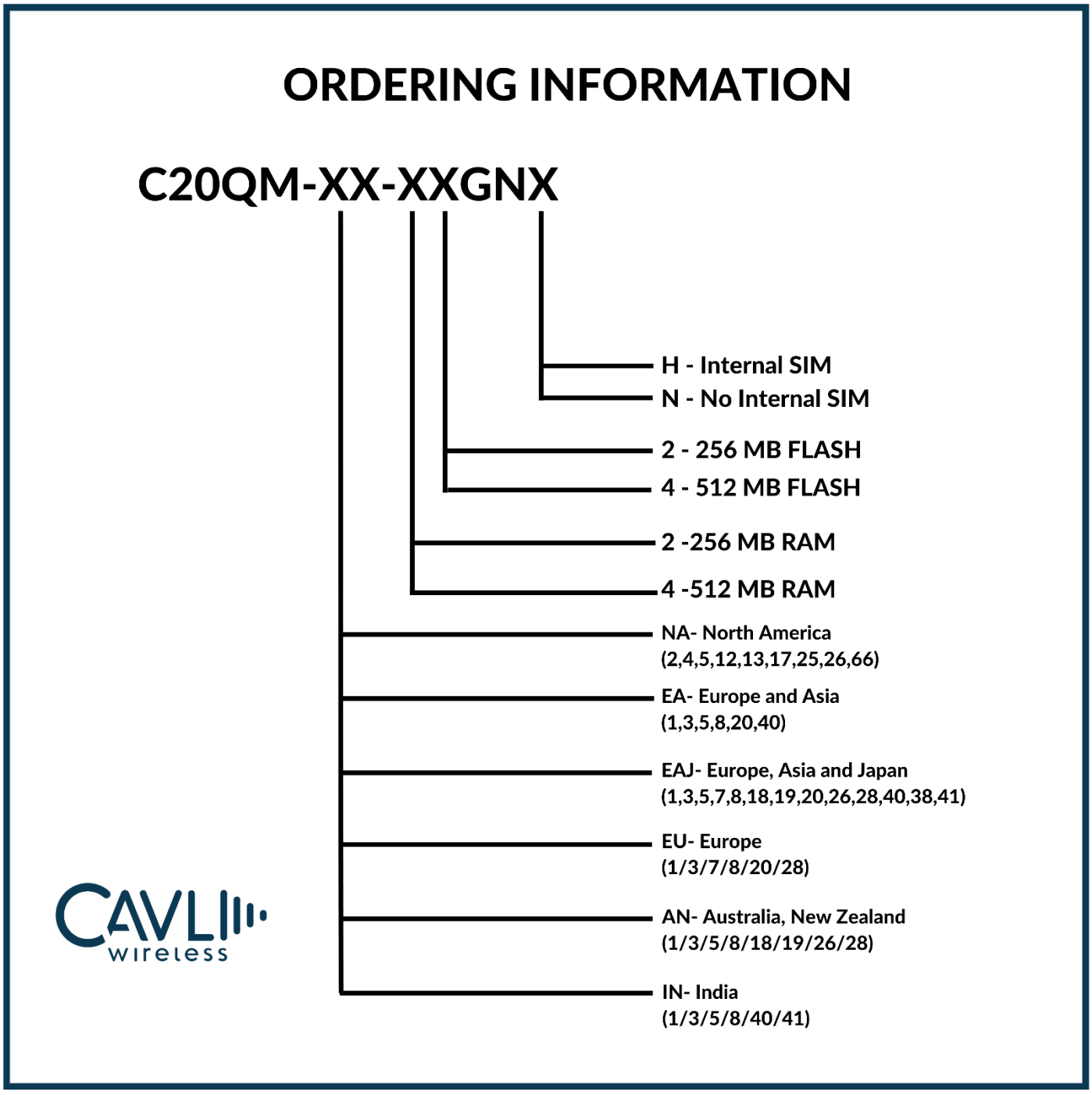


Figure 29 Pad Dimensions (Top view)

7 Ordering Information



8 Packaging and Production

8.1 Chapter Overview

- ✓ Module packaging and storage
- ✓ Production welding

8.2 Module Packaging and Storage

The C20QM module is packaged in a tape reel with 500 pcs per reel, shipped as a tape reel sealed bag.

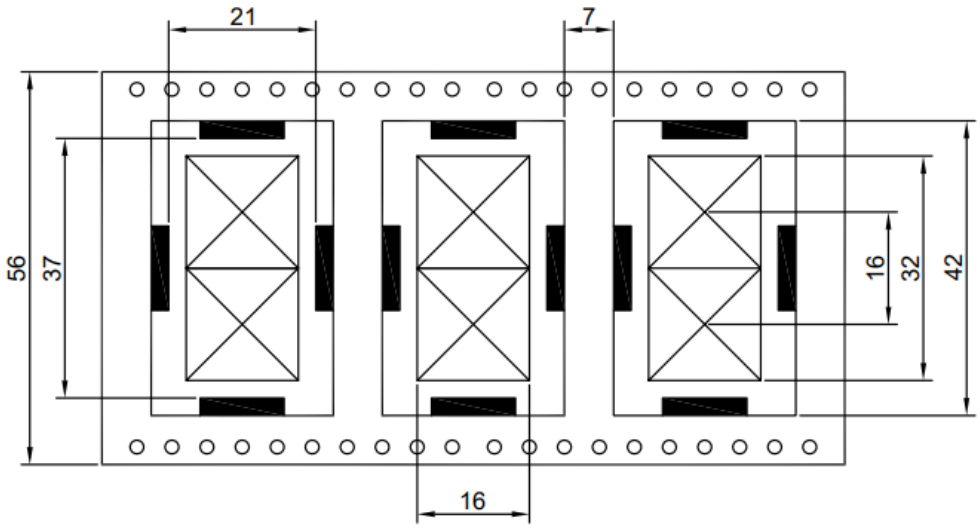


Figure 30 C20QM Tape Measurements (in mm)

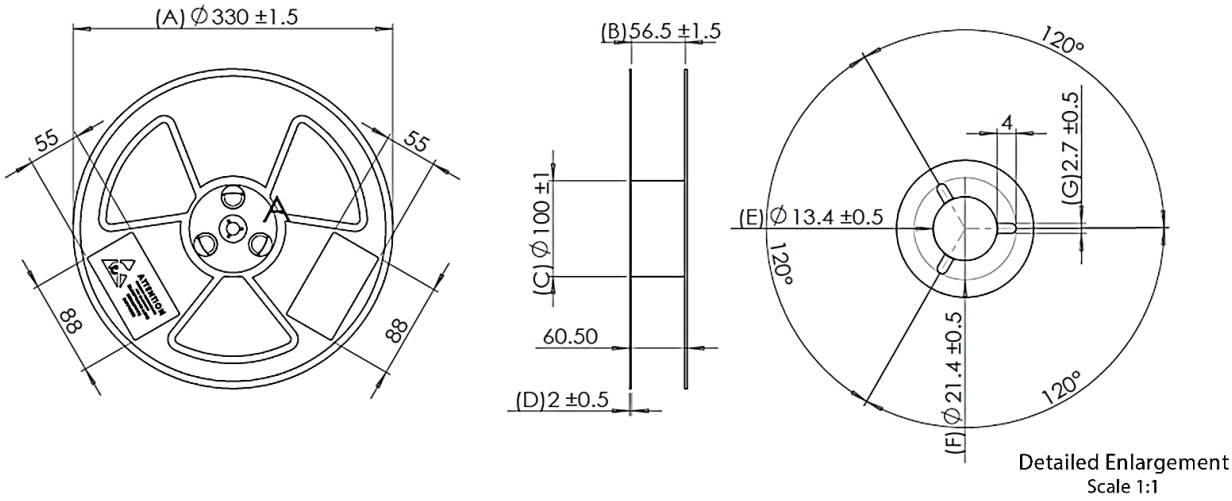


Figure 31 Reel Dimensions of C20QM (in mm)

The storage of the C20QM module is subject to the following conditions:

- ✓ The module has a moisture sensitivity rating of 3.
- ✓ When the ambient temperature is greater than 40 degrees Celsius and the air humidity is less than 90%, the module can be stored in a vacuum sealed bag for 12 months.
- ✓ When the vacuum sealed bag is opened, if the ambient temperature of the module is lower than 30 degrees Celsius and the air humidity is less than 60%, the factory can complete the patch within 72 hours, and the module can directly perform reflow soldering or other high temperature process.
- ✓ If the module is in other conditions, it needs to be baked before the patch.
- ✓ If the module needs to be baked, remove the module and bake for 48 hours at 125 degrees Celsius (allowing fluctuations of up to 5 degrees Celsius).

8.3 Production Welding

The C20QM module is packaged in an anti-static tray. The SMT wire body needs to be equipped with a Tray module. It is recommended to use a reflow oven above 7 temperature zones.

- ✓ To ensure the quality of the module paste, the thickness of the stencil corresponding to the pad portion of the C20QMmodule is recommended to be 0.18 mm.
- ✓ The recommended reflow temperature is 235~245oC, which cannot exceed 260oC.
- ✓ When the PCB is laid out on both sides, the LGA module layout must be machined on the 2nd side. Avoid

module falling parts, welding and welding, and poor internal welding of the module caused by the gravity of the module.

The recommended furnace temperature curve is shown below:

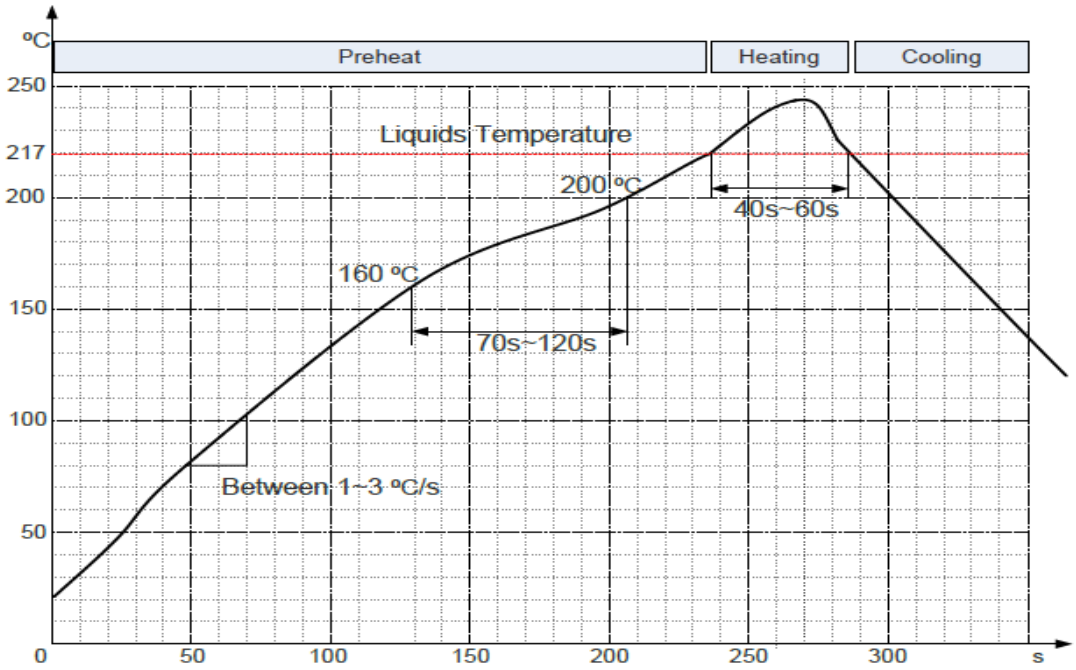


Figure 32 Reflow Soldering Temperature Graph

Table 8.1 Reflow Process Parameter Table

Warm zone	Time	Key parameter
Preheating zone (4℃~ 165℃)		Heating rate: 1℃/ s ~ 3℃ / s
Temperature zone (160℃～210℃)	（t1～t2）： 70s～120s	
Recirculation zone (> 217 ℃)	（t3～t4）： 40s～60s	Peak temperature: 235℃~ 245 ℃
Cooling zone	Cooling rate: 2℃/s ≤ Slope ≤ 5℃/s	

9 Appendix

9.1 Chapter Overview

- ✓ Abbreviations
- ✓ Safety and precautions

9.2 Abbreviations

Table 9.1 Abbreviations

Abbreviations	Full name
3GPP	Third Generation Partnership Project
AP	Access Point
AMR	Adaptive Multi-rate
BER	Bit Error Rate
CCC	China Compulsory Certification
CDMA	Code Division Multiple Access
CE	European Conformity
CSD	Circuit Switched Data
CTS	Clear to Send
DC	Direct Current
DTR	Data Terminal Ready
DL	Down Link
DTE	Data Terminal Equipment

DRX	Discontinuous Reception
EDGE	Enhanced Data Rate for GSM Evolution
EU	European Union
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FCC	Federal Communications Commission
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communication
HSDPA	High-Speed Downlink Packet Access
HSPA	Enhanced High Speed Packet Access
HSUPA	High Speed Up-link Packet Access
IMEI	International Mobile Equipment Identity
LED	Light-Emitting Diode
LTE	Long Term Evolution
NC	Not Connected
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PMU	Power Management Unit
PPP	Point-to-point protocol
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of the Use of Certain Hazardous Substances
SMS	Short Message Service
TIS	Total Isotropic Sensitivity

TVS	Transient Voltage Suppressor
TX	Transmitting Direction
UART	Universal Asynchronous Receiver-Transmitter
UMTS	Universal Mobile Telecommunications System
USIM	Universal Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WWAN	Wireless Wide Area Network

9.3 Safety and Precautions

In order to use the wireless device safely, the terminal device informs the user of the relevant safety information:

- ✓ **Interference:** When the use of wireless devices is prohibited or the use of the device may cause interference and security of the electronic device, turn off the wireless device. Because the terminal will send and receive RF signals when it is powered on. It can interfere with TV, radio, computer or other electrical equipment.
- ✓ **Medical equipment:** In medical and health care facilities where the use of wireless devices is prohibited in the express text, please follow the regulations of the site and turn off the device. Some wireless devices may interfere with the medical device, causing the medical device to malfunction or cause errors. If interference occurs, turn off the wireless device and consult a physician.
- ✓ **Flammable and explosive areas:** In flammable and explosive areas, please turn off your wireless device and follow the relevant label instructions to avoid an explosion or fire. For example; gas stations, fuel zones, chemical products areas, chemical transportation and storage facilities, areas with explosion hazard signs, areas with “turn off radio equipment” signs, etc.
- ✓ **Traffic Safety:** Please comply with local laws or regulations in your country or region regarding the use of wireless devices when driving a vehicle.
- ✓ **Aviation Safety:** When flying, please follow the airline's regulations and regulations regarding the use of wireless devices. Before taking off, turn off the wireless device to prevent wireless signals from interfering with aircraft control signals.
- ✓ **Environmental Protection:** Please comply with local laws regarding the handling of equipment packaging materials, equipment or accessories, and support recycling operations.
- ✓ **Emergency call:** This device uses wireless signals for propagation. Therefore, there is no guarantee that the network can be connected in all situations, so in an emergency this wireless device cannot be used as the only contact method.