MCP6C26

Zero-Drift, 36V Current Sense Amplifier

Features

- Single Amplifier: MCP6C26
  - Gains: 50, 100 and 200 V/V
- Bidirectional or Unidirectional
- Input (“Common Mode”) Voltages:
  - -0.2V to +36V, Specified
  - -5V to +39.5V, Survival
- Power Supply
  - 2.7V to 5.5V
  - Single or Dual (Split) Supplies
- High DC Precision
  - V_{OS}: ±15 µV (typical)
  - CMRR: 129 dB (typical at G_{DM} = 200)
  - PSRR: 136 dB (typical at G_{DM} = 200)
  - Gain Error: ±0.05% (typical)
- POR Protection
  - LV POR for V_{DD}
- Gain-Bandwidth Product: 9 MHz (typical)
- Supply Current
  - I_{DD} = 65 µA (typical)
- Specified Temperature Range
  - -40°C to +125°C

Typical Applications

- DC/DC Converters
- Battery Management
- USB Power Delivery
- Uninterruptible Power Supplies
- Differential Sensor Conditioning

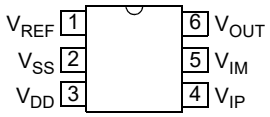
General Description

The Microchip Technology Inc. MCP6C26 current sense amplifier is offered with preset gains of 50, 100 and 200 V/V. The input voltage range (V_{IP} and V_{IM}) is -0.2V to +36V. The Differential-Mode input range ($V_{DM} = V_{IP} - V_{IM}$) supports unidirectional and bidirectional applications. The power supply can be set between 2.7V and 5.5V. Parts come in an SC70 package and are specified over the -40°C to +125°C (E-Temp) range.

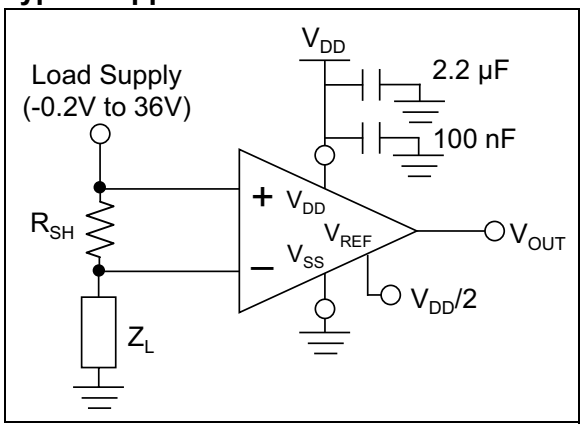
The architecture includes an internal Zero-Drift op amp and precision internal resistors. It supports very low input errors and allows current sense designs to use shunt resistors of lower value (with lower power dissipation).

Package Types (Top View)

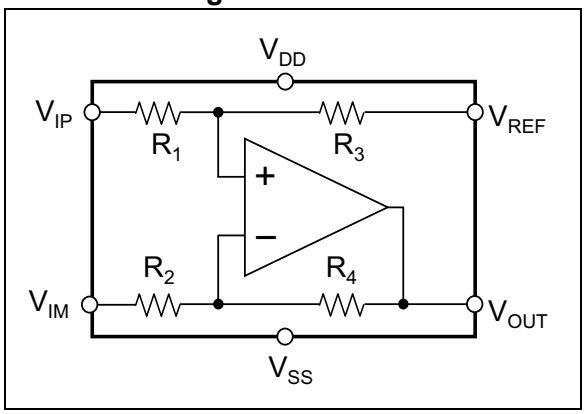
MCP6C26
SC70



Typical Application Circuit



Functional Diagram



Gain Options

Table 1 shows key specifications that differentiate between the three different differential gain (G_{DM}) options. See **Section 1.0 "Electrical Characteristics"**, **Section 6.0 "Packaging Information"** and the **Product Identification System** for further information on the G_{DM} options available.

TABLE 1: KEY DIFFERENTIATING SPECIFICATIONS

Part No.	G_{DM} (V/V) Nom.	g_E (±%)	V_{OS} (±µV) Max.	TC_1 (±nV/°C) Max. (Note 1)	CMRR (dB) Min. (Note 2)	PSRR (dB) Min.	GBWP (MHz) Typ.	BW (kHz) Typ.
MCP6C26-050	50	0.5	90	265	102	100	9	180
MCP6C26-100	100		75	240	102			90
MCP6C26-200	200		65	225	105			45

Note 1: TC_1 limits are by design and characterization only; not tested in production. TC_1 covers the Extended Temperature Range (-40°C to +125°C or E-Temp).

2: The common mode input range is 0V to 36V.

Figure 1, Figure 2 and Figure 3 show input offset voltage versus temperature for the three gain options (G_{DM} = 50, 100 and 200 V/V).

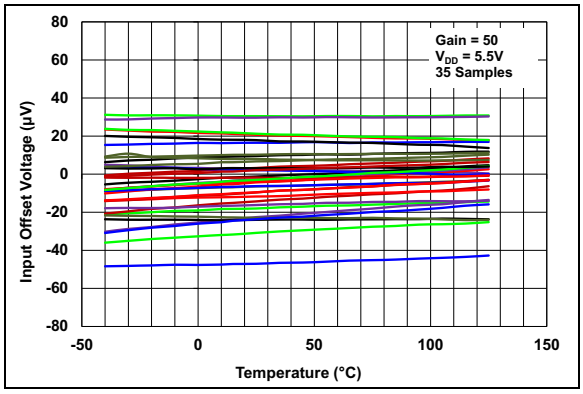


FIGURE 1: *Input Offset Voltage vs. Temperature, G_{DM} = 50 V/V.*

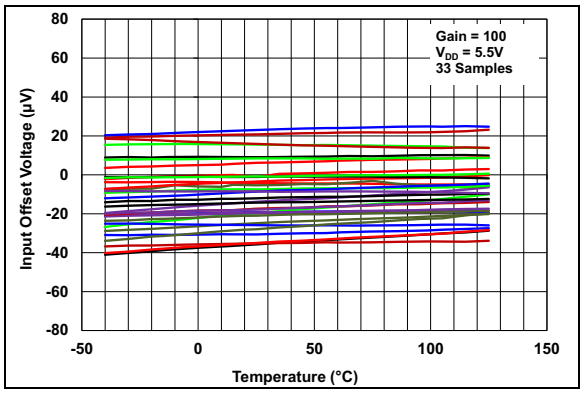


FIGURE 2: *Input Offset Voltage vs. Temperature, G_{DM} = 100 V/V.*

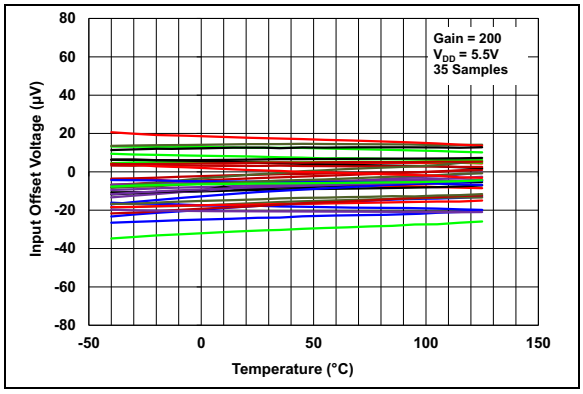


FIGURE 3: *Input Offset Voltage vs. Temperature, G_{DM} = 200 V/V.*

The MCP6C26's CMRR supports applications in noisy environments. Figure 4 shows how CMRR is high, even for frequencies near 100 kHz.

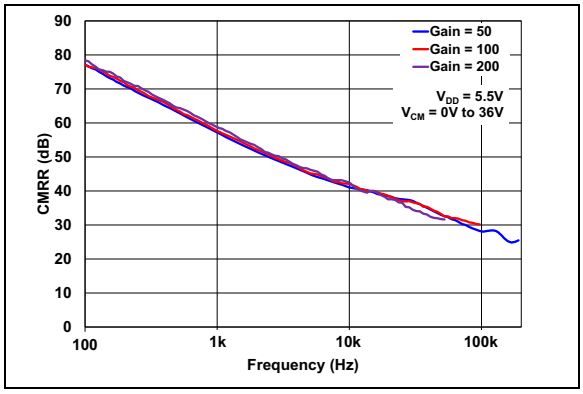


FIGURE 4: *CMRR vs. Frequency.*

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

V_{DD} - V_{SS} ..... 0V to +6.0V
Current at Input Pins (Note 1) ..... ±2 mA
Analog Inputs (V_{IP} and V_{IM}) (Note 1)(Note 2) ..... -5.0V to +39.5V
All Other Inputs and Outputs ..... V_{SS} - 0.3V to V_{DD} + 0.3V
Input Difference Voltage (V_{DM}) (Note 1)(Note 2) ..... ±39.5V
Output Short-Circuit Current ..... Continuous
Current at Output and Supply Pins ..... ±30 mA
Storage Temperature ..... -65°C to +150°C
Maximum Junction Temperature (Note 2) ..... +155°C
ESD protection (HBM, CDM) ..... ≥ 2 kV, 2 kV

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: These voltage and current ratings are physically independent; each required condition must be enforced by the user (see **Section 5.1.2 “Input Voltage/Current Limits”**).

2: This condition is intended for intermittent use only.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.7V to 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF; see Figure 1-5 and Figure 1-6.

Parameter	Sym.	Min.	Typ.	Max.	Units	Gain	Conditions
Input Offset (V_{IP} = V_{IM})							
Input Offset Voltage	V_{OS}	-90	±20	90	µV	50	
		-75	±15	75		100	
		-65	±15	65		200	
V_{OS} Drift, Linear Temp. Co.	TC_1	-265	-35	265	nV/°C	50	T_A = -40°C to +125°C, (Note 1, Note 2)
		-235	-25	235		100	
		-225	-20	225		200	
Power Supply Rejection Ratio	PSRR	100	126	—	dB	50	V_{DD} = 2.7V to 5.5V
			131			100	
			136			200	
Input Current and Impedance (V_{IP} and V_{IM})							
V_{IP}'s Input Bias Current	I_{BP}	-100	±60	100	µA	All	
V_{IM}'s Input Bias Current	I_{BM}	-100	±60	100	µA	All	
Input Common-Mode Voltage (V_{CM})							
Common-Mode Rejection Ratio	CMRR	120	132	—	dB	50	V_{DD} = 2.7V to 5.5V, V_{CM} = 0V to 36V
		123	138			100	
		129				200	
Input Common-Mode Voltage Range (Low)	V_{CML}	—	—	-0.2	V	All	
Input Common-Mode Voltage Range (High)	V_{CMH}	36	—	—	V	All	
Reference Voltage (V_{REF})							
Gain Resistance	R_1, R_2	—	20	—	kΩ	50	
			10			100	
			5			200	
	R_3, R_4	—	1	—	MΩ	All	
Reference Voltage Rejection Ratio	CMRR2	100	125	—	dB	All	V_{REF} = 0.2V to 4.8V
V_{REF} Voltage Range	V_{REF}	-0.2	—	V_{DD}+0.2	V	All	
Differential Input (V_{DM})							
Differential Gain	G_{DM}	50			V/V	50	MCP6C26-050
		100				100	MCP6C26-100
		200				200	MCP6C26-200
Differential Gain Error	g_E	-0.5	±0.05	+0.5	%	All	
Differential Gain Drift	$\Delta g_E/\Delta T_A$	—	±5	—	ppm/°C	All	$G_{DM}V_{DM}$ = 2.5V (Note 1)
Differential Nonlinearity (Note 3)	INL_{DM}	—	±100	—	ppm	All	V_{DM} = ±10 mV (Note 1)
Differential Voltage (Low)	V_{DML}	—	—	$(V_{SS}-0.2)/G_{DM}$	V	All	

Note 1: Set by design and characterization.

2: See the discussion in **Section 1.5.2, Input Offset Related Errors**.

3: See **Section 1.5, Explanation of DC Error Specifications**.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.7V to 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF; see Figure 1-5 and Figure 1-6.

Parameter	Sym.	Min.	Typ.	Max.	Units	Gain	Conditions
Differential Voltage (High)	V_{DMH}	5.7/G_{DM}	—	—	V	All	
Output (V_{OUT})							
Minimum Output Voltage Swing	V_{OL}	—	45	110	mV	All	
Maximum Output Voltage Swing	V_{DD} – V_{OH}	—	80	160	mV	All	
Output Short Circuit Current	I_{SC}	—	±20	—	mA	All	
Power Supplies (V_{DD}, V_{SS} and V_{IP})							
Low Supply Voltage	V_{DD}	2.7	—	5.5	V	All	
Quiescent Current at V_{SS}	I_{SS}	-150	-120	-90	µA		
Quiescent Current at V_{DD}	I_{DD}	40	65	90			
POR Trip Voltages, Low-Side (V_{DD})	V_{PL}	—	1.9	—	V	All	POR turns off (V_{DD} ↓)
	V_{PH}	—	1.95	—			POR turns on (V_{DD} ↑)

Note 1: Set by design and characterization.
2: See the discussion in **Section 1.5.2, Input Offset Related Errors**.
3: See **Section 1.5, Explanation of DC Error Specifications**.

TABLE 1-2: AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.7V to 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF; see Figure 1-7.

Parameter	Sym.	Min.	Typ.	Max.	Units	Gain	Conditions
AC Response							
Bandwidth	BW	—	180	—	kHz	50	$G_{DM}V_{DM}$ = 0.1V_{p-p}
		—	90	—		100	
		—	45	—		200	
V_{DM} Slew Rate	SR	—	1.3	—	V/µs	All	$G_{DM}V_{DM}$ Step = V_{DD} – 0.5V
Noise							
Input Noise Voltage Density	e_{ni}	—	42	—	nV/√Hz	50	f = 1 kHz (Note 1)
		—	36	—		100	
		—	32	—		200	
Power Up/Down							
Power On Time (V_{DD} ↑), V_{OUT} Settles	t_{PON}	—	60	—	µs	All	V_{DD} = 0V to 4.0V, V_L = 0V, 90% of V_{OUT} change
Power Off Time (V_{DD} ↓), V_{OUT} Settles	t_{POFF}	—	60	—	µs	All	V_{DD} = 4.0V to 0V, V_L = 0V, 90% of V_{OUT} change
Step Response							
Inverting Input Overdrive Timing	t_{IRDIM}	—	65	—	µs	All	
Noninverting Input Overdrive Timing	t_{IRDIP}	—	85	—	µs	All	
Large Common Mode Step Recovery Time	t_{CMS}	—	70	—	µs	All	10V V_{CM} Step

Note 1: See Figure 2-33 for the noise density over a wider frequency range.

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ and C_L = 30 pF						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Specified Temperature Range	T_A	-40	—	+125	°C	Note 1
Operating Temperature Range		-40	—	—		Note 1
Storage Temperature Range		-60	—	+150		No power
Thermal Resistance, SC-70	θ_{JA}	—	209	—	°C/W	

Note 1: Operation must not cause T_J to exceed the Absolute Maximum Junction Temperature specification (+155°C), which is not intended for continuous use. See **Section 4.1.5, Temperature Performance** for design tips.

1.3 Simplified Diagrams

1.3.1 VOLTAGE RANGE DIAGRAMS

These ranges are constant across temperature.

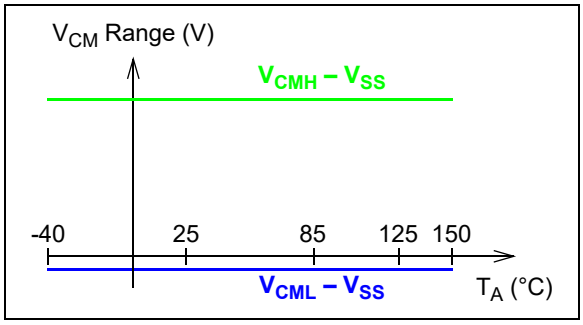


FIGURE 1-1: *Common-Mode Input Voltage Range vs. Temperature.*

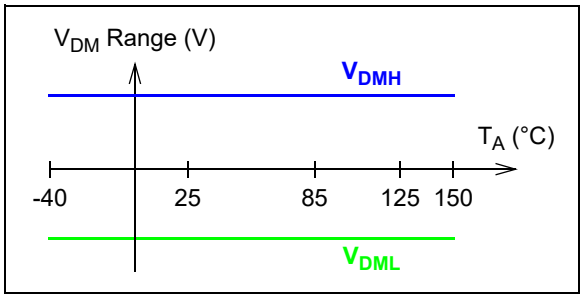


FIGURE 1-2: *Differential Input Voltage Range vs. Temperature.*

1.3.2 TIMING DIAGRAMS

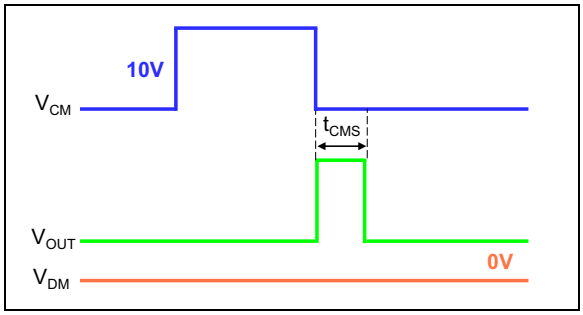


FIGURE 1-3: *Large Common-Mode Voltage Step Response.*

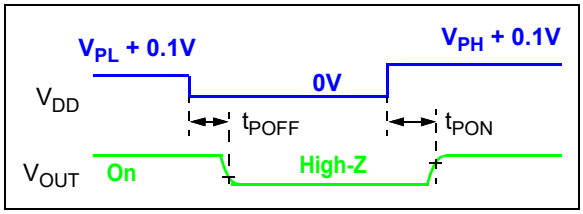


FIGURE 1-4: *V_{OUT} Power On/Off Timing Diagram.*

1.4 Simplified Test Circuits

1.4.1 V_{OS} TEST CIRCUIT

Figure 1-5 tests the MCP6C26's input offset errors (V_{OS}, 1/CMRR, 1/CMRR2 and 1/PSRR etc.). V_{OUT} is filtered and amplified, before measuring the result. Note that V_{CM} is equal to $(V_{IP} + V_{IM})/2$.

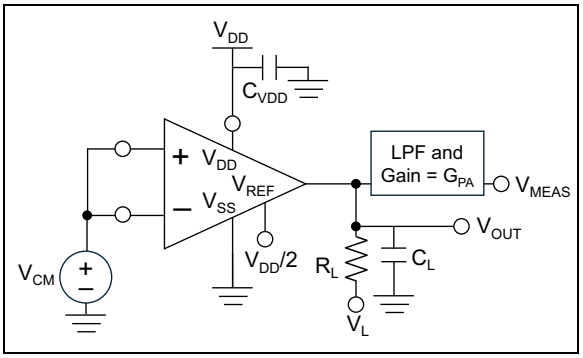


FIGURE 1-5: *Input Offset Test Circuit for the MCP6C26.*

When MCP6C26 is in its normal range of operation, the DC output voltages are (V_E is the sum of input offset errors and g_E is the gain error, refer to Equation 1-5):

EQUATION 1-1:

$$G_{DM} = \text{DM Gain}$$
$$V_{OUT} = G_{DM}(1 + g_E)V_E + V_{REF}$$
$$V_{MEAS} = G_{PA}V_{OUT}$$

1.4.2 DC DIFFERENTIAL GAIN TEST CIRCUIT

Figure 1-6 is used for testing the differential gain error, nonlinearity and input voltage range (g_E, INL_{DM}, V_{DML} and V_{DMH}). We compare V_{MEAS} with the ideal V_{OUT}, then extract the above parameters.

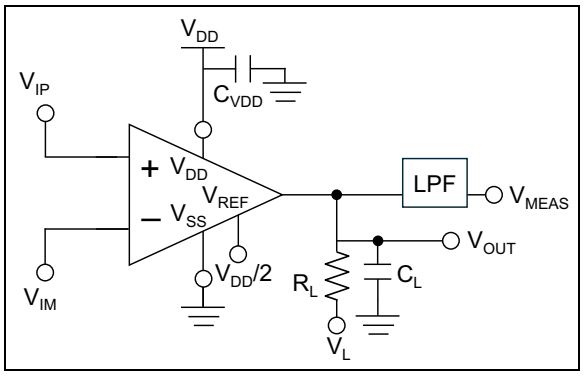


FIGURE 1-6: *Differential Gain Test Circuit.*

When measuring the differential input range, all of the voltages must be in range except V_{DM} ($V_{DM} = V_{IP} - V_{IM}$).

When measuring differential errors (g_E, $\Delta g_E/\Delta T_A$ and INL_{DM}), all voltages are held constant, except V_{DM}.

1.4.3 AC GAINS TEST CIRCUIT

Figure 1-7 is used for testing the INA's different AC gains. The AC voltages are:

- v_{out} is the AC output
- v_{cm} is the AC Common-mode input, used for CMRR plots
- v_{dm} is the AC differential input, used for G_{DM} plots (also for CMRR and PSRR)
- v_{dd} and v_{ss} are the AC supply inputs, used for PSRR plots (including PSRR+ and PSRR-)
- V_{ref} is the AC voltage reference input, used for CMRR2 plots.

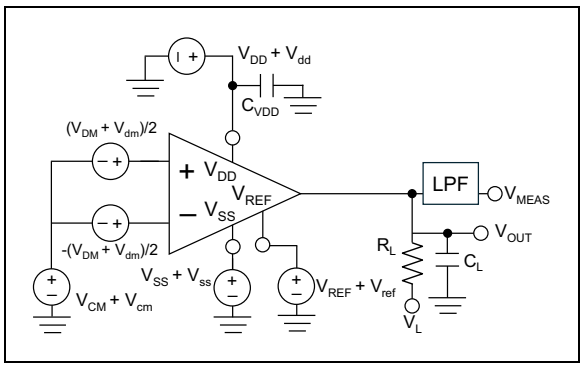


FIGURE 1-7: *AC Gain Test Circuit.*

1.5 Explanation of DC Error Specifications

1.5.1 LINEAR RESPONSE MODEL

When the inputs and the output are in their normal ranges, and the nonlinear errors are negligible, the output voltage (V_{OUT}) is:

EQUATION 1-2:

$$V_{OUT} = V_{REF} + G_{DM}(1 + g_E)(V_{DM} + V_E)$$

V_{DM} is the input voltage. V_E is the sum of input offset errors (due to V_{OS}, PSRR, CMRR, CMRR2, TC_1, TC_2, etc.). g_E is the gain error (G_{DM} is the nominal gain).

1.5.2 INPUT OFFSET RELATED ERRORS

When V_{DM} = 0V, the linear response model for V_{OUT} becomes:

EQUATION 1-3:

$$V_{OUT} = V_{REF} + G_{DM}(1 + g_E)V_E$$

The input offset error (V_E) is extracted from input offset measurements (see **Section 1.4.1 "VOS Test Circuit"**):

EQUATION 1-4:

$$V_E = \frac{V_{OUT} - V_{REF}}{G_{DM}(1 + g_E)}$$

It is usually assumed that $g_E = 0$, in Equation 1-4, when extracting V_E. The result is accurate enough, since g_E is so low.

V_E has several terms, which assume a linear response to changes in V_{DD}, V_{SS}, V_{CM} and V_{REF}.

EQUATION 1-5:

$$V_E = V_{OS} + \frac{\Delta V_{DD} - \Delta V_{SS}}{PSRR} + \frac{\Delta V_{IP}}{CMRR} + \frac{\Delta V_{REF}}{CMRR2} + \Delta T_A TC_1$$

Where:

PSRR, CMRR and CMRR2 are in units of V/V
$\Delta T_A = T_A - 25°C$ with units of °C
$V_{DM} = 0$

1.5.3 INPUT COMMON-MODE AND DIFFERENTIAL-MODE VOLTAGE NONLINEARITY

The input offset error (V_E) changes nonlinearly with V_{CM}. Figure 1-8 shows the MCP6C26's V_E vs. V_{CM}, as well as a linear fit line (V_{E_LIN}), that goes through the center point (V_C, V_2) and has the same slope as the end points. The nonlinear error is the maximum difference between the two, with the appropriate sign.

The differential-mode voltage nonlinearity is treated the same way as the common-mode voltage nonlinearity (i.e., the x-axis becomes V_{DM}).

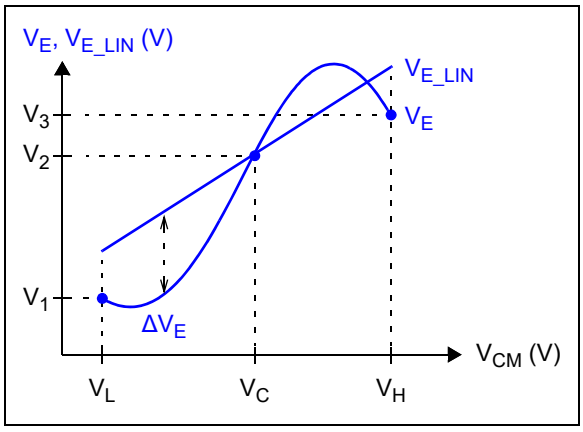


FIGURE 1-8: *Input Offset Error vs. Common-Mode or Differential-Mode Input Voltage.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.7V to 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF; see Figure 1-5, Figure 1-6 and Figure 1-7.

2.1 DC Precision

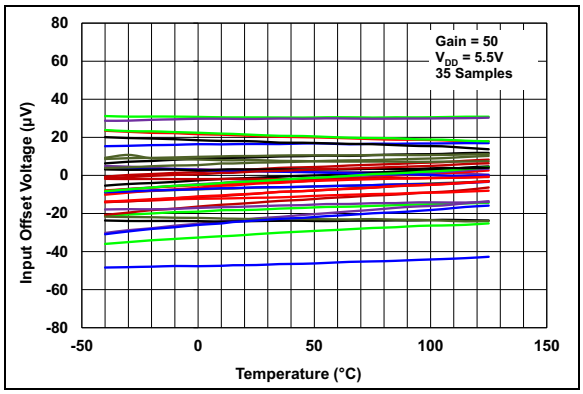


FIGURE 2-1: *Input Offset Voltage vs. Temperature, G_{DM} = 50 V/V.*

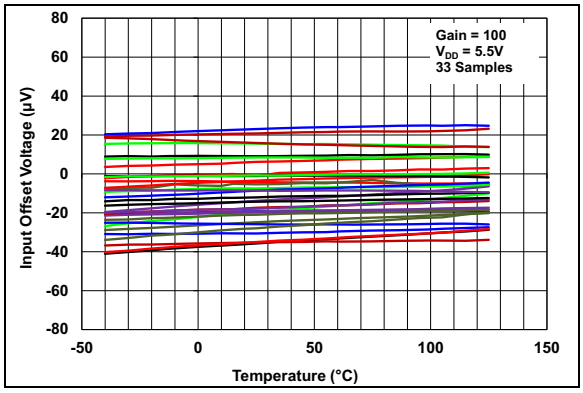


FIGURE 2-2: *Input Offset Voltage vs. Temperature, G_{DM} = 100 V/V.*

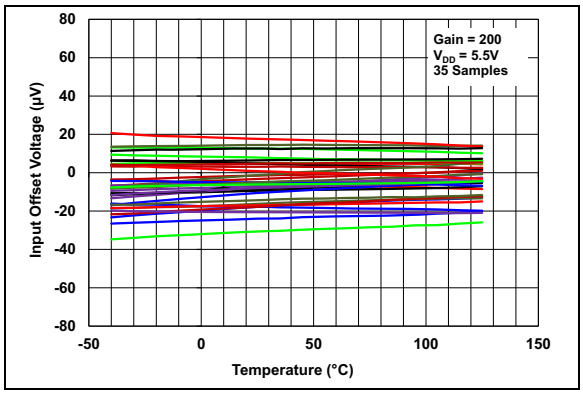


FIGURE 2-3: *Input Offset Voltage vs. Temperature, G_{DM} = 200 V/V.*

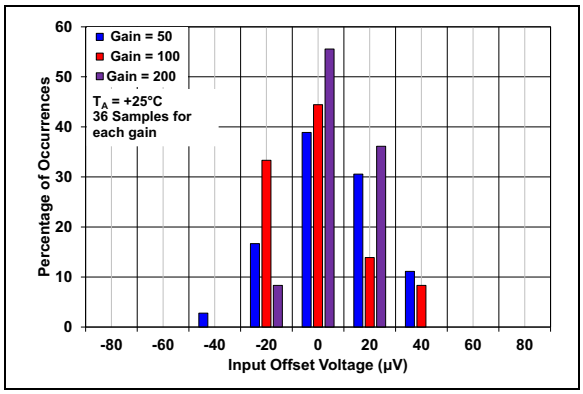


FIGURE 2-4: *Input Offset Voltage.*

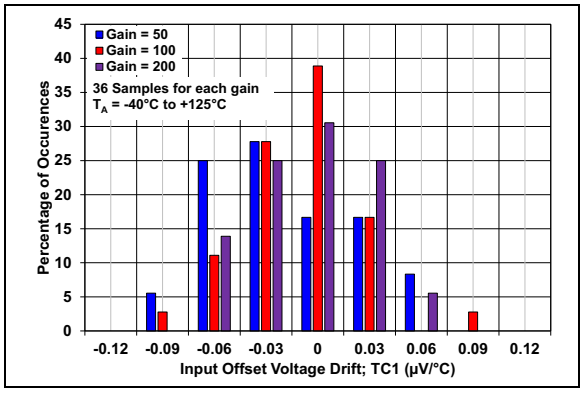


FIGURE 2-5: *Linear Input Offset Voltage Drift.*

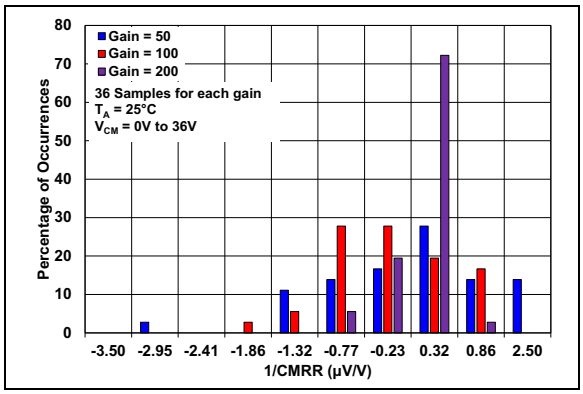


FIGURE 2-6: *1/CMRR.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.7V to 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF; see Figure 1-5, Figure 1-6 and Figure 1-7.

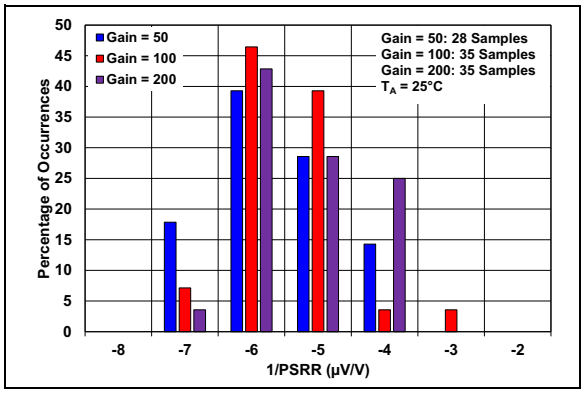


FIGURE 2-7: *1/PSRR.*

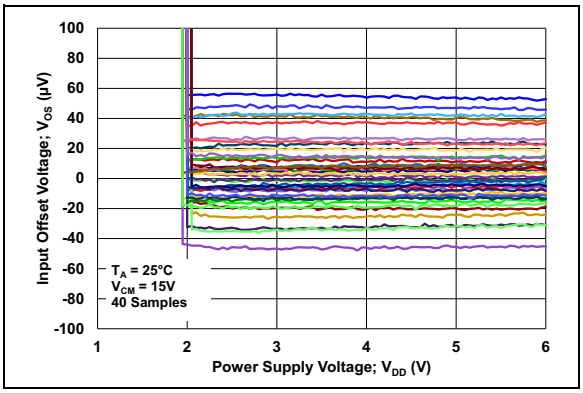


FIGURE 2-10: *Input Offset Voltage vs. Power Supply Voltage, with G_{DM} = 50.*

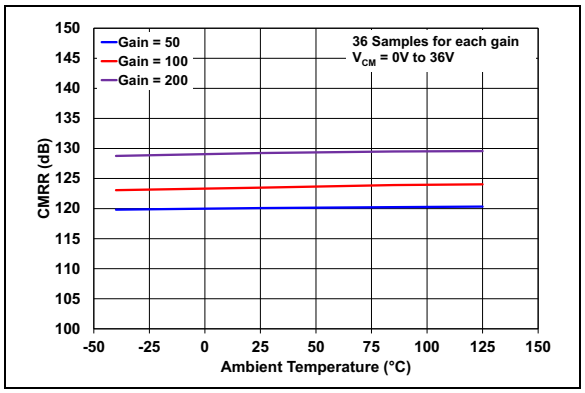


FIGURE 2-8: *CMRR vs. Ambient Temperature.*

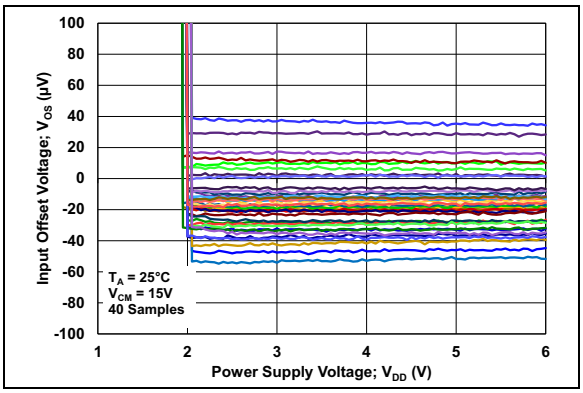


FIGURE 2-11: *Input Offset Voltage vs. Power Supply Voltage, with G_{DM} = 100.*

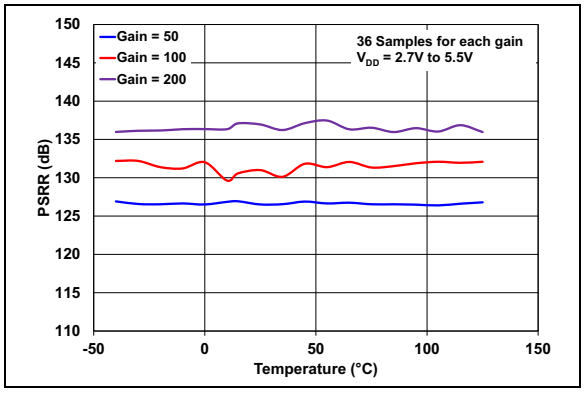


FIGURE 2-9: *PSRR vs. Ambient Temperature.*

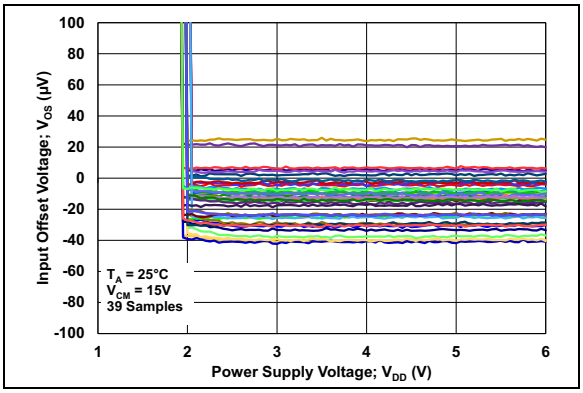


FIGURE 2-12: *Input Offset Voltage vs. Power Supply Voltage, with G_{DM} = 200.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.7V to 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 30 pF; see Figure 1-5, Figure 1-6 and Figure 1-7.

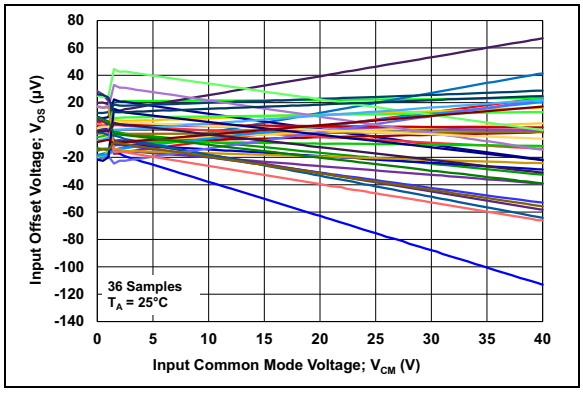


FIGURE 2-13: *Input Offset Voltage vs. Common-Mode Input Voltage, with G_{DM} = 50.*

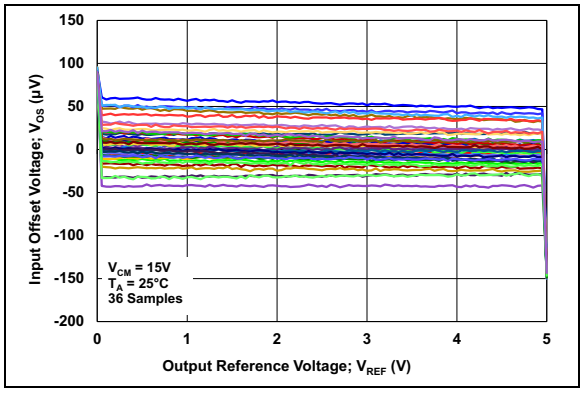


FIGURE 2-16: *Input Offset Voltage vs. Reference Voltage, with G_{DM} = 50.*

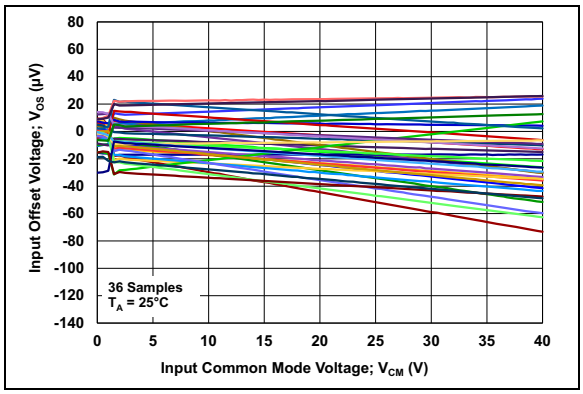


FIGURE 2-14: *Input Offset Voltage vs. Common-Mode Input Voltage, with G_{DM} = 100.*

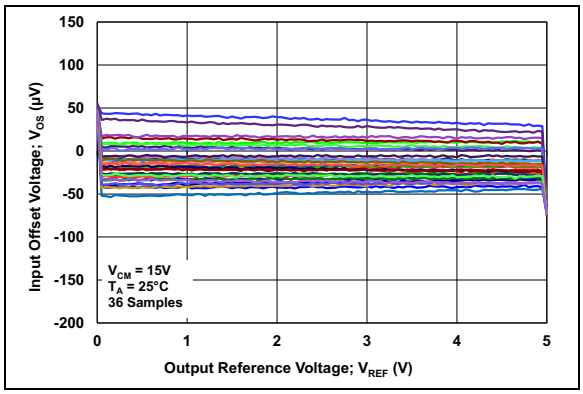


FIGURE 2-17: *Input Offset Voltage vs. Reference Voltage, with G_{DM} = 100.*

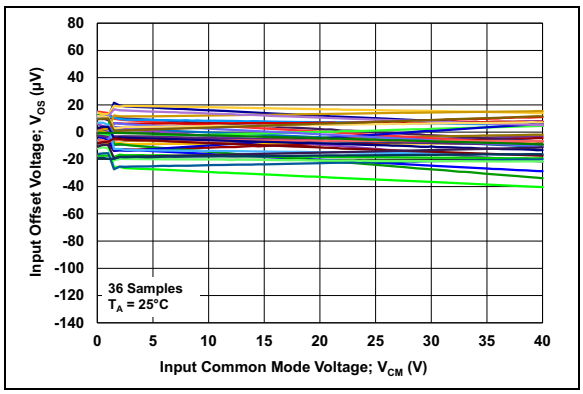


FIGURE 2-15: *Input Offset Voltage vs. Common-Mode Input Voltage, with G_{DM} = 200.*

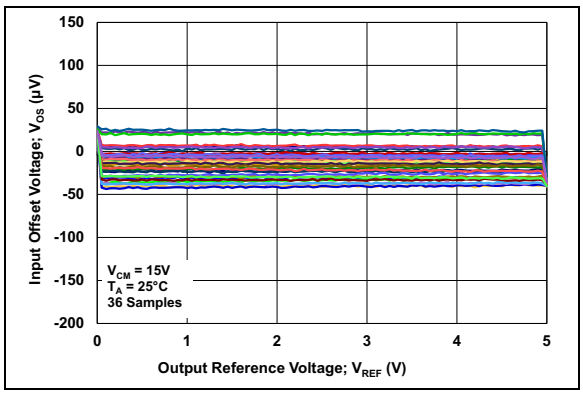


FIGURE 2-18: *Input Offset Voltage vs. Reference Voltage, with G_{DM} = 200.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.7V to 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF; see Figure 1-5, Figure 1-6 and Figure 1-7.

2.2 Other DC Voltages and Currents

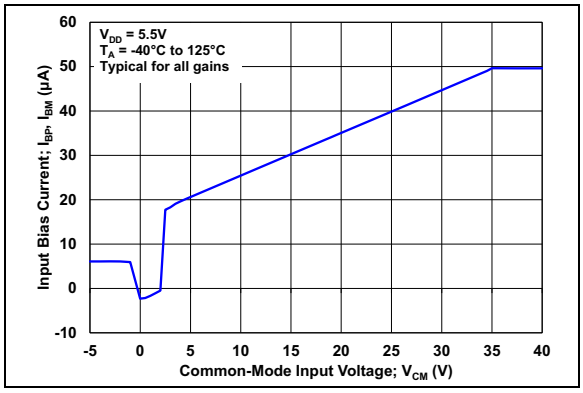


FIGURE 2-19: *Input Bias Current (I_{BP}, I_{BM}) vs. Input Common-Mode Voltage.*

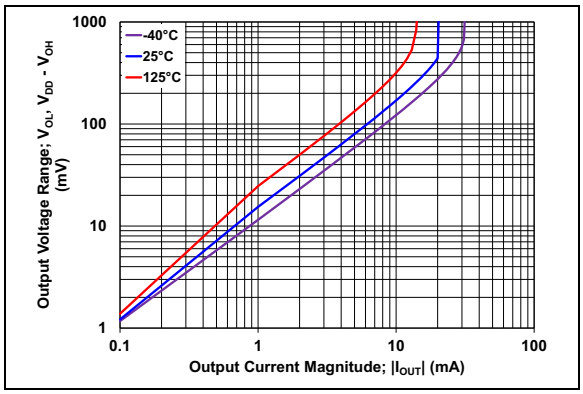


FIGURE 2-20: *Output Voltage Range vs. Output Current.*

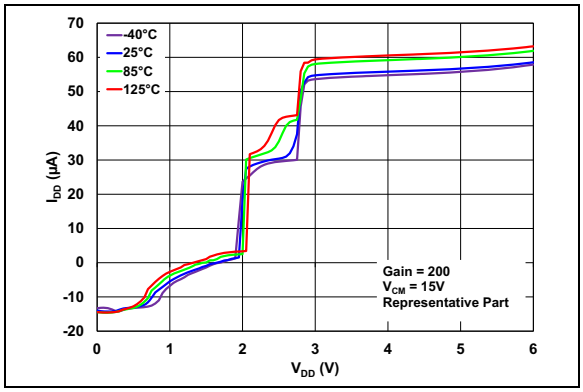


FIGURE 2-21: *Supply Current vs. Power Supply Voltage, Ambient Temperature.*

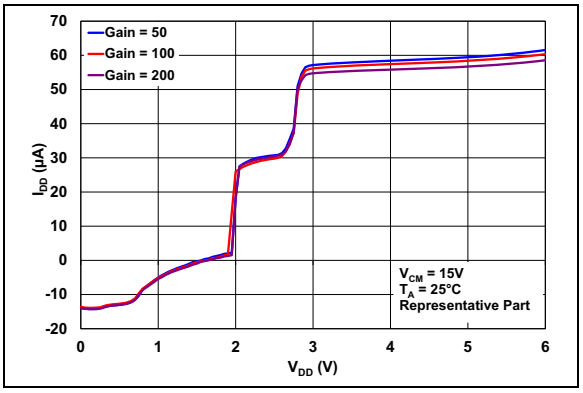


FIGURE 2-22: *Supply Current vs. Power Supply Voltage, Gain.*

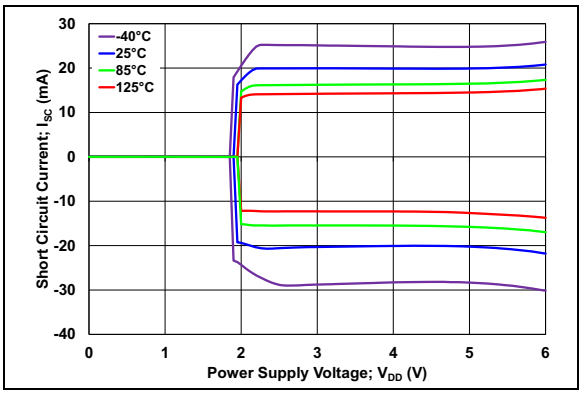


FIGURE 2-23: *Output Short Circuit Current vs. Power Supply Voltage.*

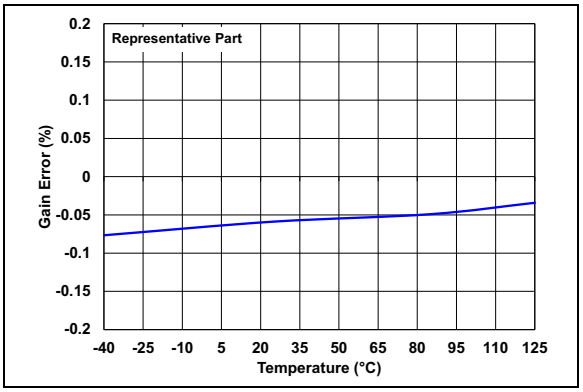


FIGURE 2-24: *Gain Error vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.7V to 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF; see Figure 1-5, Figure 1-6 and Figure 1-7.

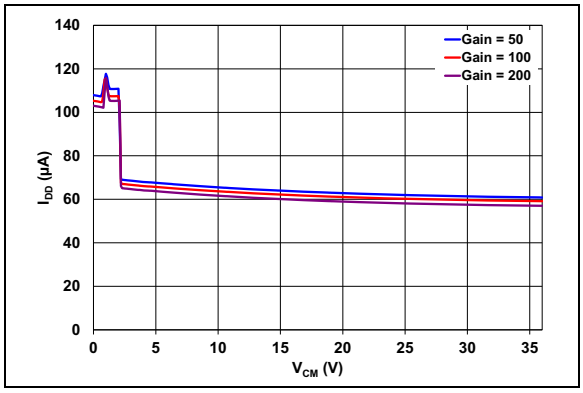


FIGURE 2-25: *Supply Current vs. Input Common-Mode Voltage.*

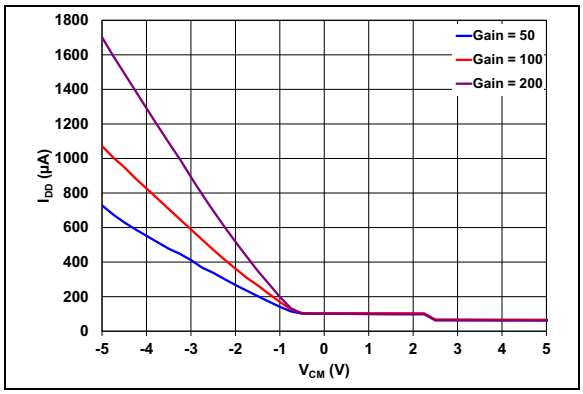


FIGURE 2-26: *Supply Current vs. Input Common-Mode Voltage (Survival Region).*

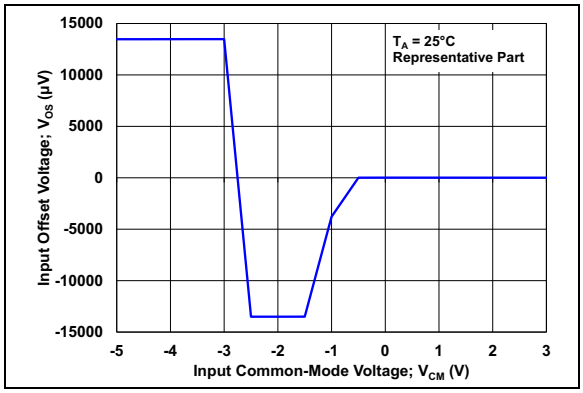


FIGURE 2-27: *Input Offset Voltage vs. Input Common-Mode Voltage (Survival Region).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.7V to 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF; see Figure 1-5, Figure 1-6 and Figure 1-7.

2.3 Frequency Response

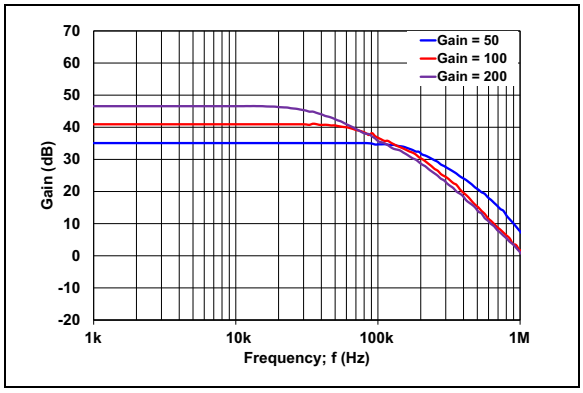


FIGURE 2-28: *Gain vs. Frequency.*

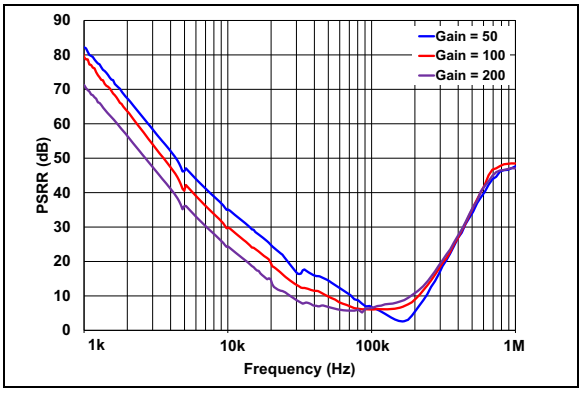


FIGURE 2-31: *PSRR vs. Frequency.*

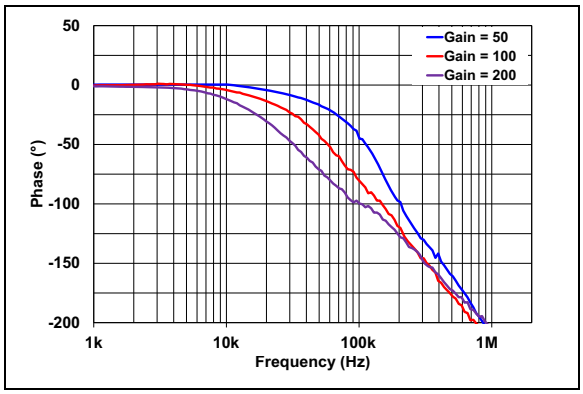


FIGURE 2-29: *Phase vs. Frequency.*

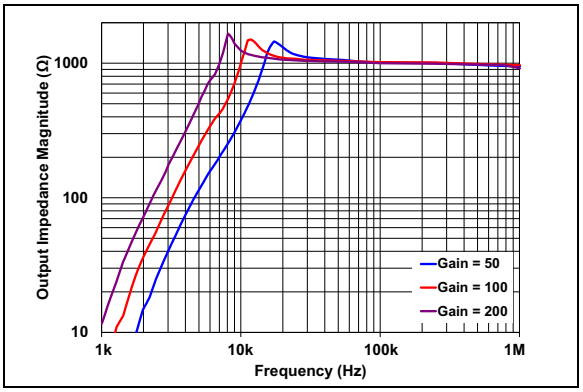


FIGURE 2-32: *Closed-Loop Output Impedance Magnitude vs. Frequency.*

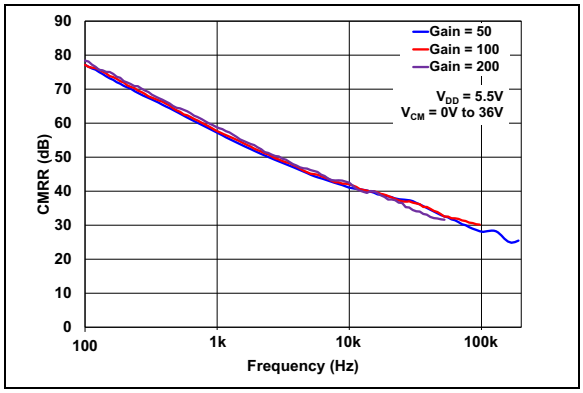


FIGURE 2-30: *CMRR vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.7V to 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF; see Figure 1-5, Figure 1-6 and Figure 1-7.

2.4 Noise and Intermodulation Distortion

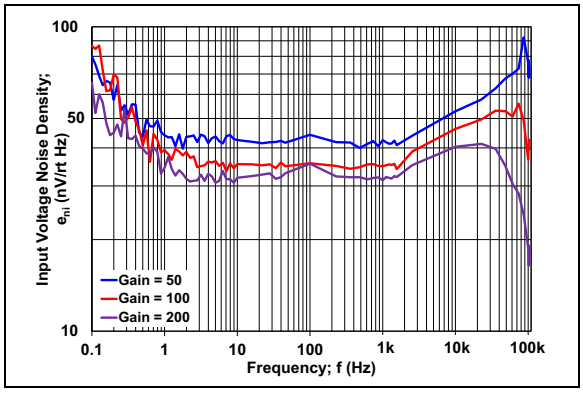


FIGURE 2-33: *Input Noise Voltage Density vs. Frequency.*

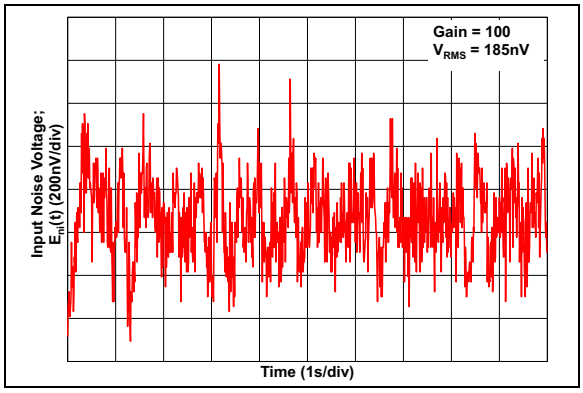


FIGURE 2-36: *Input Noise Voltage vs. Time, G_{DM} = 100.*

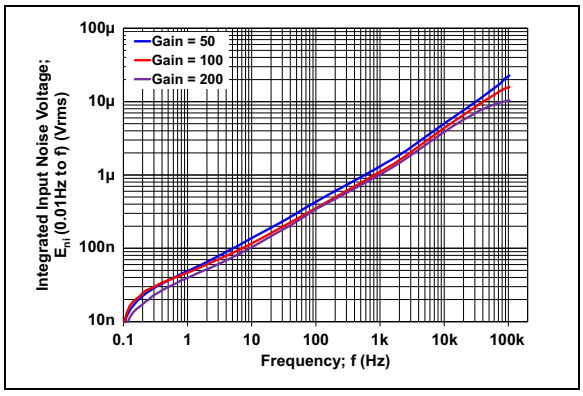


FIGURE 2-34: *Integrated Input Noise.*

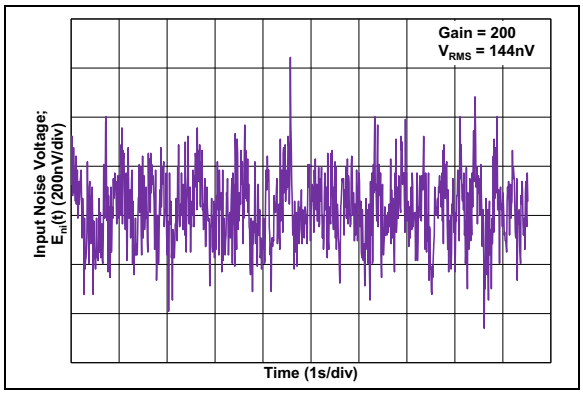


FIGURE 2-37: *Input Noise Voltage vs. Time, G_{DM} = 200.*

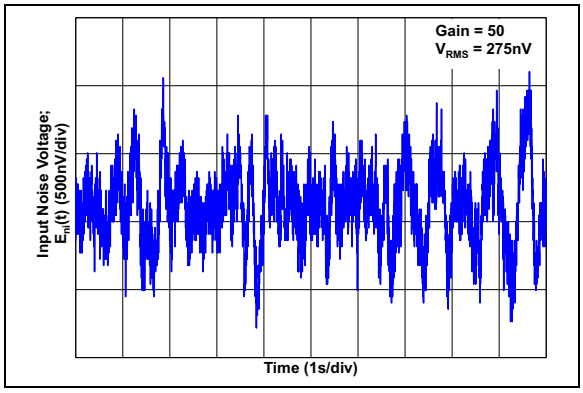


FIGURE 2-35: *Input Noise Voltage vs. Time, G_{DM} = 50.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.7V to 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF; see Figure 1-5, Figure 1-6 and Figure 1-7.

2.5 Time Response

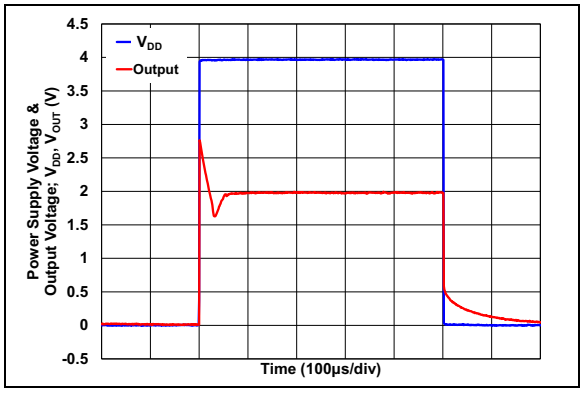


FIGURE 2-38: *Input Offset Voltage vs. Time, at Power-Up.*

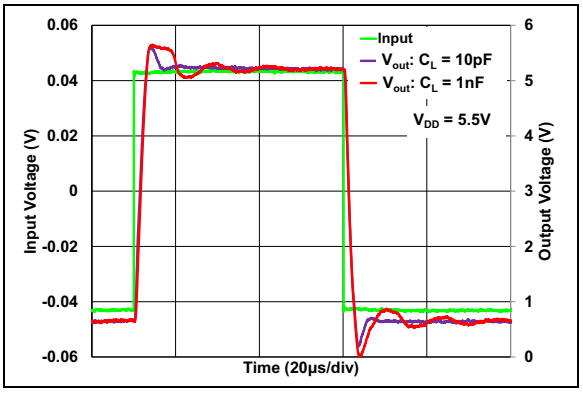


FIGURE 2-41: *Small Signal Step Response to Differential Input Voltage, with Capacitive Load (C_L).*

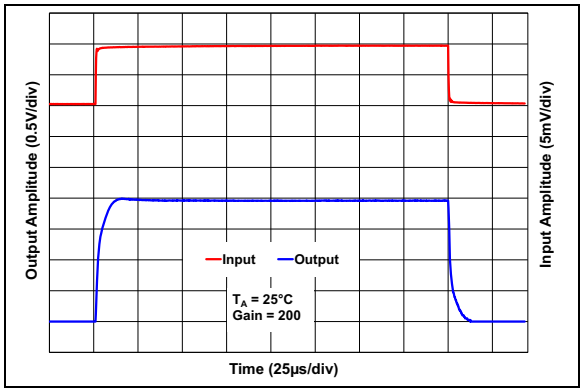


FIGURE 2-39: *Small Signal Step Response to Differential Input Voltage.*

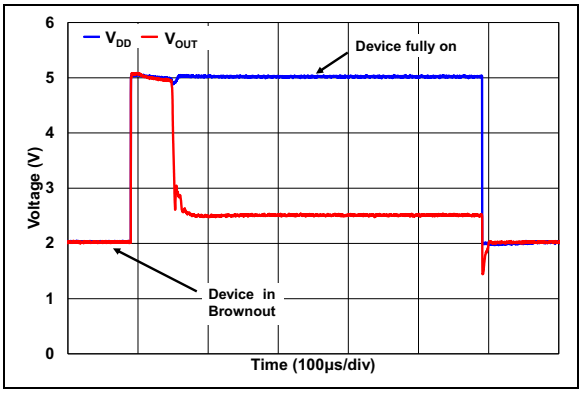


FIGURE 2-42: *Brownout Recovery.*

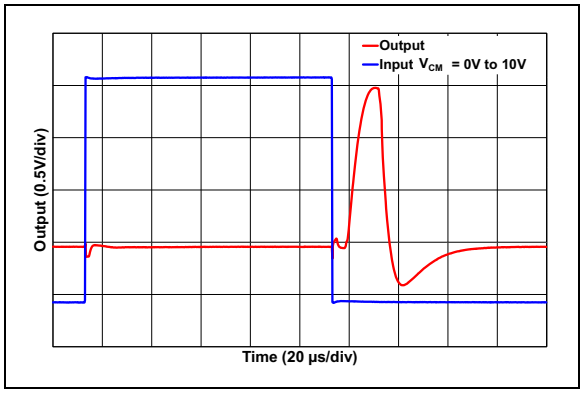


FIGURE 2-40: *Small Signal Step Response to Common-Mode Input Voltage.*

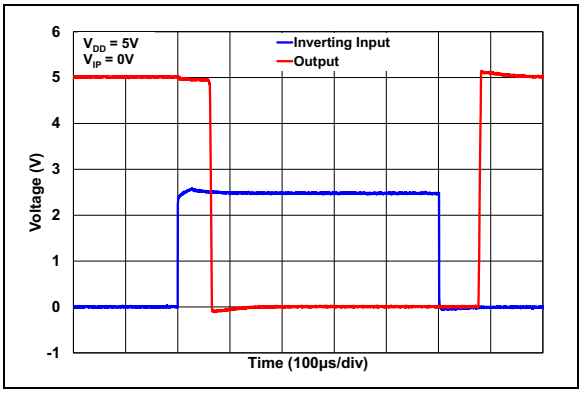


FIGURE 2-43: *Overload Recovery Inverting.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 2.7V to 5.5V, V_{SS} = GND, V_{CM} = 15V, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF; see Figure 1-5, Figure 1-6 and Figure 1-7.

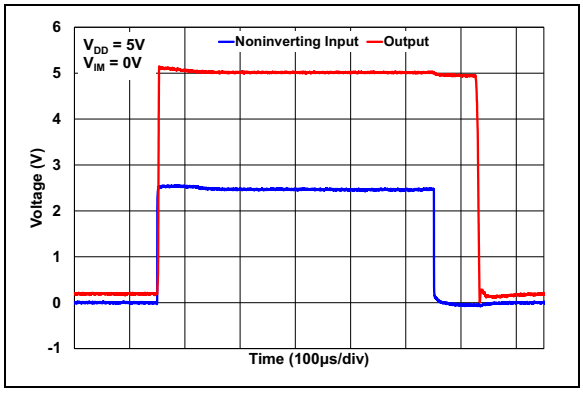


FIGURE 2-44: *Overdrive Recovery Non Inverting.*

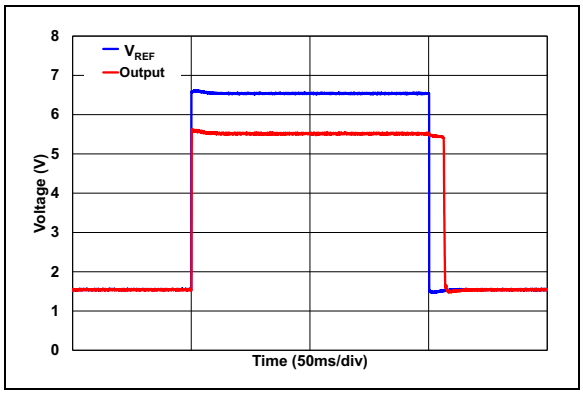


FIGURE 2-45: *Reference Voltage Overdrive.*

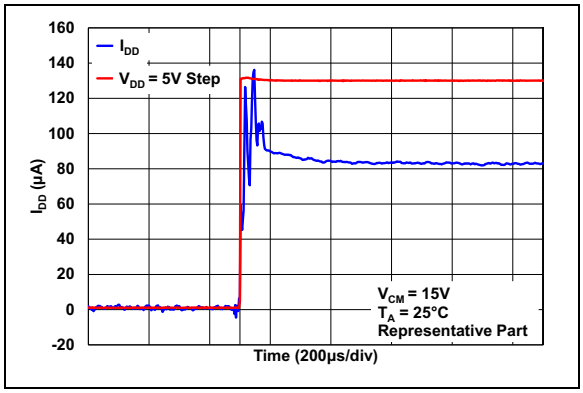


FIGURE 2-46: *Supply Current During Power Up.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6C26 SC-70	Sym.	Description
1	V_{OUT}	Output voltage
2	V_{SS}	Negative power supply
3	V_{IP}	Noninverting input (at load's R_{SH}) and positive (high-side) power supply
4	V_{IM}	Inverting input (at load's R_{SH})
5	V_{REF}	Output reference
6	V_{DD}	Positive (low-side) power supply

3.1 Noninverting and Inverting Analog Signal Input (V_{IP} and V_{IM})

The noninverting and inverting inputs (V_{IP} and V_{IM}) drive a resistor connected to the internal op amp. They are designed to operate over a wide voltage range, with a voltage source to drive it. The difference voltage V_{DM} (or $V_{IP} – V_{IM}$) is the input signal for this amplifier. The common-mode voltage V_{CM} (or $(V_{IP} + V_{IM})/2$) is rejected by this amplifier.

3.2 Analog Output Reference Voltage (V_{REF})

The analog output reference voltage drives a resistor connected to the internal op amp. V_{REF} is set to a DC voltage, which shifts V_{OUT}.

3.3 Analog Output (V_{OUT})

The analog output pin (V_{OUT}) is a low-impedance voltage source.

3.4 Low-Side Power Supplies (V_{DD}, V_{SS})

V_{DD} is normally between V_{SS} + 2.7V and V_{SS} + 5.5V, while the V_{REF} and V_{OUT} pins are usually between V_{SS} and V_{DD}. $V_{DD} – V_{SS}$ triggers the LV POR.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need good bypass capacitors.

In split supply configurations, including dual supplies, ground is between V_{SS} and V_{DD}. Both supply pins will need good bypass capacitors.

In a single (negative) supply configuration, V_{DD} connects to ground and V_{SS} connects to the supply. V_{SS} will need good bypass capacitors.

4.0 DEVICE OPERATION

This chapter includes additional information on basic operations and major functions.

4.1 Basic Performance

4.1.1 IDEAL PERFORMANCE

Figure 4-1 shows the basic circuit; inputs, supplies and output. When the inputs (V_{IP}, V_{IM}, V_{DD}, V_{SS} and V_{REF}) and output (V_{OUT}) are in their specified ranges, and the part is nearly ideal, the output voltage is:

EQUATION 4-1:

$$V_{OUT} \approx V_{REF} + G_{DM}V_{DM}$$

Where:

G_{DM}	=	Differential-Mode Gain
V_{REF}	=	Output Reference Voltage
V_{DM}	=	Differential-Mode Input ($V_{IP} – V_{IM}$)

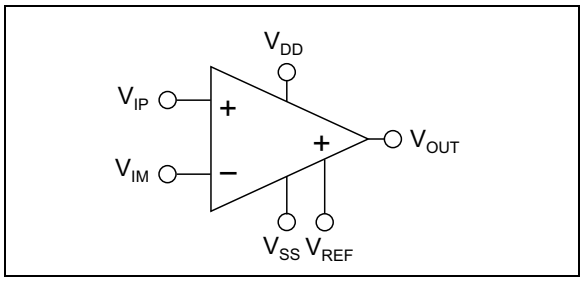


FIGURE 4-1: *Basic Circuit.*

For normal operation, keep:

- V_{CM} between V_{CML} and V_{CMH}
- V_{DM} between V_{DML} and V_{DMH}
- V_{REF} between V_{RL} and V_{RH}
- V_{OUT} between 0.1V to V_{DD} – 0.1V, usually V_{OL} and V_{OH} are hard limits

4.1.2 ANALOG ARCHITECTURE

Figure 4-2 shows the block diagram for these current sense amplifiers.

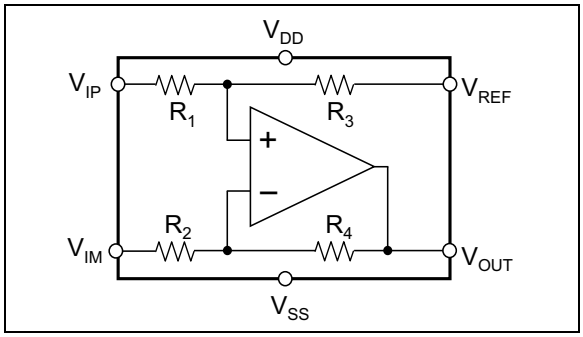


FIGURE 4-2: *MCP6C26 Block Diagram.*

4.1.3 DC PERFORMANCE

4.1.3.1 DC Voltage Errors

Section 1.5, Explanation of DC Error Specifications covers some DC specifications. The input offset error (with temperature coefficients), gain error and nonlinearities are discussed in detail.

4.1.3.2 DC Current Errors

Figure 4-3 shows the resistors and currents that change the DC bias point. The input bias currents (I_{BP}, I_{BM} and I_{BR}), together with a circuit's external input resistances, give an DC error (see Section 1.4.2, DC Differential Gain Test Circuit).

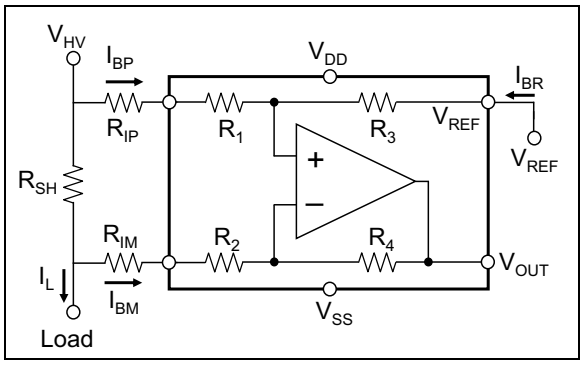


FIGURE 4-3: *DC Bias Resistors and Currents.*

R_{SH} is set by the design requirements, given the load current (I_L). For most applications, R_{SH} would be between 100 µΩ and 1Ω. Keep R_{IP} and R_{IM} below 10Ω to minimize input offset errors.

The DC input offset error due to the input currents is:

$$V_{OS\_IR} = V_{DM} - I_L R_{SH}$$
$$= I_{BM}(R_{SH} + R_{WIM}) - I_{BP}R_{WIP}$$

4.1.4 AC PERFORMANCE

The Gain-Bandwidth Products of these parts (GBWP) is set internally to 9MHz; divide by the gain to obtain the small signal bandwidth (BW). The Bandwidth at the maximum output swing is called the Full Power Bandwidth (FPBW), which is limited either by the BW or by the Slew Rate (SR). To estimate the FPBW for sine waves, use this approximate formula:

$$FPBW \approx \min(BW, SR/(\pi V_{PP})),$$
V_{PP} = the peak-to-peak magnitude of V_{OUT}

These parts are compensated to have a stable response. For instance, step response overshoot is low. (look at small and large signal step response and if the rise times are similar then this description is accurate)

4.1.5 TEMPERATURE PERFORMANCE

The input offset voltage's temperature drift is detailed in Equation 1-5. Other temperature responses are shown in **Section 1.2, Specifications** and **Section 2.0 "Typical Performance Curves"**.

Since there are three power supply pins (V_{IP}, V_{DD} and V_{SS}), and V_{IP} reaches 36V, power and temperature rise calculations are important.

The power dissipated is calculated as follows (I_{OUT} is positive when it flows out of the V_{OUT} pin):

EQUATION 4-2:

$$P_{TOT} = P_{DD} + P_{BM} + P_{BP} + P_{OUT}$$

Where:

R_1 = 20k, 10k, 5k (Note 1)
R_2 = 20k, 10k, 5k (Note 1)
R_3 = 1 MΩ (Note 1)
R_4 = 1 MΩ (Note 1)
I_{OUT} = $(V_{OUT} - V_L)/R_L$
P_{DD} = $(V_{DD} - V_{SS})\ I_{DD}$
P_{BM} = $(V_{IM} - V_{REF})^2/(R_2 + R_4)$
P_{BP} = $(V_{IP} - V_{REF})^2/(R_1 + R_3)$
P_{OUT} = $(V_{DD} - V_{OUT})\ I_{OUT}$, $I_{OUT} \geq 0A$
= $(V_{SS} - V_{OUT})\ I_{OUT}$, $I_{OUT} < 0A$

Note 1: See DC Electrical Characteristics for the respective gains for each resistance. These are typical values only.

Now we can estimate the junction temperature of the device (see Table 1-3):

EQUATION 4-3:

$$T_J = T_A + P_{TOT}\theta_{JA}$$

4.1.6 NOISE PERFORMANCE

This part is designed to have low input noise voltage density at lower frequencies. The offset correction modulates low frequency 1/f noise to higher frequencies.

The measured input noise voltage density is shown in Figure 2-33. Figure 2-34 also shows Integrated Input Noise Voltage (E_{ni}, in units of V_{RMS}) between 0 Hz and f (between 0.1 Hz and 100 kHz).

4.1.7 FINAL TEST VS. BENCH

Final test measurements are not as accurate as bench measurements. For this reason, the input offset voltage related specifications (V_{OS}, TC_1, ..., CMRR and PSRR) are significantly wider than the histograms from bench measurements.

The bench results will give good guidance on how to design your circuit. The specified limits (for final test) give min/max limits used to screen outliers in production.

4.1.8 INTERMODULATION DISTORTION (IMD)

These amplifiers will show intermodulation distortion (IMD) products when an AC signal is present.

The signal and clock can be decomposed into sine wave tones (Fourier series components). These tones interact with the zero-drift circuitry's nonlinear response to produce IMD tones at sum and difference frequencies. Each of the square wave clock's harmonics has a series of IMD tones centered on it. These effects can be minimized by reducing external signals that cause intermodulation.

4.2 Internal Protection

The MCP6C26 helps the designer provide enough protection against undesired conditions and signals in their environment.

4.2.1 INTERNAL PROTECTION DEVICES

All of the ESD structures clamp their inputs when they try to go too far below V_{SS}. Their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow overvoltage events. Very fast ESD events (that meet the specification) are limited so that damage does not occur.

The supply inputs (V_{DD} - V_{SS}) are also connected to PORs, so that internal power up sequencing is well controlled.

The V_{IP} and V_{IM} input pins have an ESD structure (D1, D2, X1, X2) designed to limit V_{IP} - V_{SS}, V_{IM} - V_{SS} and V_{DM}. If either V_{IP} or V_{IM} go too high, they exceed a breakdown voltage and clamp. If either one goes too low (e.g., -5V), the current at the inputs is limited.

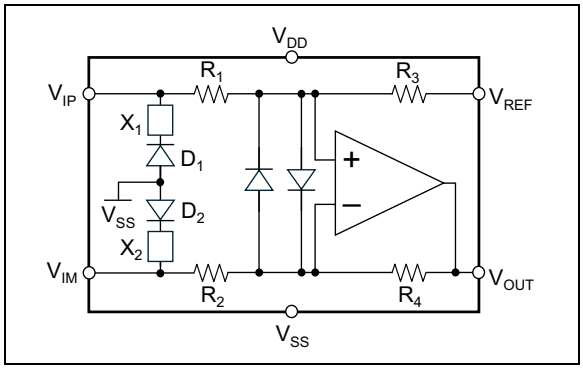


FIGURE 4-4: *Input Protection for V_{IP}, V_{IM} and $V_{DM} = V_{IP} – V_{IM}$.*

The V_{REF}, V_{OUT} and V_{DD} pins have ESD structures that limit their voltages when they try to go too far below V_{SS} (i.e., limit V_{REF} - V_{SS}, V_{OUT} - V_{SS} and V_{DD} - V_{SS}).

4.2.2 PHASE REVERSAL

This part is designed to not exhibit phase inversion when the input signals (V_{CM}, V_{DM} and V_{REF}) exceed their specified ranges.

5.0 APPLICATIONS

This chapter includes design recommendations and typical application circuits.

The Common-mode rejection (see Figure 2-13, Figure 2-14, Figure 2-15 and Figure 2-31) supports high accuracy applications in noisy environments.

The power supply rejection (see Figure 2-32) also has excellent rejection at higher frequencies than traditional.

5.1 Recommended Design Practices

Some simple design practices help take advantage of the MCP6C26's performance in high-side current sensing applications.

5.1.1 SAFETY PRECAUTIONS

Since the MCP6C26 is used in circuits with voltages and currents that can be hazardous to humans, appropriate cautions need to be observed when designing and using said circuits. Please refer to the appropriate industry and government standards and laws to determine design and usage practices.

5.1.2 INPUT VOLTAGE/CURRENT LIMITS

To prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages and currents at and into the V_{IP} and V_{IM} input pins, as well as the differential input voltage V_{DM} (see **Section 1.1, Absolute Maximum Ratings †**). Note that the voltage limits are independent of the current limits and need separate attention to ensure these limits.

The ESD protection on the V_{CM} and V_{DM} inputs was discussed in **Section 4.2.1, Internal Protection Devices**. This structure was chosen to protect the input transistors against many (but not all) overvoltage conditions, and to minimize input bias currents (I_{BP} and I_{BM}).

To protect the inputs, always drive V_{IP} with a low impedance source and use a shunt resistor (R_{SH}) with low resistance (designed to not fail open). Placing zener diode(s) or a transorb across R_{SH} will also help protect the inputs.

5.1.3 BYPASS CAPACITORS

Be sure to specify capacitors that will support your application. Be sure to look at:

- Voltage Rating (well above the maximum value at each pin)
- Dielectrics (good Temp. Cos. and reasonable Volt. Cos.)
- Size
- Surface Mount vs. Leaded
- Cost vs. availability

If possible, connect V_{SS} to ground. This will make your design simpler.

For both positive and negative single power supply configurations, bypass V_{DD} to V_{SS} with a local bypass capacitor next to these pins (e.g., 100 nF). A bulk bypass capacitor should also be added close by (e.g., 2.2 µF); placing it next to the local bypass capacitor is a good choice.

For dual power supply configurations, bypass V_{DD} and V_{SS} to ground separately with a local bypass capacitor next to these pins. A bulk bypass capacitor should also be added close by; placing it next to the local bypass capacitor is a good choice.

5.1.4 PROTECTING THE INPUTS IN HIGH-SIDE CURRENT SENSING APPLICATIONS

Designs using the MCP6C26 will need protection methods in the circuit design. When working on the bench, be careful to use the same protection methods (e.g., do not hot-swap the supply voltages). The following subsections give ideas that may be useful in your design.

5.1.4.1 Protecting V_{DM} (V_{IP} - V_{IM})

The shunt resistor (R_{SH} in Figure 5-1 keeps V_{DM} in range, as long as the load current is not too high. If extra protection is needed in your design, ideas to consider include:

- Limiting V_S's output current
- Setting V_S's output ESR high enough to reduce overshoot
  - The ESR should be a dynamic resistance, not a physical one.

5.1.4.2 Protection for Capacitive Loads

Capacitive loads pass large currents when their voltage changes fast (e.g., at start-up or power down). These currents will cause voltage drops across resistors and (parasitic) inductors in the current path. The voltage drop across inductors can be substantial.

Limiting the current from V_S helps protect the circuit in Figure 5-1. The resistance seen by V_S (R_S (V_S's ESR) and R_{CL} (C_{CL}'s ESR) helps reduce step response overshoot, which provides more protection. Using C_{SH} will create a voltage divider for fast edges; be careful to limit the resulting V_{DM}.

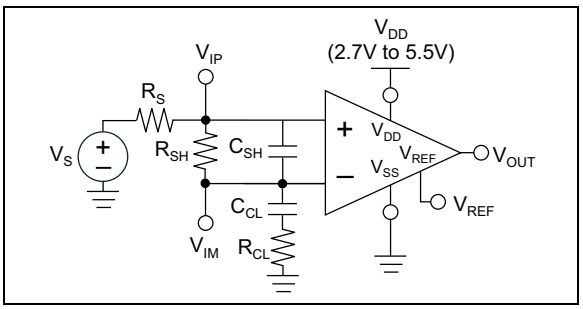


FIGURE 5-1: *Protection for Capacitive Loads.*

5.1.4.3 Protection for Motor Loads

Motor loads are inductive, with resistance and feedback voltage (back EMF) effects. They will generate large voltages when their currents change fast (e.g., at start-up or power down). These voltages will cause currents to flow through resistors, inductors and (parasitic) capacitors in the current path. The currents through capacitors can be substantial.

Limiting the current and/or edge rates from V_S helps protect the circuit in Figure 5-2. The resistance R_S (V_S's ESR) might help in some designs. The catch diode (D_1) keeps the motor voltage from going too far below ground, which protects the inputs.

Overvoltage events at V_S need to be limited. Current from V_S can be limited to one direction with a forward-biased diode between V_S and V_{IP}.

Elements in parallel to the motor can help protect the components. For DC protection, a forward-biased diode and series resistor may help. For AC protection, a capacitor may help. Varistors can help too.

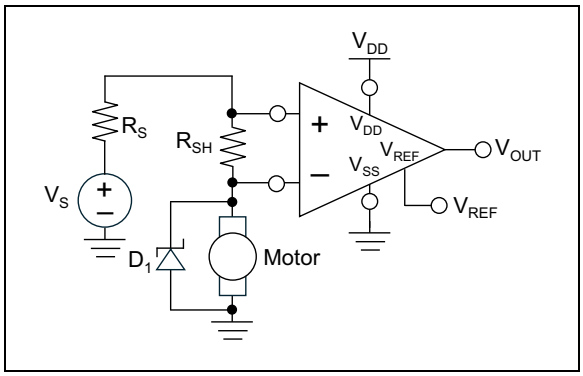


FIGURE 5-2: *Protection for Motor Loads.*

5.1.4.4 Protection From Long Line (Wire) Effects

Long wires between the source (V_S) and MCP6C26 to the load can cause issues in some applications. These issues include capacitive loading and transmission line effects.

The wire capacitance acts in parallel to the load, when the frequency content to the load is relatively slow. If the load is light, this can be a significant effect. The protections for capacitive loads can also be used here.

The wire acts as a transmission line when the frequency content to the load is relatively fast. The highest frequency of interest in a PWM waveform is related to the edges' rise and fall times (t_r) and their equivalent bandwidth (BW). The relative permittivity (ε_r) and relative permeability (μ_r) of the PCB modify the wavelength (λ). The wavelength is then estimated as:

EQUATION 5-1:

$$BW \approx \frac{0.35}{t_r}$$

$$\lambda = \frac{\varepsilon_r \mu_r (3 \times 10^8 M/s)}{BW}$$

The wire's length should be less than $\lambda/10$. When that is not the case, there are several possible remedies, such as:

- Placing a filter at the load to limit BW (increase t_r)
- Placing a series R-C snubber in parallel with the load
- Limiting rise and fall times at the source (V_S).

5.1.5 SETTING THE VOLTAGE AT V_{REF}

Ensure that Load supply, V_{DD}, V_{SS} and V_{REF} remain within specified limits.

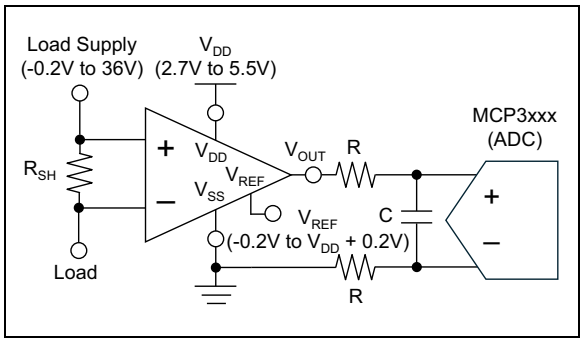


FIGURE 5-3: *V_{REF} Bypass Circuit #1.*

Figure 5-3 uses an IC V_{REF} to generate V_{REF} - V_{SS}, an R-C low pass filter to reject fast glitches seen at V_{REF} - V_{SS} and an op amp buffer (≥ 1 MHz) to drive V_{REF} with a low impedance source (notice only one connection to V_{SS} is shown, for good precision).

5.1.6 INPUT FILTERING

Figure 5-4 depicts input filter connections. The series input resistors should not exceed 10Ω, and companion capacitor values determined accordingly. Input filtering may be required for any or all of these reasons:

1. An inherently noisy current signal,
2. The effects of shunt inductance,
3. To avoid aliasing in the chopper stabilized amplifier if there is considerable signal content near the zero-drift switching frequency of 200 kHz, or
4. To reduce effects of fast transients.

It is also possible to filter noise at the output of the MCP6C26 (assuming the amplitude of the noise is low enough to not cause overloading within the MCP6C26).

The inductance of low value shunts causes a rise in high frequency response at surprisingly low frequencies (e.g. 10 kHz to 20 kHz) accentuating high-frequency components including fast transients. In some cases this high frequency content can aggravate aliasing in the output voltage.

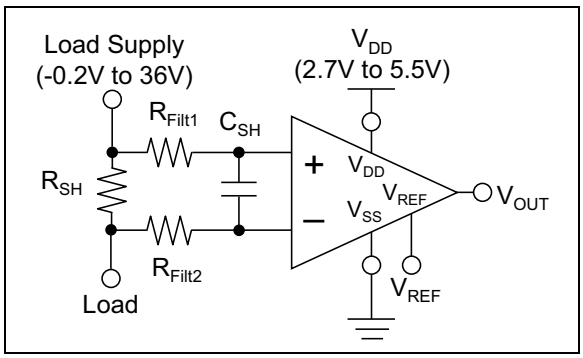


FIGURE 5-4: *Input Filtering.*

5.1.7 TEMPERATURE RISE

Make sure that T_J does not exceed the Absolute Maximum Junction Temperature spec (see **Section 1.1, Absolute Maximum Ratings †**). This is a strong concern when T_A is high (e.g., at +125°C) and when I_{OUT}'s magnitude is large (e.g., near the short circuit limit) or when V_{IP} is high.

Formulas needed for this part of the design are found in **Section 4.1.5, Temperature Performance**.

5.1.8 ENSURING STABILITY

A few simple design techniques will help take advantage of these stable parts. Simulations and bench measurements help to verify the solutions (e.g., look at step response overshoot and ringing).

5.1.8.1 Driving V_{REF}

The voltage source driving the V_{REF} pin must be low impedance (see Section 5.1.6, Input Filtering), throughout the MCP6C26's bandwidth, so that the signal gain is constant within the signal bandwidth.

5.1.8.2 Source Impedances

The recommended DC source resistances (at V_{IP}, V_{IM} and V_{REF}; see Section 5.1.6, Input Filtering) will help ensure stability, by keeping R-C time constants very fast.

5.1.8.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage amplifiers. As the load capacitance increases, the feedback loop's phase margin decreases. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. Sensitivity to capacitive loads also changes with gain (G_{DM}).

When driving large capacitive loads with these parts, a small series resistor at the output (R_{ISO} in Figure 5-5) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

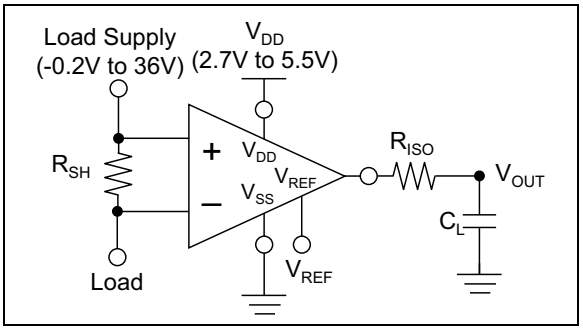


FIGURE 5-5: *Include R_{ISO} with Capacitive Loads to Improve Phase Margin.*

Figure 5-6 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized (by $50/G_{DM}$) load capacitance (C_L).

After selecting R_{ISO} for the circuit, double check the resulting frequency response peaking and step response overshoot on the bench. Modify R_{ISO}'s value until the response is reasonable.

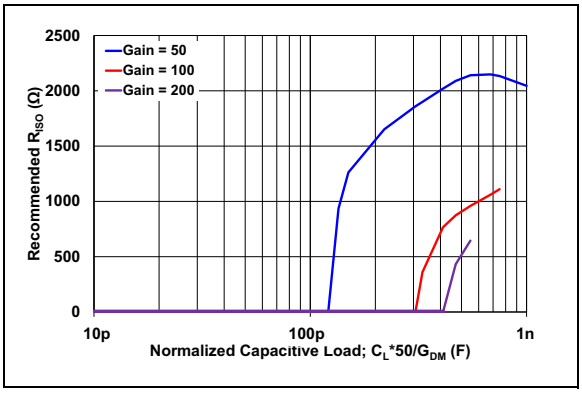


FIGURE 5-6: *Recommended R_{ISO} vs. Capacitive Load.*

5.1.9 UNIDIRECTIONAL APPLICATIONS

In unidirectional applications where $V_{REF} = V_{SS}$, it is important to minimize output headroom (V_{OL}). The lower V_{OL} is, the more accurate the zero scale reading is. This is done by making R_L high and by tying V_L to V_{SS}.

In unidirectional applications where $V_{REF} = V_{DD}$, it is important to minimize output headroom ($V_{DD} - V_{OH}$). The higher V_{OH} is, the more accurate the zero scale reading is. This is done by making R_L high and by tying V_L to V_{DD}.

Figure 5-3 shows how to connect V_{REF} and V_{SS} for best performance.

5.1.10 BIDIRECTIONAL APPLICATIONS

To maximize headroom, reduce V_{OL} and V_{OH} by setting R_L high and by setting V_L to mid-supply.

5.1.11 SUPPLY PINS

See Section 3.4, Low-Side Power Supplies (VDD, VSS) for common power supply pin design approaches.

Setting V_{SS} = GND has the potential to increase rejection of crosstalk and glitches. In any case, a good ground design (e.g., ground plane on a PCB) and appropriate bypass capacitors are needed to realize these benefits. It pays to be sure that your capacitor's voltage rating and dielectric will support your needs over your voltage and temperature ranges. With some dielectrics, it pays to also take aging (changes over time) into account too.

5.1.12 PCB TIPS

These amplifiers are specified up to 36V at the V_{IP} pin and the load currents can be high. For these reasons, the PCB design needs to be done with care.

Industry standards, such as IPC-2221A, give requirements for many PCB related topics. These topics include current capacity of traces, spacing between conductors, altitude effects, coatings and parasitic impedances.

A package's pin spacing, together with other design choices, affects the maximum voltage allowed between adjacent pins.

5.1.13 OTHER APPLICATIONS

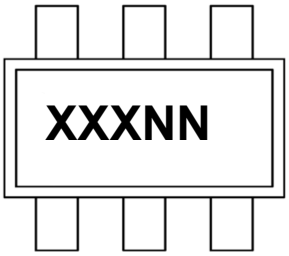
Other applications not related to high-side current sensing that the MCP6C26 can be used for are:

- Low-side current sensing
- Differential sensor conditioning.

6.0 PACKAGING INFORMATION

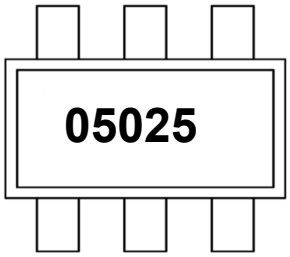
6.1 Package Marking Information

6-Lead SC70



Part Number	Code
MCP6C26T-050E/LTY	050NN
MCP6C26T-100E/LTY	100NN
MCP6C26T-200E/LTY	200NN

Example

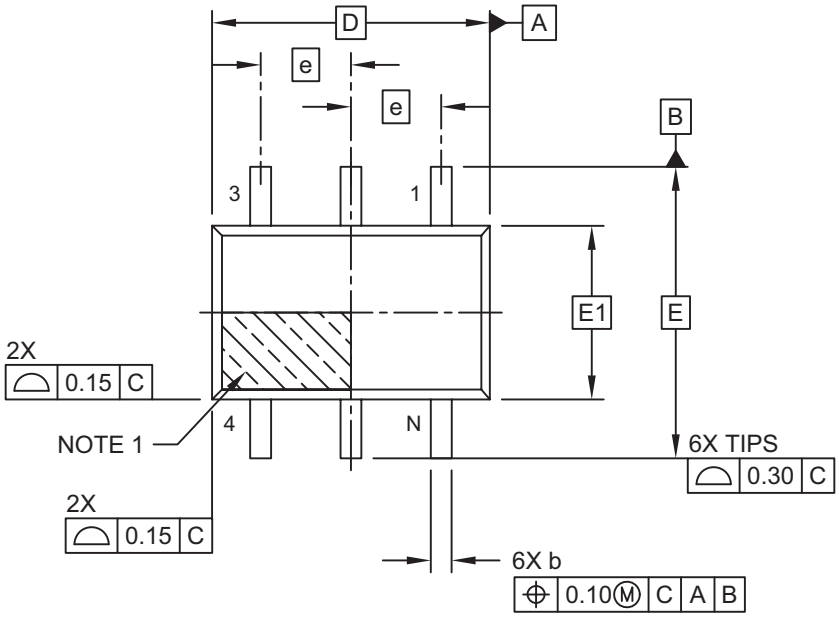


Legend:	XX...X	Device-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

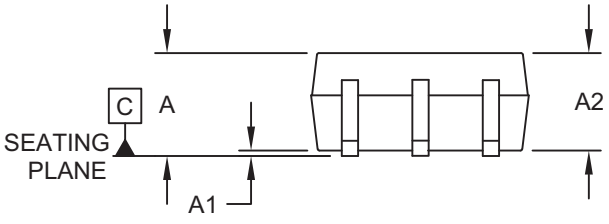
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6-Lead Plastic Small Outline Transistor (D4A) - 2.0x1.25mm Body [SC70]

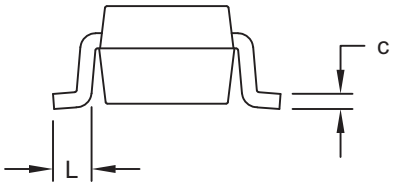
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

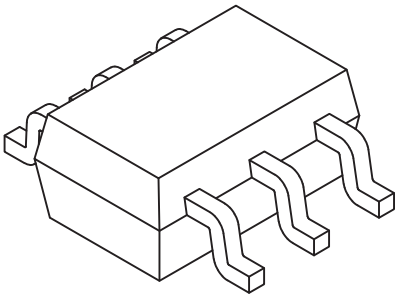


END VIEW

Microchip Technology Drawing C04-1133C Sheet 1 of 2

6-Lead Plastic Small Outline Transistor (D4A) - 2.0x1.25mm Body [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	0.90	1.00
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	2.50	2.60	2.70
Overall Width	E		2.10 BSC	
Exposed Pad Width	E1		1.25 BSC	
Terminal Width	b	0.15	-	0.30
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.22

Notes:

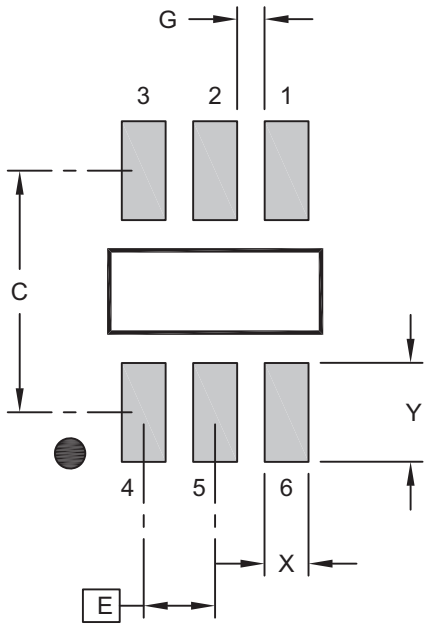
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1133C Sheet 2 of 2

6-Lead Plastic Small Outline Transistor (D4A) - 2.0x1.25mm Body [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		1.90	
Contact Pad Width (X6)	X			0.42
Contact Pad Length (X6)	Y			0.77
Distance Between Pads	G	0.23		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3133C

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2024)

- Initial release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-XXX	X	/XXX
Device	Tape and Reel Option	Gain Option	Temperature Range	Package

Device:	MCP6C26:	36V High and Low-Side Current Sense Difference Amplifier
Tape and Reel Option:	T	= Tape and Reel(1)
Gain Option:	050 100 200	= Differential Gain of 50 V/V = Differential Gain of 100 V/V = Differential Gain of 200 V/V
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	LTY	= Plastic Small Outline Transistor (SC-70), 6-Lead Nickel-Palladium-Gold Leadframe

Examples:

a) MCP6C26T-050E/LTY: Tape and Reel, Differential Gain = 50, Extended Temperature, 6LD SC70

b) MCP6C26T-100E/LTY: Tape and Reel, Differential Gain = 100, Extended Temperature, 6LD SC70

c) MCP6C26T-200E/LTY: Tape and Reel, Differential Gain = 200, Extended Temperature, 6LD SC70

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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