



WM02DN110C

Dual N-Channel Enhancement Mode MOSFET

Description

WM02DN110C uses advanced power trench technology that has been especially tailored to minimize the on-state resistance. This device is suitable for un-directional or bidirectional load switch, facilitated by its common-drain configuration.

$V_{(BR)DSS}(V)$	$I_D(A)$	$R_{DS(on)TYP}(m\Omega)$
20	11	6.0 @ $V_{GS}=4.5V$
		6.2 @ $V_{GS}=4.0V$
		6.5 @ $V_{GS}=3.7V$
		7.0 @ $V_{GS}=3.1V$
		8.2 @ $V_{GS}=2.5V$

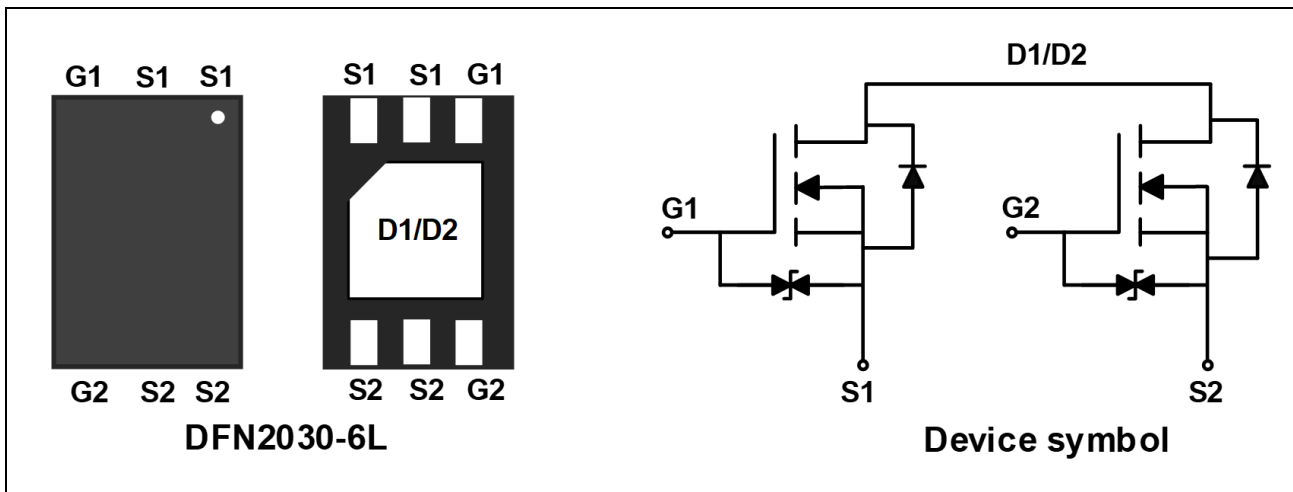
Features

- Super high dense cell for low $R_{DS(on)}$
- RoHS Compliant and Halogen-Free
- ESD protected: Class 2

Applications

- Battery protection
- Load switch

Schematic & PIN Configuration



Absolute Maximum Rating

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current	$T_A=25^\circ C$	I_D	11	A
	$T_A=70^\circ C$		8.8	A
Pulsed Drain Current ¹		I_{DM}	70	A
Single Pulse Avalanche Energy ⁵		E_{AS}	39	mJ
Avalanche Current		I_{AS}	28	A
Total Power Dissipation	$T_A=25^\circ C$	P_D	1.56	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ C$
Maximum Junction-to-Ambient ²		$R_{\theta JA}$	80	$^\circ C/W$

Electrical Characteristics ($T_{amb}=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	20	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20V, V _{GS} = 0V			1	μA
Gate-body Leakage current	I _{GSS}	V _{DS} = 0V, V _{GS} = ±8V	-	-	±10	μA
Gate-Threshold Voltage ³	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	0.45	-	1.5	V
Drain-Source on-Resistance ³	R _{DS(on)}	V _{GS} = 4.5V, I _D = 5.5A	4.5	6.0	7.5	mΩ
		V _{GS} = 4.0V, I _D = 5.5A	4.8	6.2	7.8	
		V _{GS} = 3.7V, I _D = 5.5A	5.0	6.5	8.5	
		V _{GS} = 3.1V, I _D = 5.5A	5.3	7.0	9.3	
		V _{GS} = 2.5 V, I _D = 5.5A	6	8.2	10.5	
Forward Transconductance ³	g _{fs}	V _{DS} = 5V, I _D = 5.5A	-	45	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} = 10V, V _{GS} =0V, f =1MHz	-	1767	-	pF
Output Capacitance	C _{oss}		-	184	-	
Reverse Transfer Capacitance	C _{rss}		-	155	-	
Switching Characteristics						
Total Gate Charge ⁴	Q _g	V _{GS} =4.5V, V _{DS} = 16V, I _D = 10A	-	23	-	nC
Gate-Source Charge ⁴	Q _{gs}		-	3.5	-	
Gate-Drain Charge ⁴	Q _{gd}		-	8.4	-	
Turn-on Delay Time ⁴	t _{d(on)}	V _{GS} =4.5V, V _{DD} = 16V, R _G = 6Ω, I _D = 5.5A	-	10.2	-	nS
Rise Time ⁴	t _r		-	41	-	
Turn-off Delay Time ⁴	t _{d(off)}		-	67	-	
Fall Time ⁴	t _f		-	31	-	
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	I _S = 1A, V _{GS} = 0V	-	-	1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface mounted on FR4 board using 1 square inch pad size, 1oz single-side copper.
3. Pulse Test: Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
4. Guaranteed by design, not subject to product
5. The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=28A$.

Typical Characteristics

Figure 1. Output Characteristics

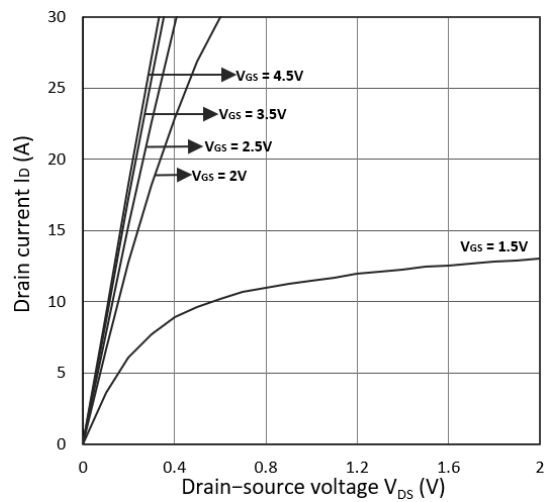


Figure 2. Transfer Characteristics

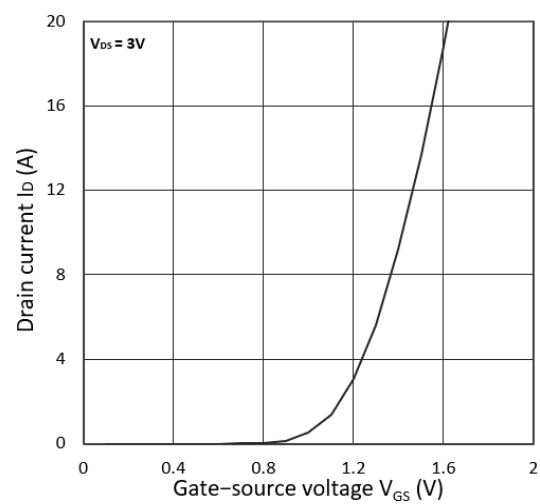
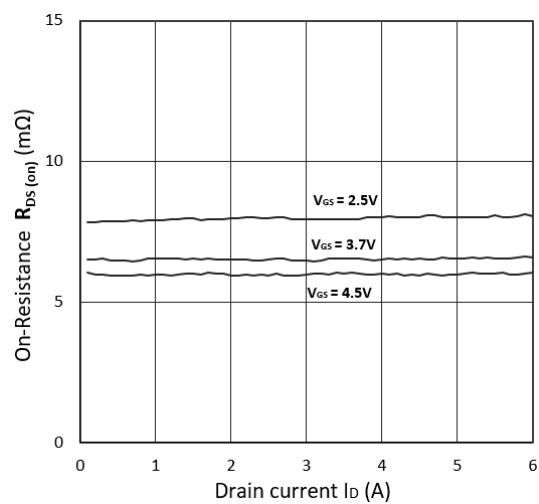
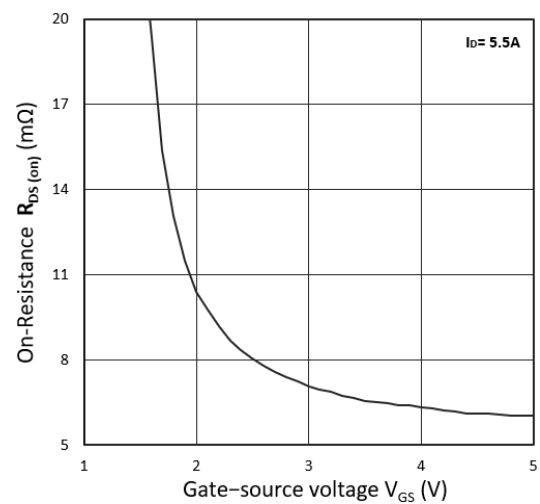
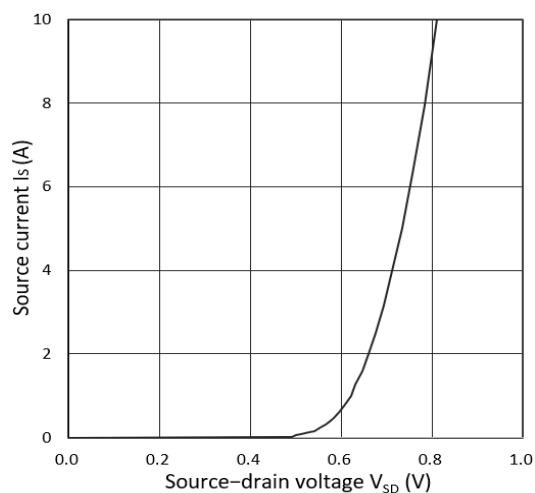
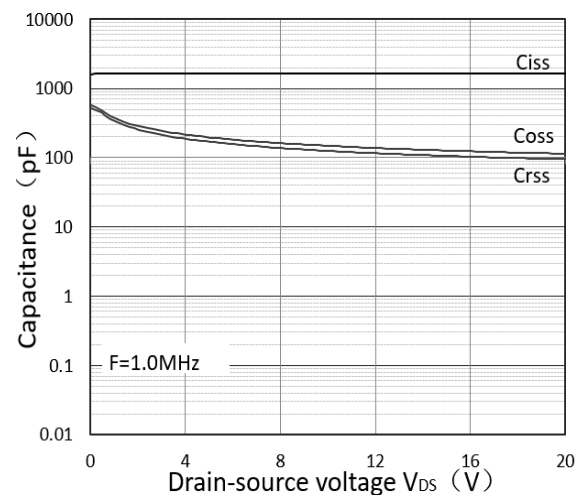
Figure 3. $R_{DS(ON)}$ vs. I_D Figure 4. $R_{DS(ON)}$ vs. V_{GS} Figure 5. I_S vs. V_{SD} 

Figure 6. Capacitance Characteristics



Outline Drawing –DFN2030-6L

PACKAGE OUTLINE

Diagram showing the top view of the package. It is a square with side length D. The width is labeled W. A dashed circle in the bottom-left corner is labeled "OPTION PIN MARKING".

TOP VIEW

Diagram showing the bottom view of the package. It features six rectangular pads arranged in two rows of three. The pitch between pads is e. The width of the pad array is D1. The length of the package is L. The distance from the top edge to the top of the pads is k. The width of the pads is b. A dashed circle with a diagonal line is labeled "OPTION". The label "N1" is located near the bottom pads.

BOTTOM VIEW

Diagram showing the side view of the package. The height of the package is A. The height of the top layer is A1. The height of the bottom layer is A2.

SIDE VIEW

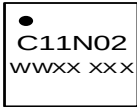
DFN2030-6L package symbol, showing a square package with six pins.

DFN2030-6L

DIMENSIONS

SYMBOL	MILLIMETER		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A2	0.203		0.008	
D	1.95	2.05	0.077	0.081
E	2.95	3.05	0.116	0.120
k	1.65	1.75	0.057	0.061
D1	1.45	1.55	0.065	0.069
b	0.20	0.30	0.008	0.012
e	0.50 BSC		0.020BSC	
L	0.30	0.40	0.012	0.016

Marking Codes

Part Number	WM02DN110C	
Marking Code		C11N02 = Device Code WWXX XXX= Date Code

Package Information

Qty: 3k/Reel

CONTACT INFORMATION

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For additional information, please contact your local Sales Representative.

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Specifications are subject to change without notice.
 The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.
 Users should verify actual device performance in their specific applications.