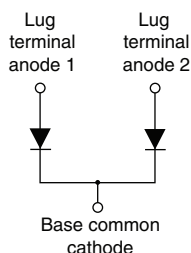


High Performance Schottky Rectifier, 200 A


TO-244


FEATURES

- 175 °C T_J operation
- Center tap module
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- UL approved file E222165 
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	200 A
V_R	100 V
Package	TO-244
Circuit configuration	Two diodes common cathode

DESCRIPTION / APPLICATIONS

The VS-203CNQ.. center tap Schottky rectifier module series has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature. Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	200	A
V_{RRM}		100	V
I_{FSM}	$t_p = 5 \mu s$ sine	12 800	A
V_F	100 A _{pk} , $T_J = 125^\circ C$ (per leg)	0.70	V
T_J	Range	-55 to +175	°C

VOLTAGE RATINGS			
PARAMETER	SYMBOL	VS-203CNQ100PbF	UNITS
Maximum DC reverse voltage	V_R	100	V
Maximum working peak reverse voltage	V_{RWM}		

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current See fig. 5	$I_{F(AV)}$	50 % duty cycle at $T_C = 142^\circ C$, rectangular waveform	100	A
per leg			200	
Maximum peak one cycle non-repetitive surge current per leg See fig. 7	I_{FSM}	5 μs sine or 3 μs rect. pulse	12 800	A
		10 ms sine or 6 ms rect. pulse	1700	
Non-repetitive avalanche energy per leg	E_{AS}	$T_J = 25^\circ C$, $I_{AS} = 13 A$, $L = 0.2 mH$	15	mJ
Repetitive avalanche current per leg	I_{AR}	Current decaying linearly to zero in 1 μs Frequency limited by T_J maximum $V_A = 1.5 \times V_R$ typical	1	A

**ELECTRICAL SPECIFICATIONS**

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS	
Maximum forward voltage drop per leg See fig. 1	$V_{FM}^{(1)}$	100 A	$T_J = 25\text{ }^{\circ}\text{C}$	0.86	V	
		200 A		1.03		
		100 A	$T_J = 125\text{ }^{\circ}\text{C}$	0.70		
		200 A		0.84		
Maximum reverse leakage current per leg See fig. 2	$I_{RM}^{(1)}$	$T_J = 25\text{ }^{\circ}\text{C}$	$V_R = \text{Rated } V_R$	3	mA	
		$T_J = 125\text{ }^{\circ}\text{C}$		40		
Threshold voltage	$V_{F(TO)}$	$T_J = T_J \text{ maximum}$		0.50	V	
Forward slope resistance	r_t			1.08	mΩ	
Maximum junction capacitance per leg	C_T	$V_R = 5\text{ }V_{DC}$ (test signal range 100 kHz to 1 MHz) $25\text{ }^{\circ}\text{C}$		2650	pF	
Typical series inductance per leg	L_S	From top of terminal hole to mounting plane		7.0	nH	
Maximum voltage rate of change	dV/dt	Rated V_R		10 000	V/μs	

Note(1) Pulse width < 300 μ s, duty cycle < 2 %**THERMAL - MECHANICAL SPECIFICATIONS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}	-55	-	175	$^{\circ}\text{C}$
Thermal resistance, junction to case per leg per module	R_{thJC}	-	-	0.38	$^{\circ}\text{C/W}$
		-	-	0.19	
Thermal resistance, case to heatsink	R_{thCS}	-	0.10	-	
Weight		-	68	-	g
			2.4		oz.
Mounting torque		35.4 (4)	-	53.1 (6)	lbf · in (N · m)
Mounting torque center hole		30 (3.4)	-	40 (4.6)	
Terminal torque		30 (3.4)	-	44.2 (5)	
Vertical pull		-	-	80	lbf · in
2" lever pull		-	-	35	

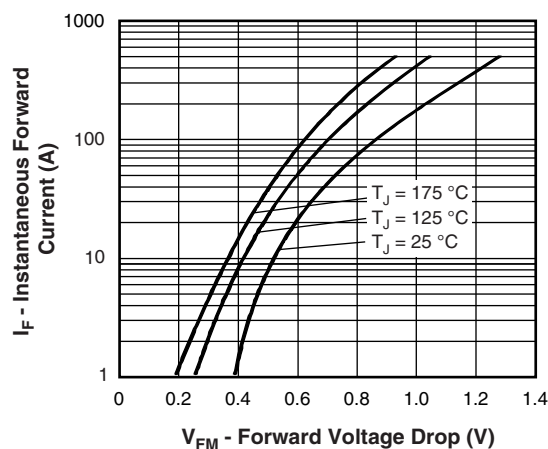


Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

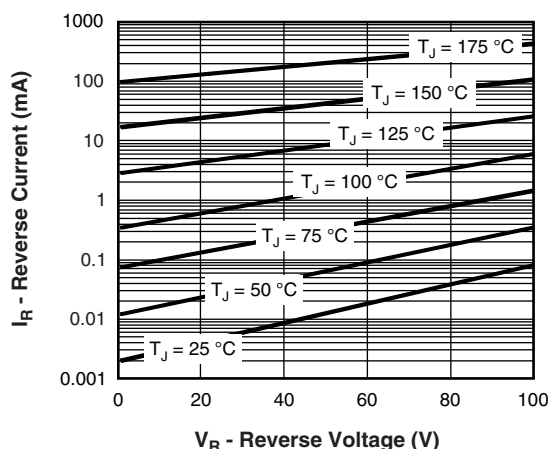


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

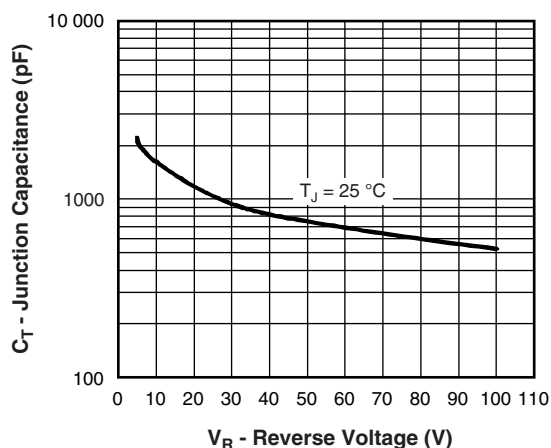


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

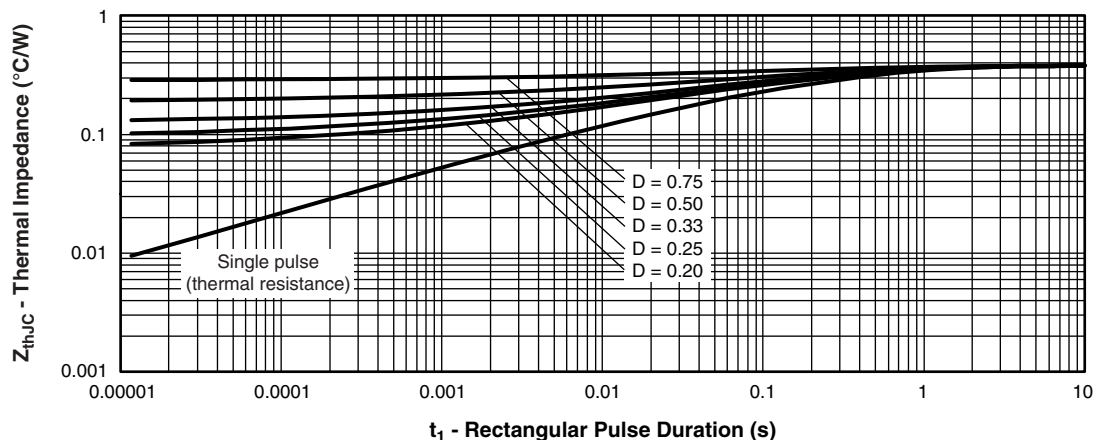
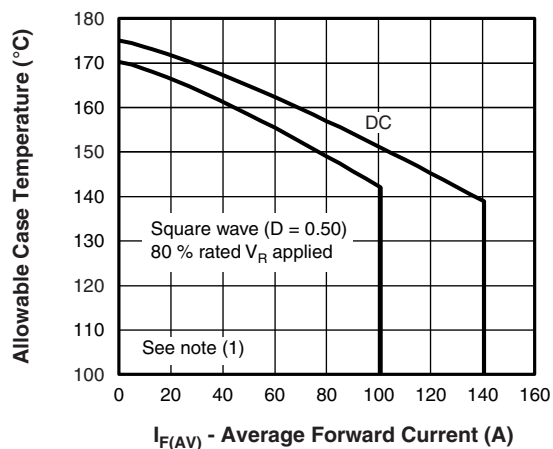

Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics (Per Leg)


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

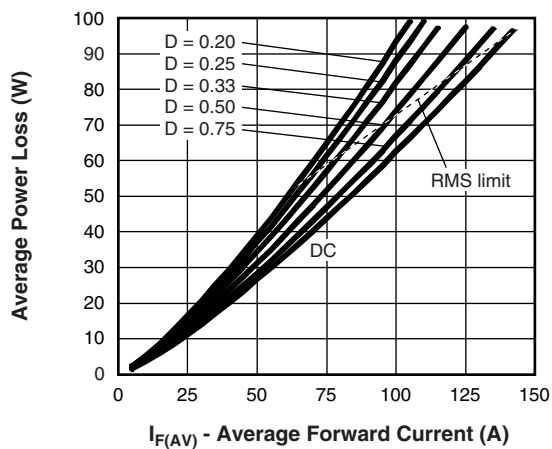


Fig. 6 - Forward Power Loss Characteristics (Per Leg)

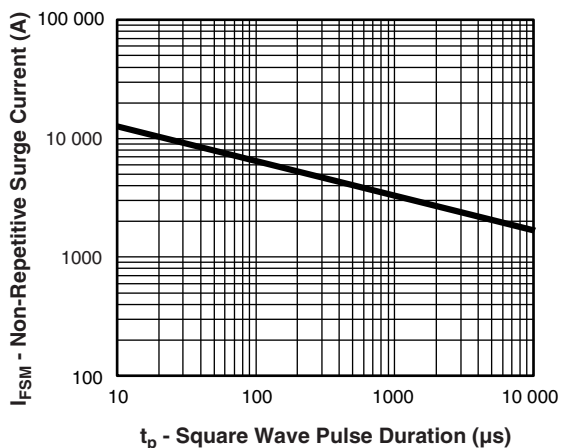


Fig. 7 - Maximum Non-Repetitive Surge Current (Per Leg)

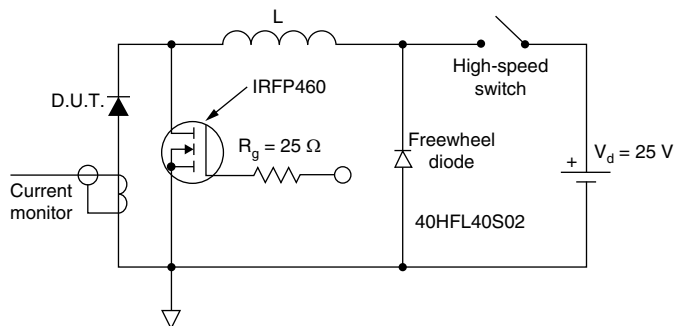


Fig. 8 - Unclamped Inductive Test Circuit

Note

- (1) Formula used: $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$;
 P_d = forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6);
 P_{dREV} = inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at $V_{R1} = 80\%$ rated V_R

ORDERING INFORMATION TABLE

Device code	VS-	20	3	C	N	Q	100	PbF
	1	2	3	4	5	6	7	8
1	Vishay Semiconductors product							
2	Average current rating (x 10)							
3	Product silicon identification							
4	C = circuit configuration							
5	N = not isolated							
6	Q = Schottky rectifier diode							
7	Voltage rating (100 = 100 V)							
8	Lead (Pb)-free							

LINKS TO RELATED DOCUMENTS

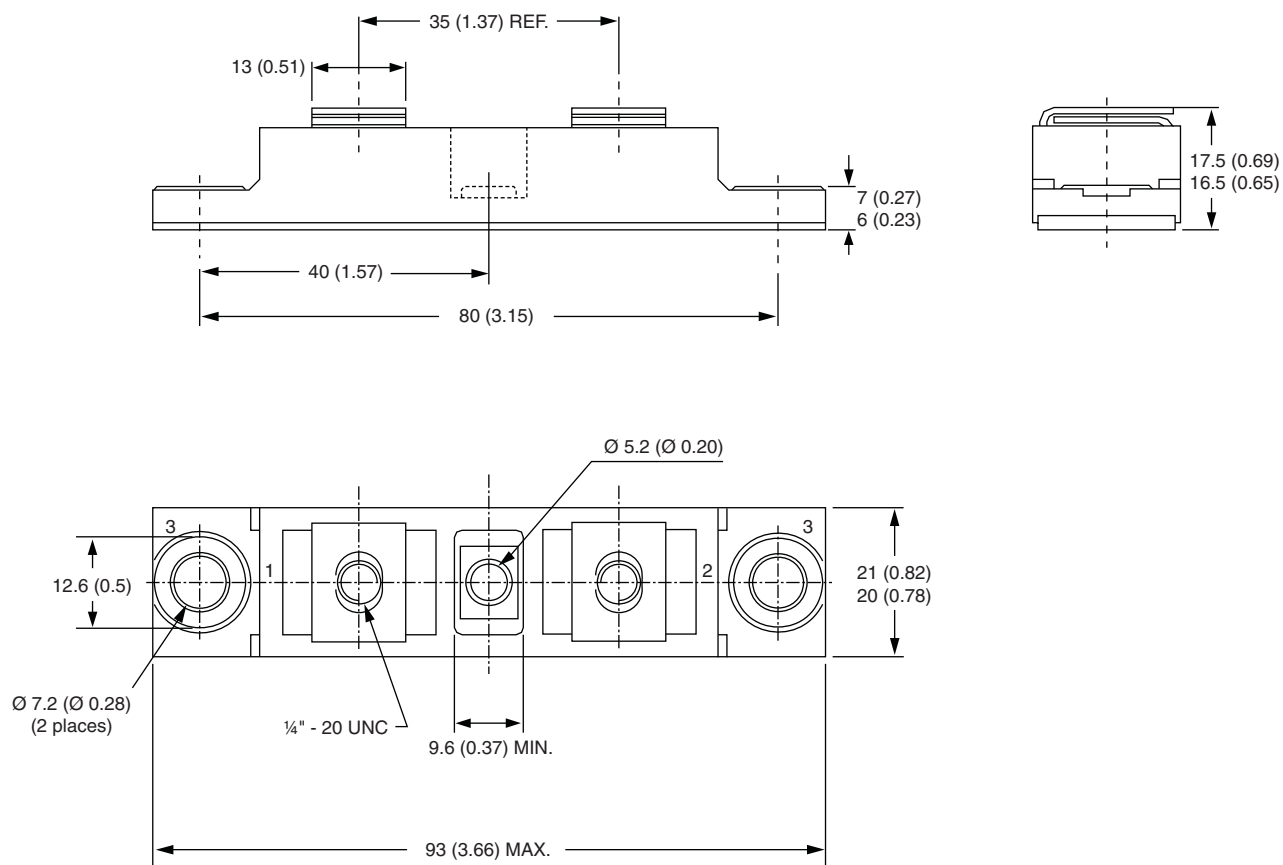
Dimensions

www.vishay.com/doc?95021



TO-244

DIMENSIONS in millimeters (inches)





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