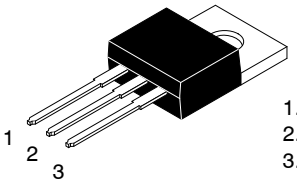
PNP Epitaxial Silicon Transistor

KSA1010



1. Base
2. Collector
3. Emitter

TO−220−3LD
CASE 340AT

High Speed High Voltage Switching

- Industrial Use
- Complement to KSC2334

ABSOLUTE MAXIMUM RATINGS

(T_C = 25°C unless otherwise noted.)

Symbol	Parameter	Ratings	Unit
V_{CBO}	Collector−Base Voltage	−100	V
V_{CEO}	Collector−Emitter Voltage	−100	V
V_{EBO}	Emitter−Base Voltage	−7	V
I_C	Collector Current (DC)	−7	A
I_{CP}	Collector Current (Pulse) (Note 1)	−15	A
I_B	Base Current	−3.5	A
P_C	Collector Dissipation (T_C = 25°C)	40	W
	Collector Dissipation (T_A = 25°C)	1.5	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. PW ≤ 300 μs, Duty Cycle ≤ 10%.

MARKING DIAGRAM

YWW = Date Code (Year & Week)
ZZ = Lot Run Traceability Code
A1010 = Specific Device Code
Y = h_{FE} Grade

ORDERING INFORMATION

Device	Package	Shipping
KSA1010YTU	TO−220−3LD (Pb−Free)	1000 Units / Tube

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CEO}(sus)	Collector−Emitter Sustaining Voltage	I_C = −5 A, I_{B1} = −0.5 A, L = 1 mH	−100	−	V
V_{CEX}(sus)1	Collector−Emitter Sustaining Voltage	I_C = −5 A, I_{B1} = $-I_{B2}$ = −0.5 A, V_{BE}(off) = 5 V, L = 180 μH, Clamped	−100	−	V
V_{CEX}(sus)2	Collector−Emitter Sustaining Voltage	I_C = −10 A, I_{B1} = −1 A, I_{B2} = 0.5 A, V_{BE}(off) = 5 V, L = 180 μH, Clamped	−100	−	V
I_{CBO}	Collector Cut−off Current	V_{CB} = −100 V, I_E = 0	−	−10	μA
I_{CER}	Collector Cut−off Current	V_{CE} = −100 V, R_{BE} = 51 Ω, T_C = 125°C	−	−1	mA
I_{CEX1}	Collector Cut−off Current	V_{CE} = −100 V, V_{BE}(off) = 1.5 V	−	−10	μA
I_{CEX2}	Collector Cut−off Current	V_{CE} = −100 V, V_{BE}(off) = 1.5 V, T_C = 125°C	−	−1	mA
I_{EBO}	Emitter Cut−off Current	V_{EB} = −5 V, I_C = 0	−	−10	μA
h_{FE1} h_{FE2} h_{FE3}	DC Current Gain (Note 2)	V_{CE} = −5 V, I_C = −0.5 A V_{CE} = −5 V, I_C = −3 A V_{CE} = −5 V, I_C = −5 A	40 40 20	− 200 −	
V_{CE}(sat)	Collector−Emitter Saturation Voltage (Note 2)	I_C = −5 A, I_B = −0.5 A	−	−0.6	V
V_{BE}(sat)	Base−Emitter Saturation Voltage (Note 2)	I_C = −5 A, I_B = −0.5 A	−	−1.5	V
t_{ON}	Turn On Time	V_{CC} = −50 V, I_C = −5 A, I_{B1} = $-I_{B2}$ = −0.5 A, R_L = 10 Ω	−	0.5	μs
t_{STG}	Storage Time		−	1.5	μs
t_F	Fall Time		−	0.5	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: PW ≤ 350 μs, Duty Cycle ≤ 2%.

h_{FE} Classification

Classification	R	O	Y
h_{FE2}	40 ~ 80	60 ~ 120	100 ~ 200

TYPICAL CHARACTERISTICS

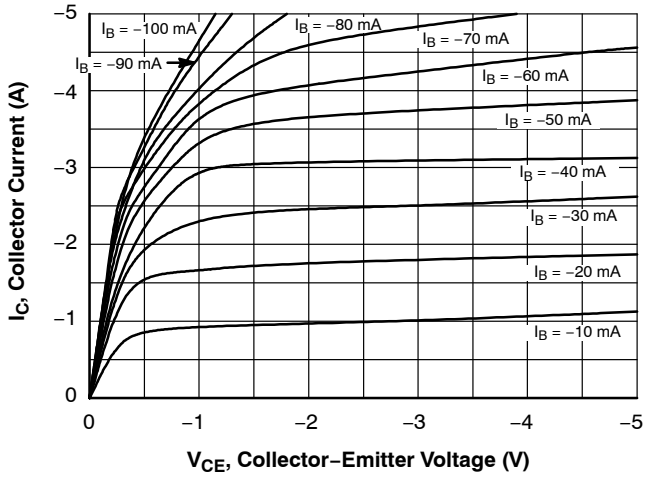


Figure 1. Static Characteristic

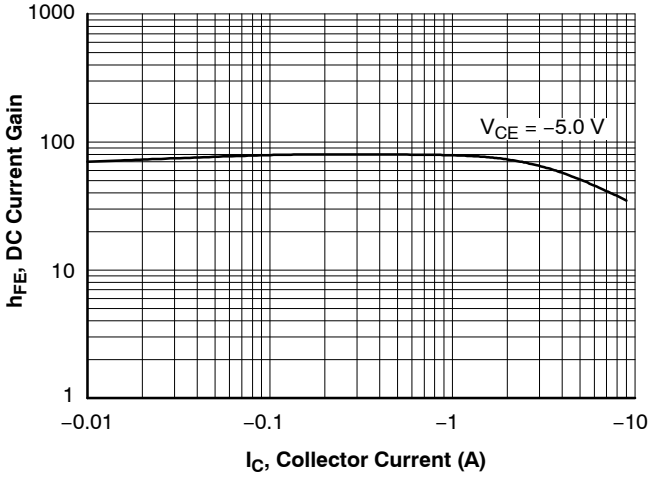


Figure 2. DC Current Gain

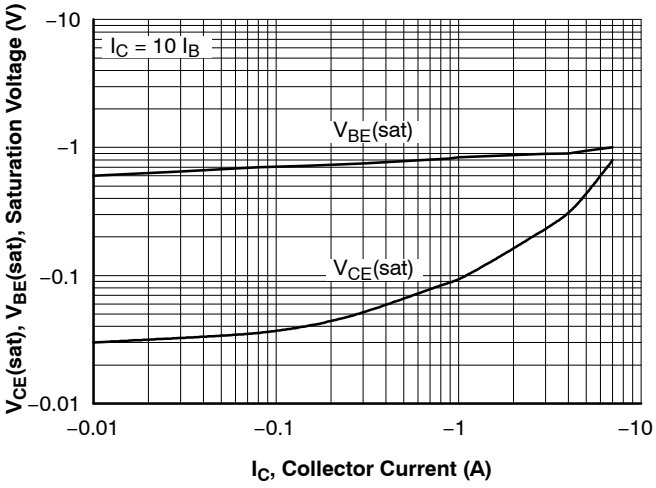


Figure 3. Base−Emitter Saturation Voltage Collector−Emitter Saturation Voltage

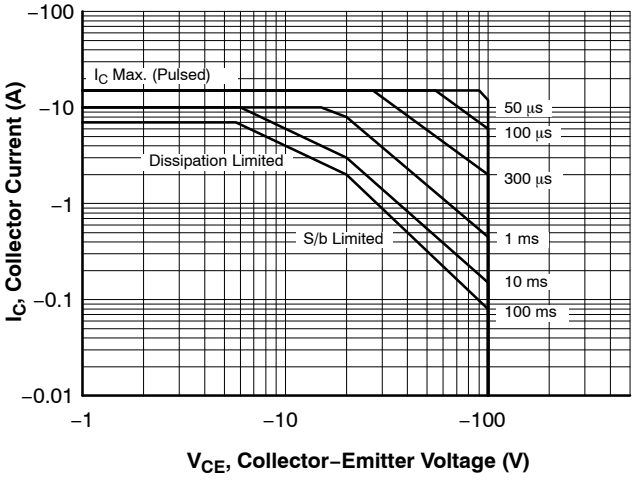


Figure 4. Safe Operating Area

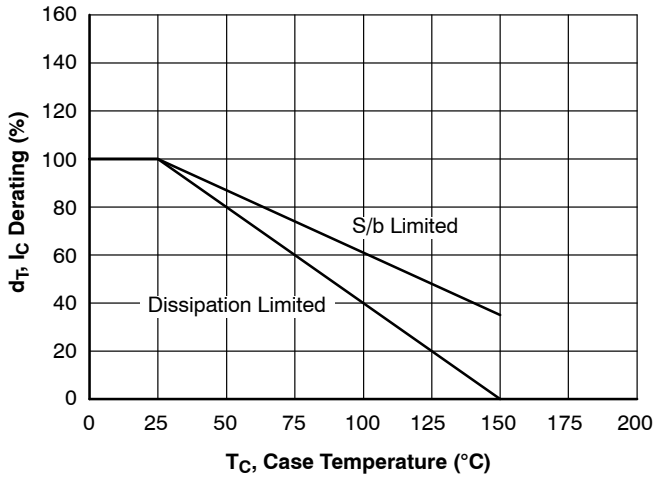


Figure 5. Derating Curve of Safe Operating Areas

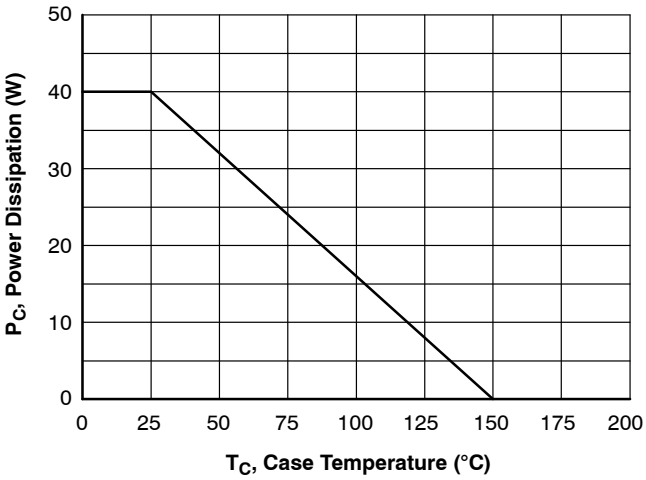


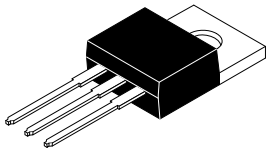
Figure 6. Power Derating

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



Scale 1:1

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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