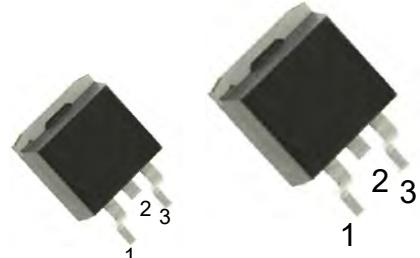


DESCRIPTION:

With high ability to withstand the shock loading of large current, BT151S-500R/650R/800R series of silicon controlled rectifiers provide high dv/dt rate with strong resistance to electromagnetic interference. They are especially recommended for use on solid state relay, motorcycle, power charger, T-tools etc.

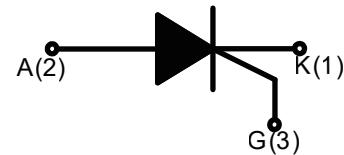


TO-252

TO-263

MAIN FEATURES

Symbol	Value	Symbol
V_{DRM}/ V_{RRM}	500/650/800	V
$I_{T(RMS)}$	12	A
I_{GT}	≤ 15	mA



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Storage junction temperature range	T_{stg}	-40 - 150	°C
Operating junction temperature range	T_j	-40 - 150	°C
Repetitive peak off-state voltage ($T_j=25^\circ\text{C}$)	V_{DRM}	500/650/800	V
Repetitive peak reverse voltage ($T_j=25^\circ\text{C}$)	V_{RRM}	500/650/800	V
RMS on-state current	$I_{T(RMS)}$	12	A
TO-252 ($T_c=115^\circ\text{C}$) TO-263 ($T_c=100^\circ\text{C}$)			
Non repetitive surge peak on-state current ($F=50\text{Hz } tp=10\text{ms}$)	I_{TSM}	120	A
Non repetitive surge peak on-state current ($F=60\text{Hz } tp=8.3\text{ms}$)	I_{TSM}	132	A
I^2t value for fusing ($tp=10\text{ms}$)	I^2t	72	A^2s
Repetitive rate of rise of on-state current ($I_G=2 \times I_{GT}$)	dI_T/dt	50	$\text{A}/\mu\text{s}$
Peak gate current	I_{GM}	2	A



BT151S BT151B series Thyristors



Peak gate power	P _{GM}	5	W
Average gate power dissipation	P _{G(AV)}	0.5	W

ELECTRICAL CHARACTERISTICS (T_j=25°C unless otherwise specified)

Symbol	Test Condition	Value			Unit
		MIN.	TYP.	MAX.	
I _{GT}	V _D =12V R _L =33Ω	-	4	15	mA
V _{GT}		-	0.75	1.5	V
V _{GD}	V _D =V _{DRM} T _j =150°C R _L =3.3KΩ	0.2	-	-	V
I _L	I _G =1.2I _{GT}	-	12	40	mA
I _H	I _T =500mA	-	12	30	mA
dV/dt	V _D =540V Gate Open T _j =150°C	50	-	-	V/μs
dV/dt	V _D =436V Gate Open T _j =150°C	80	-	-	V/μs
t _{on}	I _{GT} =20mA I _A =100mA I _R =10mA T _j =25°C	-	2	-	μs
t _{off}		-	30	-	μs
R _d	Dynamic resistance T _j =125°C	-	-	35	mΩ

STATIC CHARACTERISTICS

Symbol	Parameter		Value(MAX)	Unit
V _{TM}	I _{TM} =23A	t _p =380μs	1.6	V
I _{DRM}	V _D =V _{DRM}	T _j =25°C	10	μA
I _{RRM}		T _j =150°C	1	mA

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
R _{th(j-c)}	Junction to case	TO-252 1.3		°C/W
		TO-263	2.0	
R _{th(j-a)}	Junction to ambient	TO-252 70		
		TO-263	45	



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FIG.1: Maximum power dissipation versus RMS on-state current

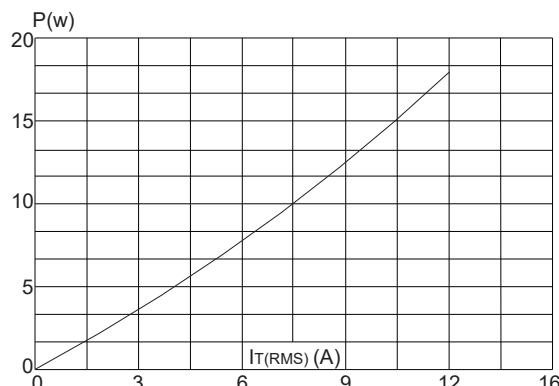


FIG.3: Surge peak on-state current versus number of cycles

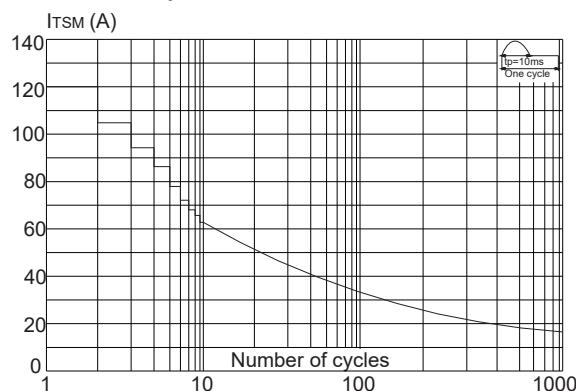


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10\text{ms}$, and corresponding value of I^2t ($\frac{dI}{dt} < 50\text{A}/\mu\text{s}$)

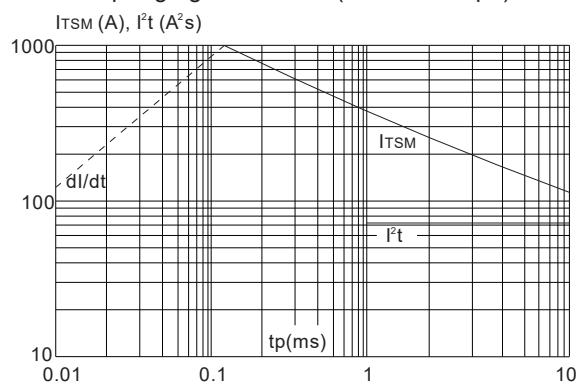


FIG.2: RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35 μm) (full cycle)

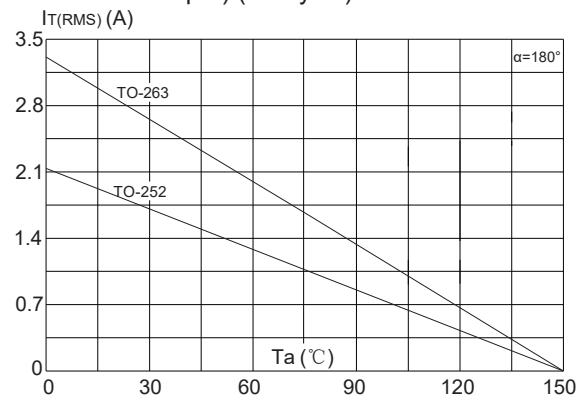


FIG.4: On-state characteristics (maximum values)

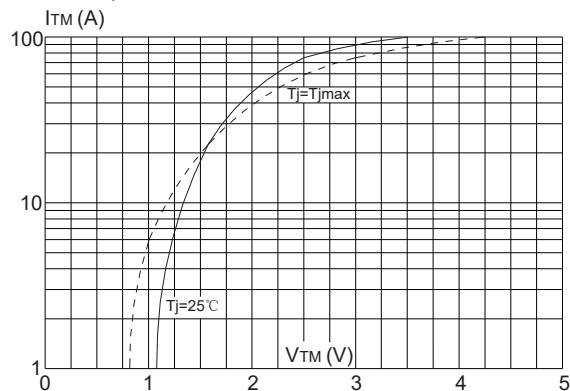
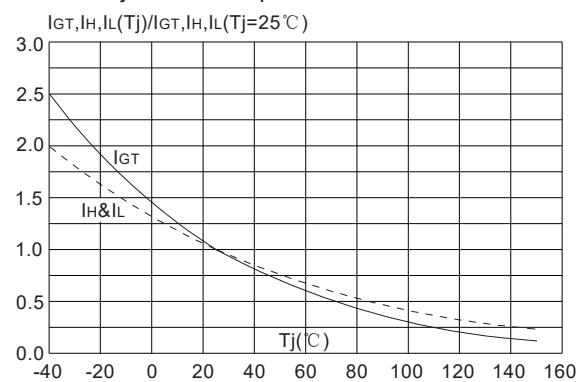
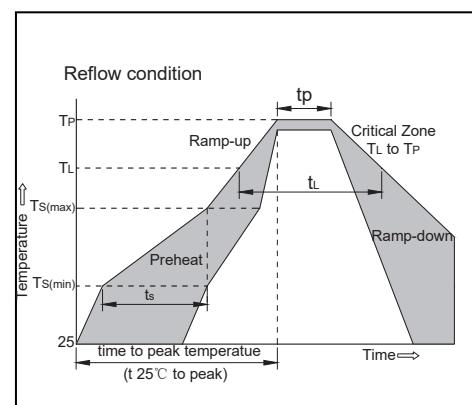


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature

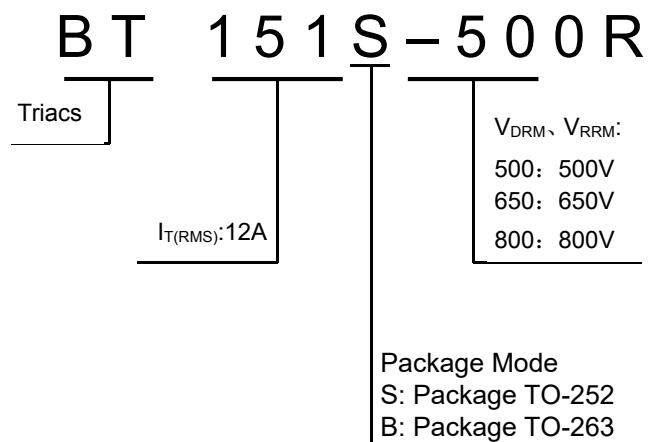


SOLDERING PARAMETERS

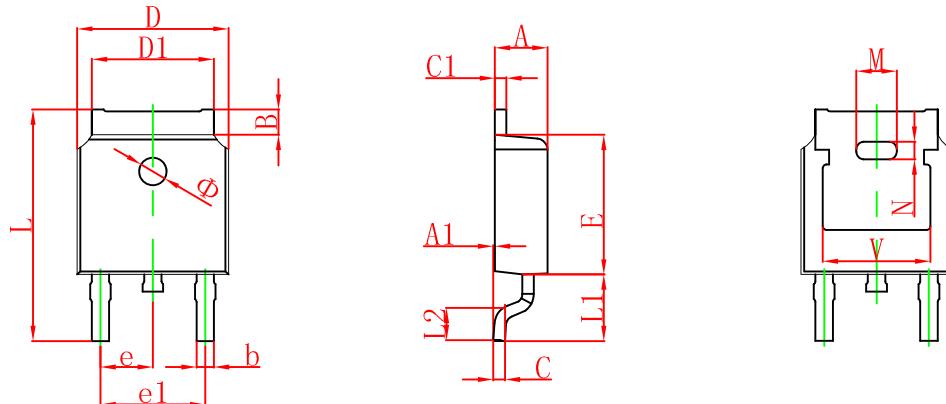
Reflow Condition		Pb-Free assembly (see figure at right)
Pre Heat	-Temperature Min ($T_{s(\min)}$)	+150°C
	-Temperature Max($T_{s(\max)}$)	+200°C
	-Time (Min to Max) (ts)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max
$T_{s(\max)}$ to T_L - Ramp-up Rate		3°C/sec. Max
Reflow	-Temperature(T_L) (Liquidus)	+217°C
	-Temperature(t_L)	60-150 secs.
Peak Temp (T_p)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		20-40secs.
Ramp-down Rate		6°C/sec. Max
Time 25°C to Peak Temp (T_p)		8 min. Max
Do not exceed		+260°C



ORDERING INFORMATION

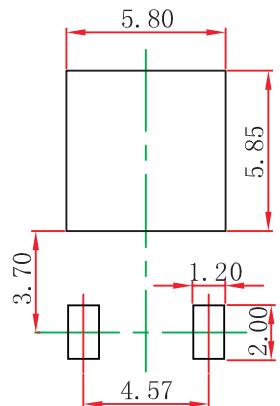


TO-252 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.380	0.087	0.094
A1	0.000	0.100	0.000	0.004
B	0.800	1.400	0.031	0.055
b	0.710	0.810	0.028	0.032
c	0.460	0.560	0.018	0.022
c1	0.460	0.560	0.018	0.022
D	6.500	6.700	0.256	0.264
D1	5.130	5.460	0.202	0.215
E	6.000	6.200	0.236	0.244
e	2.286 TYP.		0.090 TYP.	
e1	4.327	4.727	0.170	0.186
M	1.778REF.		0.070REF.	
N	0.762REF.		0.018REF.	
L	9.800	10.400	0.386	0.409
L1	2.9REF.		0.114REF.	
L2	1.400	1.700	0.055	0.067
V	4.830 REF.		0.190 REF.	
Φ	1.100	1.300	0.043	0.051

Suggested Pad Layout



Note:

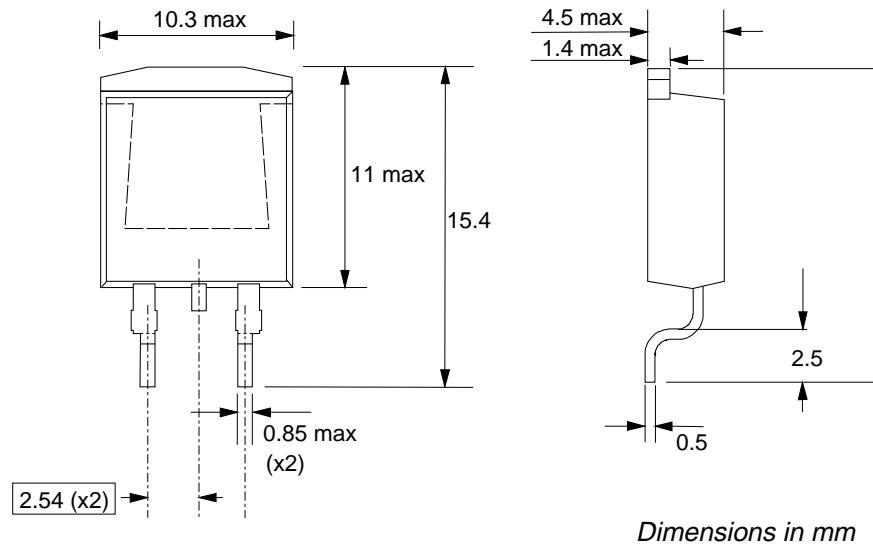
1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.05 mm.
3. The pad layout is for reference purposes only.



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TO-263(D2PAK) Package Outline Dimensions



Suggested Pad Layout

