74LVC14A

Hex inverting Schmitt trigger with 5 V tolerant input Rev. 10 — 4 August 2023 Product data sheet

1. General description

The 74LVC14A is a hex inverter with Schmitt-trigger inputs. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- CMOS low-power consumption
- · Direct interface with TTL levels
- · Unlimited input rise and fall times
- Complies with JEDEC standard JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Applications

- Wave and pulse shapers for highly noisy environments
- · Astable multivibrators
- · Monostable multivibrators

4. Ordering information

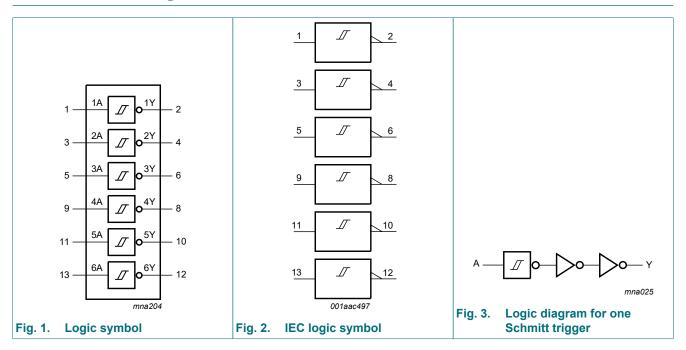
Table 1. Ordering information

Type number	Package					
	Temperature range	Name	Description	Version		
74LVC14AD	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1		
74LVC14APW	body width 4.4 mm					
74LVC14ABQ	-40 °C to +125 °C	o°C to +125 °C DHVQFN14 plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm				
74LVC14ABZ	·					



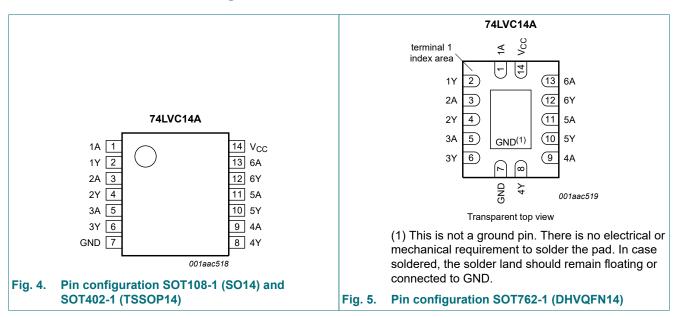
Hex inverting Schmitt trigger with 5 V tolerant input

5. Functional diagram

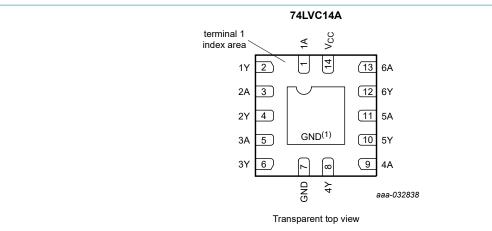


6. Pinning information

6.1. Pinning



Hex inverting Schmitt trigger with 5 V tolerant input



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 6. Pin configuration SOT8014-1 (DHXQFN14)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input nA	Output nY
L	Н
Н	L

3 / 16

Hex inverting Schmitt trigger with 5 V tolerant input

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
VI	input voltage	[1]	-0.5	+6.5	V
Vo	output voltage	[2]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
Io	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		SOT108-1; SOT402-1; SOT762-1 [3]	-	500	mW
		SOT8014-1 [4]	-	250	mW

^[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C

^[2] The output voltage ratings may be exceeded if the output current ratings are observed.

^[3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C. For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C. For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

^[4] For SOT8014-1 (DHXQFN14) package: P_{tot} derates linearly with 8.7 mW/K above 121 °C.

Hex inverting Schmitt trigger with 5 V tolerant input

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °	C to +85	°C	-40 °C to	+125 °C	Unit
			Min	Typ [1]	Max	Min	Max	
V _{OH}	HIGH-level	$V_I = V_{T+}$ or V_{T-}						
	output voltage	I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level	$V_I = V_{T+}$ or V_{T-}						
	voltage output	I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
l _l	input leakage current	$V_{CC} = 3.6 \text{ V}; V_{I} = 5.5 \text{ V or GND}$	-	±0.1	±5	-	±20	μA
I _{CC}	supply current	$V_{CC} = 3.6 \text{ V}; V_{I} = V_{CC} \text{ or GND}; I_{O} = 0 \text{ A}$	-	0.1	10	-	40	μΑ
Δl _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	μΑ
C _I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	4.0	-	-	-	pF

^[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

5 / 16

Hex inverting Schmitt trigger with 5 V tolerant input

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 8.

Symbol	Parameter	Conditions		-40	°C to +85	5 °C	-40 °C to	+125 °C	Unit
				Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Fig. 7	2]						
		V _{CC} = 1.2 V		-	16	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V		1.0	6.1	12.7	1.0	14.7	ns
		V _{CC} = 2.3 V to 2.7 V		1.5	3.5	7.8	1.5	10.0	ns
		V _{CC} = 2.7 V		1.5	3.6	7.5	1.5	9.5	ns
		V _{CC} = 3.0 V to 3.6 V		1.0	3.2	6.4	1.0	8.0	ns
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V	3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation	per buffer; V_I = GND to V_{CC}	4]						
	capacitance	V _{CC} = 1.65 V to 1.95 V		-	9.0	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V		-	12.5	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V		-	15.6	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz; f_o = output frequency in MHz

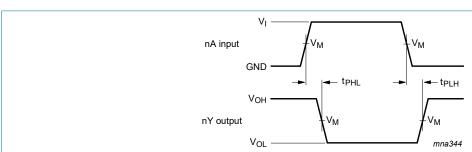
 C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1. Waveforms and test circuit



V_M = 1.5 V at V_{CC} ≥ 2.7 V

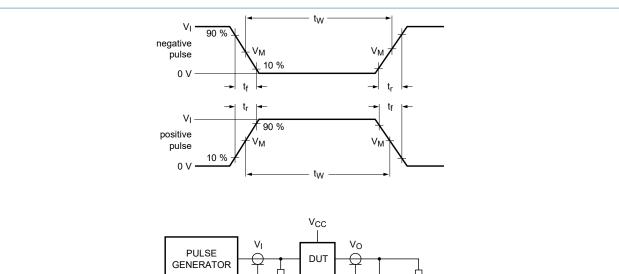
 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. Propagation delay input (nA) to output (nY)

Hex inverting Schmitt trigger with 5 V tolerant input

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Test data is given in <u>Table 8</u>. Definitions for test circuit:

R_L = Load resistance

C_L = Load capacitance including jig and probe capacitance

 R_{T} = Termination resistance should be equal to output impedance Z_{o} of the pulse generator.

Fig. 8. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input		Load			
	V _I	t _r , t _f	CL	R _L		
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ		
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ		
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω		
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω		
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω		

Hex inverting Schmitt trigger with 5 V tolerant input

12. Transfer characteristics

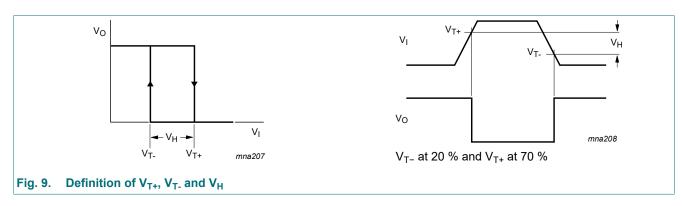
Table 9. Transfer characteristics

Voltages are referenced to GND (ground = 0 V); see Fig. 9.

Symbol	Parameter	Conditions	T _{amb} = -40 °	°C to +85 °C	T _{amb} = -40 °	C to +125 °C	Unit
			Min	Max	Min	Max	
V _{T+}	positive-going	V _{CC} = 1.2 V	0.2	1.0	0.2	1.0	V
	threshold voltage	V _{CC} = 1.65 V	0.4	1.3	0.4	1.3	V
		V _{CC} = 1.95 V	0.6	1.5	0.6	1.5	V
		V _{CC} = 2.3 V	8.0	1.7	0.8	1.7	V
		V _{CC} = 2.5 V	0.9	1.7	0.9	1.7	V
		V _{CC} = 2.7 V	1.1	2	1.1	2	V
		V _{CC} = 3 V	1.2	2	1.2	2	V
		V _{CC} = 3.6 V	1.2	2	1.2	2	V
V _{T-}	negative-going threshold voltage	V _{CC} = 1.2 V	0.12	0.75	0.12	0.75	V
		V _{CC} = 1.65 V	0.15	0.85	0.15	0.85	V
		V _{CC} = 1.95 V	0.25	0.95	0.25	0.95	V
		V _{CC} = 2.3 V	0.4	1.1	0.4	1.1	V
		V _{CC} = 2.5 V	0.4	1.2	0.4	1.2	V
		V _{CC} = 2.7 V	0.8	1.4	0.8	1.4	V
		V _{CC} = 3 V	8.0	1.5	0.8	1.5	V
		V _{CC} = 3.6 V	0.8	1.5	0.8	1.5	V
V _H	hysteresis voltage	V _{CC} = 1.2 V	0.1	1.0	0.1	1.0	V
	(V _{T+} - V _{T-})	V _{CC} = 1.65 V	0.2	1.15	0.2	1.15	V
		V _{CC} = 1.95 V	0.2	1.25	0.2	1.25	V
		V _{CC} = 2.3 V	0.3	1.3	0.3	1.3	V
		V _{CC} = 2.5 V	0.3	1.3	0.3	1.3	V
		V _{CC} = 2.7 V	0.3	1.1	0.3	1.1	V
		V _{CC} = 3 V	0.3	1.2	0.3	1.2	V
		$V_{CC} = 3.6 \text{ V}$ [1]	0.3	1.2	0.3	1.2	V

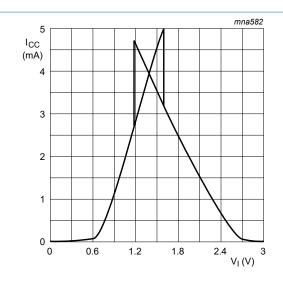
^[1] Typical transfer characteristic is displayed in Fig. 10.

12.1. Waveforms transfer characteristics



8 / 16

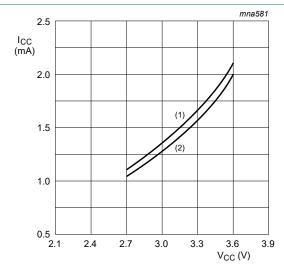
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 V_{CC} = 3.3 V.

Fig. 10. Typical transfer characteristic

13. Application information



- (1) Positive-going edge.
- (2) Negative going-edge.

Linear change of V_{I} between 0.8 V to 2.0 V.

All values given are typical unless otherwise specified.

Fig. 11. Average supply current as a function of supply voltage



 $f = \frac{1}{T} \approx \frac{1}{0.8 \times RC}$ at $V_{CC} = 3.0 \text{ V}$

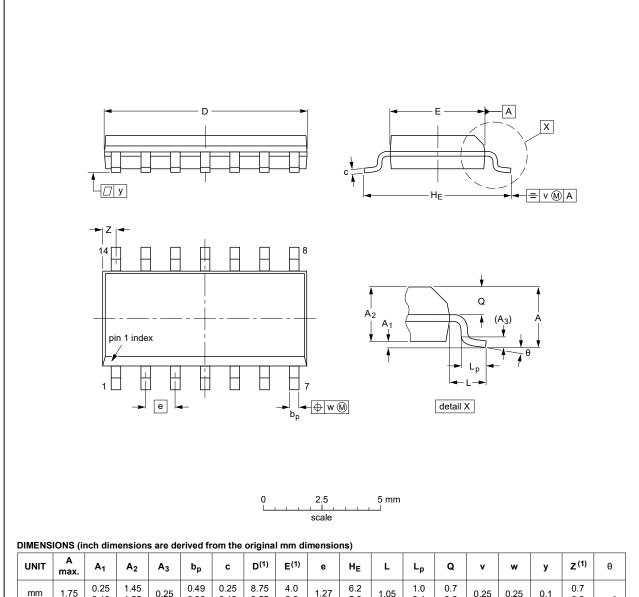
Fig. 12. Relaxation oscillator

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14. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

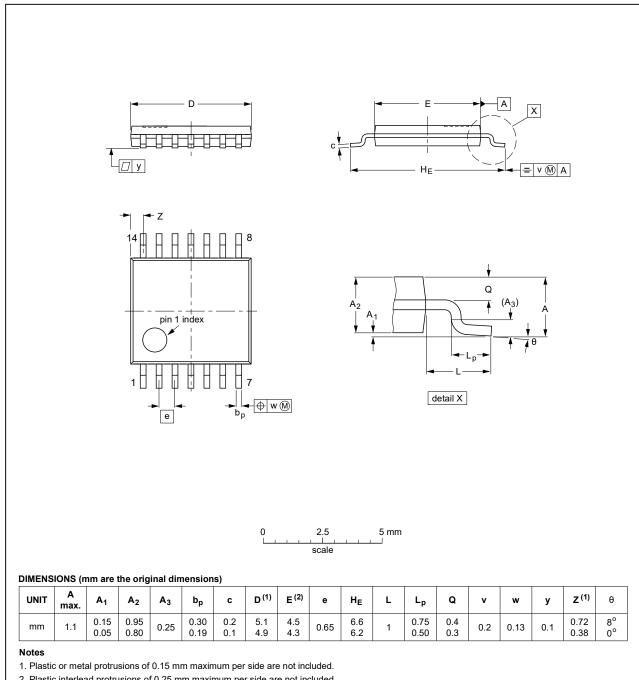
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	IEC	JEDEC	JEITA		PROJECTION	1330E DATE	
S	OT108-1	076E06	MS-012				99-12-27 03-02-19

Fig. 13. Package outline SOT108-1 (SO14)

Hex inverting Schmitt trigger with 5 V tolerant input

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION		REFER	EUROPEAN	ISSUE DATE		
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT402-1		MO-153				99-12-27 03-02-18

Fig. 14. Package outline SOT402-1 (TSSOP14)

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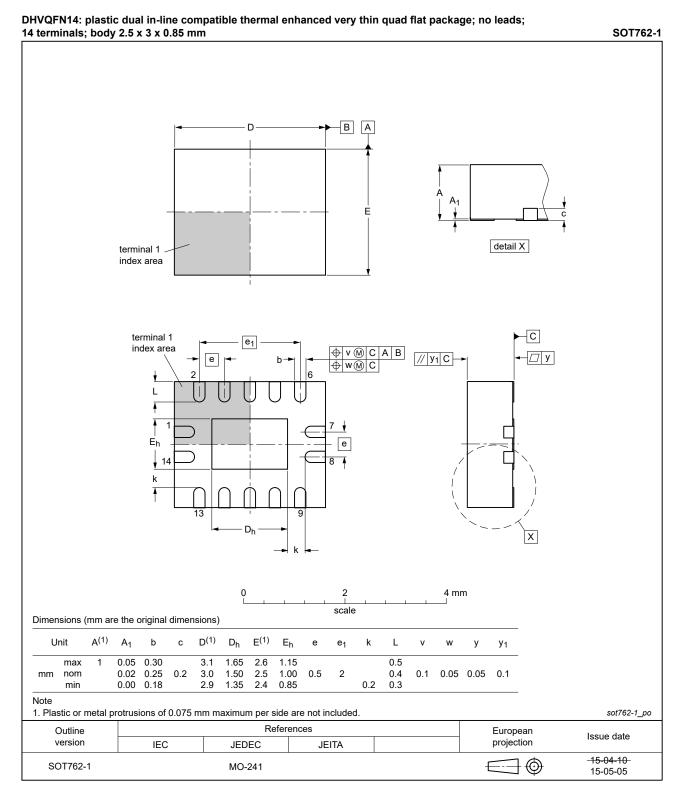


Fig. 15. Package outline SOT762-1 (DHVQFN14)

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DHXQFN14: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 14 terminals; 0.4 mm pitch; body 2 mm x 2 mm x 0.48 mm

SOT8014-1

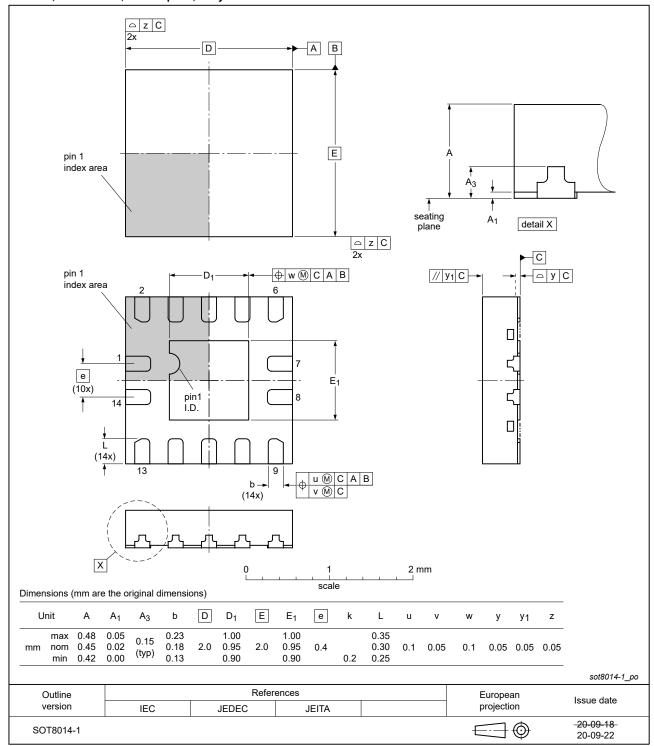


Fig. 16. Package outline SOT8014-1 (DHXQFN14)

Hex inverting Schmitt trigger with 5 V tolerant input

15. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74LVC14A v.10	20230804	Product data sheet	-	74LVC14A v.9		
Modifications:	Section 2:	<u>Section 2</u> : ESD specification updated according to the latest JEDEC standard.				
74LVC14A v.9	20210920	Product data sheet	-	74LVC14A v.8		
Modifications:	Type numb	Type number 74LVC14ADB (SOT337-1/SSOP14) removed.				
74LVC14A v.8	20210429	Product data sheet	-	74LVC14A v.7		
Modifications:	Type numb	Type number 74LVC14ABZ (SOT8014-1 / DHXQFN14) added.				
74LVC14A v.7	20200724	Product data sheet	-	74LVC14A v.6		
	guidelines Legal texts Section 1	Logar toxic flavor booth adapted to the flow delinparty flame whore appropriate.				
74LVC14A v.6	20160610	Product data sheet	-	74LVC14A v.5		
Modifications:	• <u>Table 4</u> : tal	<u>Table 4</u> : table note removed (errata).				
74LVC14A v.5	20111223	Product data sheet	-	74LVC14A v.4		
Modifications:	guidelines • Legal texts	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7 and Table 8: values added for lower voltage ranges. 				
74LVC14A v.4	20050215	Product data sheet	-	74LVC14A v.3		
74LVC14A v.3	20030228	Product specification	-	74LVC14A v.2		
74LVC14A v.2	20020315	Product specification	-	74LVC14A v.1		
74LVC14A v.1	19980428	Product specification		-		

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

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Hex inverting Schmitt trigger with 5 V tolerant input

Contents

1. General description	1
2. Features and benefits	1
3. Applications	1
4. Ordering information	1
5. Functional diagram	
6. Pinning information	
6.1. Pinning	
6.2. Pin description	
7. Functional description	
8. Limiting values	
9. Recommended operating conditions	
10. Static characteristics	
11. Dynamic characteristics	6
11.1. Waveforms and test circuit	
12. Transfer characteristics	
12.1. Waveforms transfer characteristics	8
13. Application information	
14. Package outline	
15. Abbreviations	
16. Revision history	
17. Legal information	
-	

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