ShinDengen

P33LF6QLKD

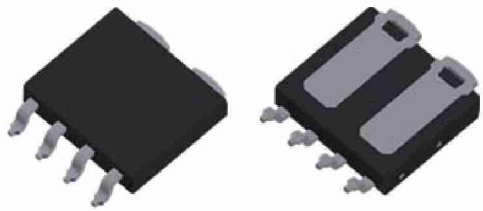
Power MOSFETs
60V, 33A, Dual N-channel

Feature

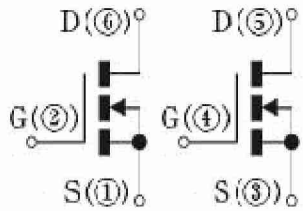
- N-channel
- Small SMD
- Dual type
- 4.5V Gate Drive
- Low Capacitance
- Based on AEC-Q101
- Halogen free
- Pb free terminal
- RoHS:Yes

OUTLINE

Package (House Name): LF_Dual



Equivalent circuit



Absolute Maximum Ratings (unless otherwise specified : Tc=25℃, per FET)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 175	℃
Channel tempertature	Tch		-55 to 175	℃
Drain-source voltage	V_{DSS}		60	V
Gate-source voltage	V_{GSS}		±20	V
Continuous drain current(DC)	I_D		33	A
Continuous drain current(Peak)	I_{DP}	Pulse width 10μs, duty=1/100	99	A
Continuous source current(DC)	Is		33	A
Total power dissipation	P_T	With heatsink	50	W
Total power dissipation	P_T	※	2.5	W
Total power dissipation	P_T	※	1.5	W
Single avalanche current	I_{AS}	Starting Tch=25℃ Tch≦150℃	20	A
Single avalanche energy	E_{AS}	Starting Tch=25℃ Tch≦150℃	43	mJ

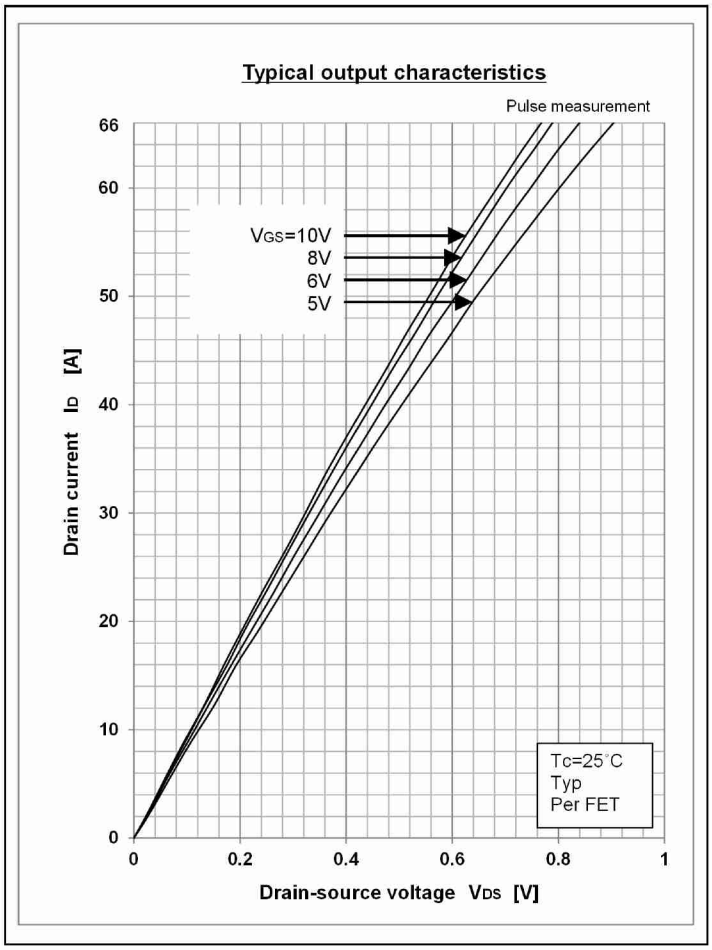
※ :See the original Specifications

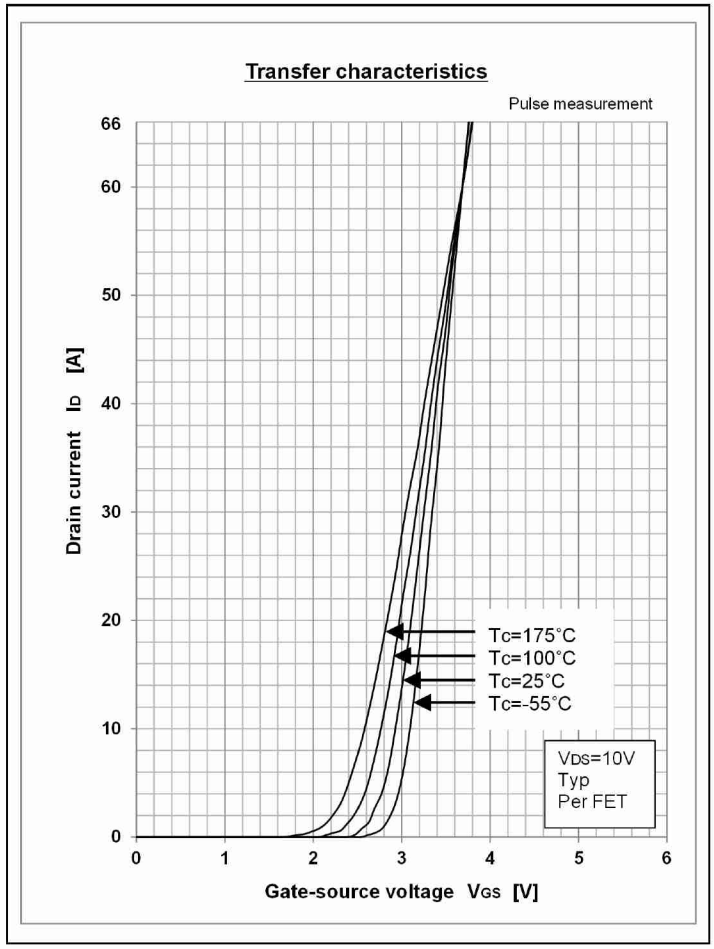
Electrical Characteristics (unless otherwise specified : Tc=25°C, per FET)

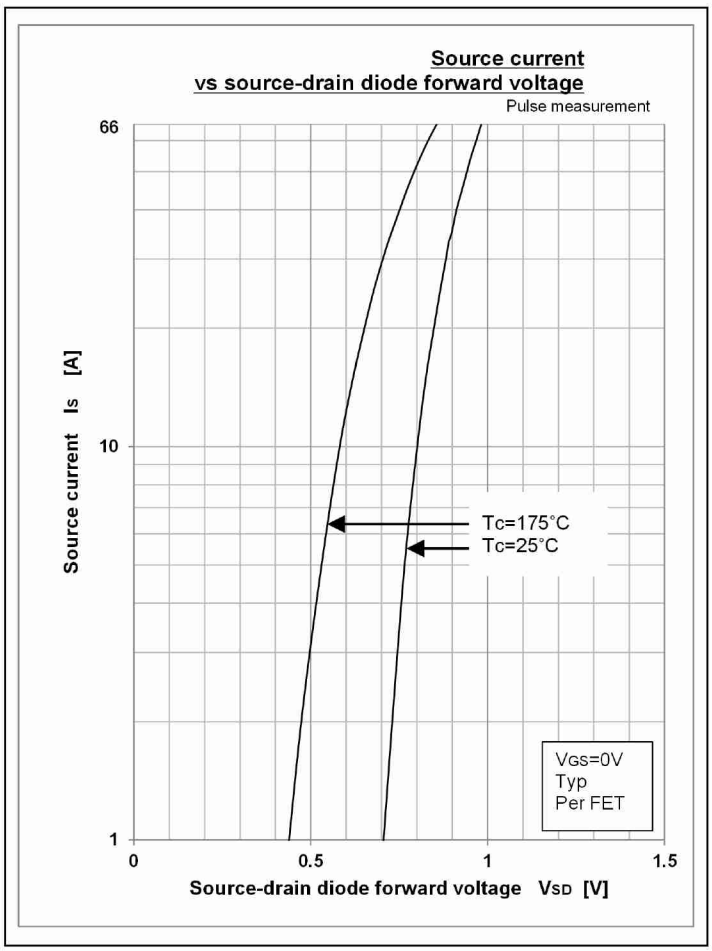
Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	60			V
Zero gate voltage drain current	I_{DSS}	VDS=60V, VGS=0V			1	μA
Gate-source leakage current	I_{GSS}	VGS=±20V, VDS=0V			±0.1	μA
Forward transconductance	g_{fs}	ID=16.5A, VDS=10V	9			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=16.5A, VGS=10V		0.0105	0.0131	Ω
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=16.5A, VGS=4.5V		0.0127	0.0169	Ω
Gate threshold voltage	Vth	ID=1mA, VDS=10V	1.5	2	2.5	V
Source-drain diode forward voltage	V_{SD}	IS=33A, VGS=0V			1.2	V
Thermal resistance	Rth(j-c)	Junction to case			2.98	°C/W
Thermal resistance	Rth(j-a)	Junction to ambient ※			60	°C/W
Thermal resistance	Rth(j-a)	Junction to ambient ※			100	°C/W
Total gate charge	Qg	VDD=48V, VGS=10V, ID=33A		37		nC
Gate to source charge	Qgs	VDD=48V, VGS=10V, ID=33A		8		nC
Gate to drain charge	Qgd	VDD=48V, VGS=10V, ID=33A		10		nC
Input capacitance	Ciss	VDS=25V, VGS=0V, f=1MHz		1913		pF
Reverce transfer capacitnce	Crss	VDS=25V, VGS=0V, f=1MHz		83		pF
Output capacitance	Coss	VDS=25V, VGS=0V, f=1MHz		175		pF
Turn-on delay time	td(on)	ID=16.5A, RL=1.82Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		5.5		ns
Rise time	tr	ID=16.5A, RL=1.82Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		16		ns
Turn-off delay time	td(off)	ID=16.5A, RL=1.82Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		22		ns
Fall time	tf	ID=16.5A, RL=1.82Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		4.5		ns
Diode reverse recovery time	trr	IF=33A, VGS=0V, di/dt=100A/μs		39		ns
Diode reverse recovery charge	Qrr	IF=33A, VGS=0V, di/dt=100A/μs		40		nC

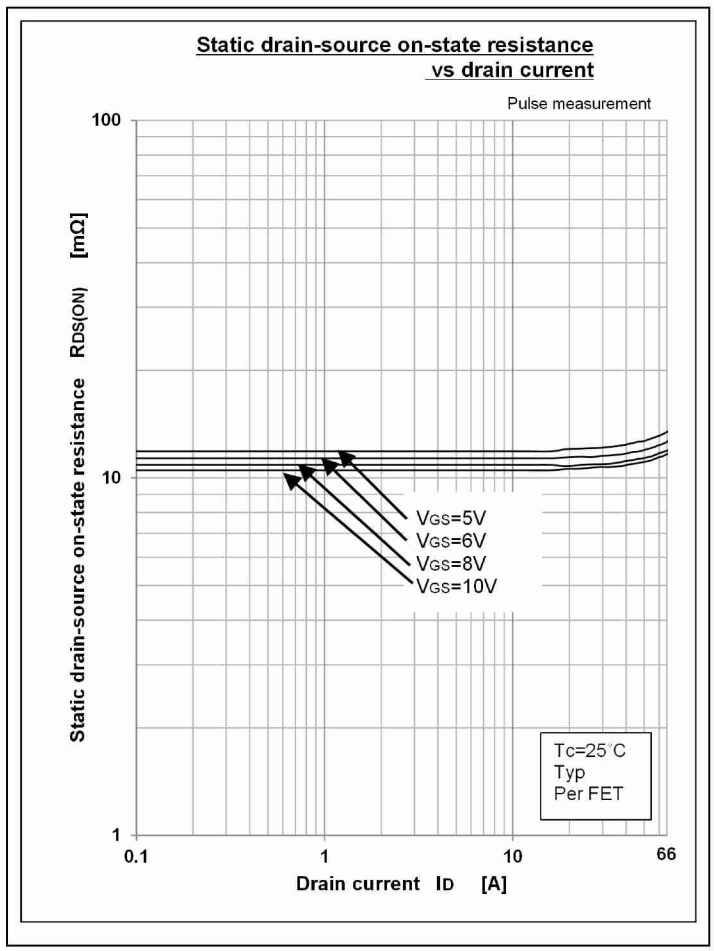
※ :See the original Specifications

CHARACTERISTIC DIAGRAMS

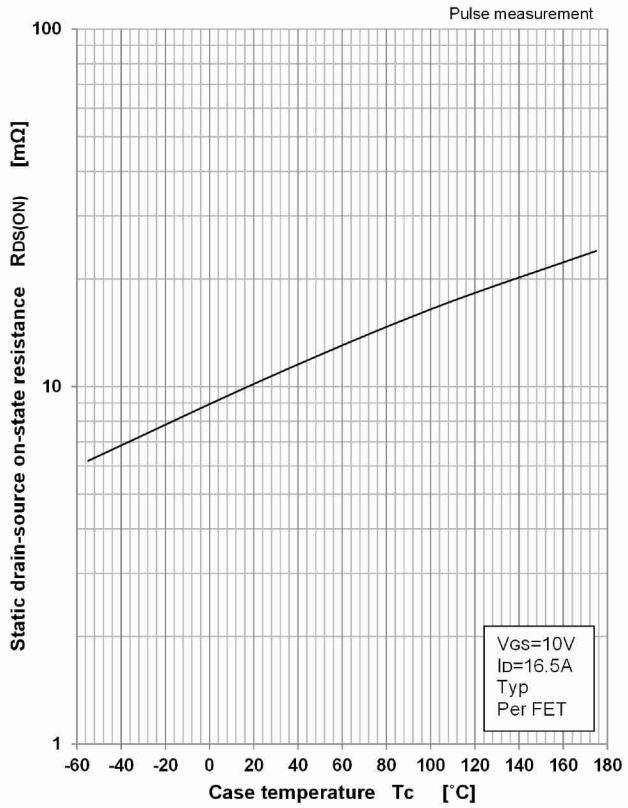




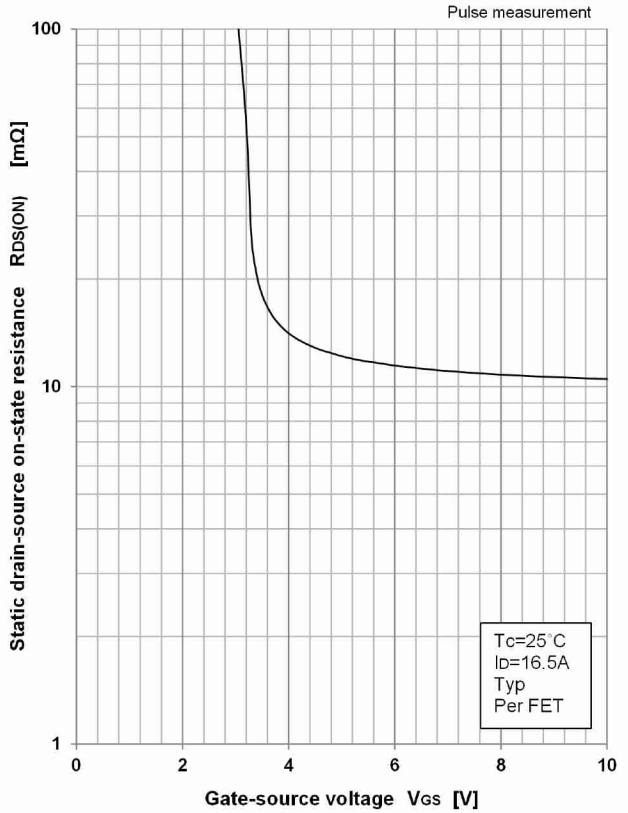




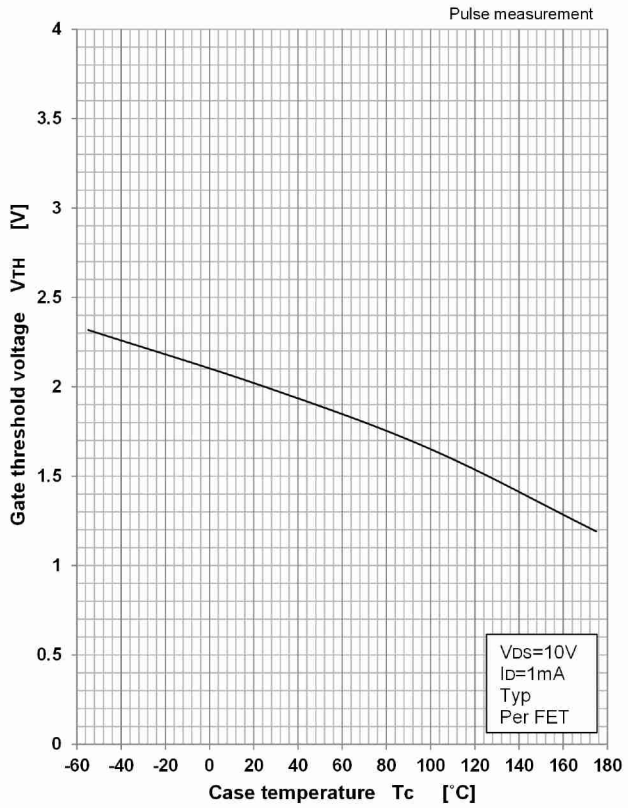
Static drain-source on-state resistance vs case temperature



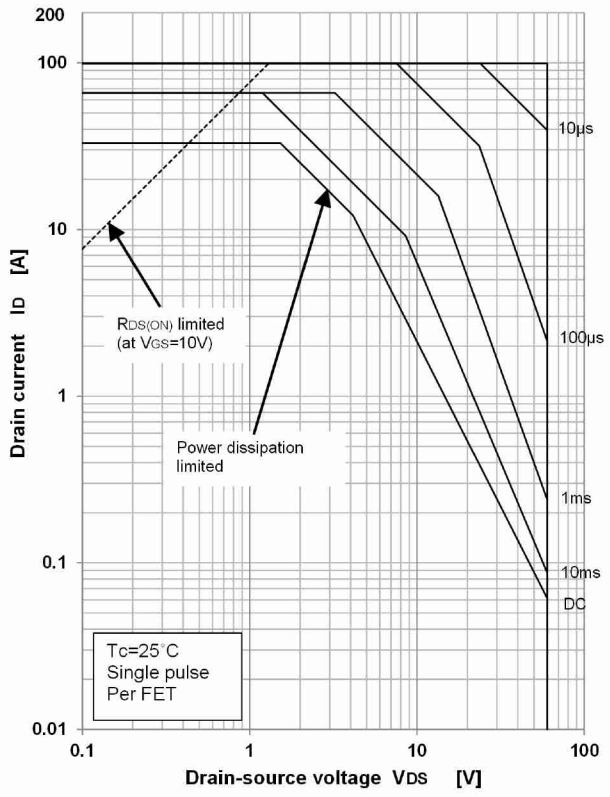
Static drain-source on-state resistance vs gate-source voltage

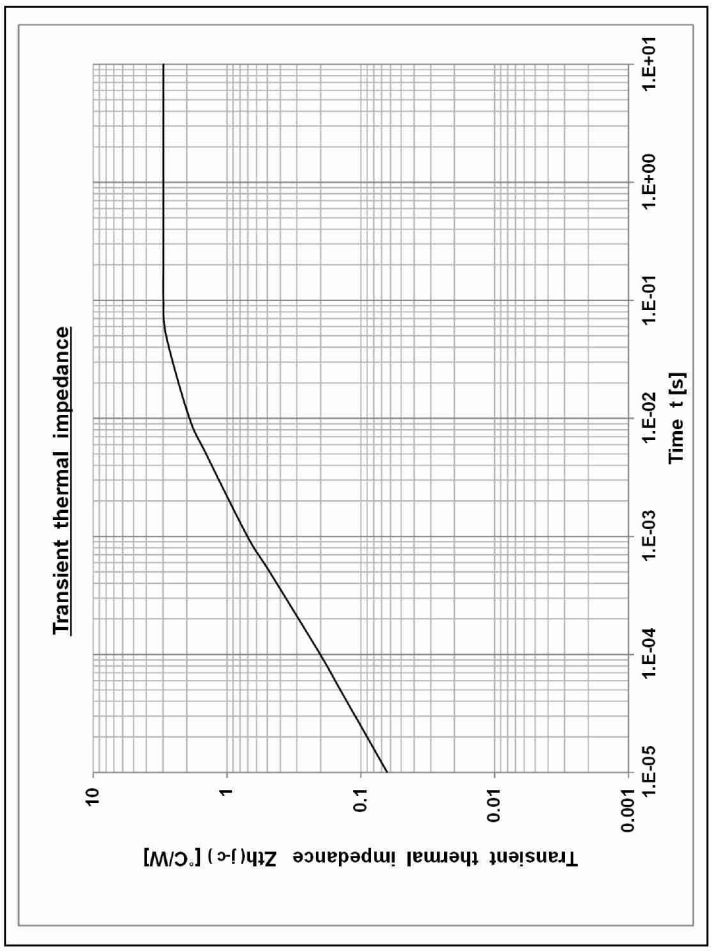


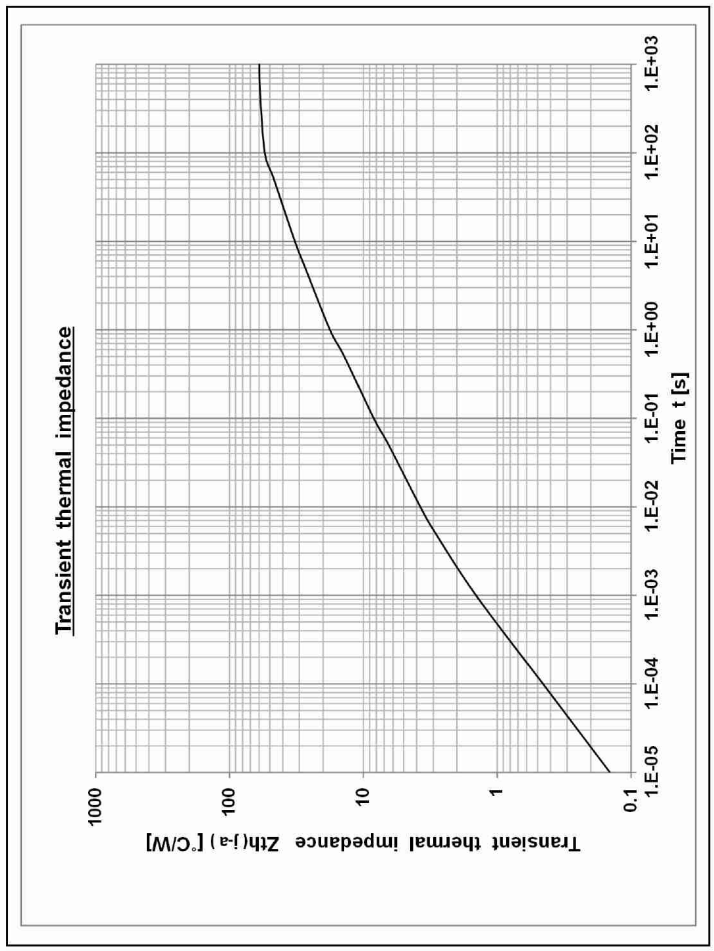
Gate threshold voltage vs case temperature

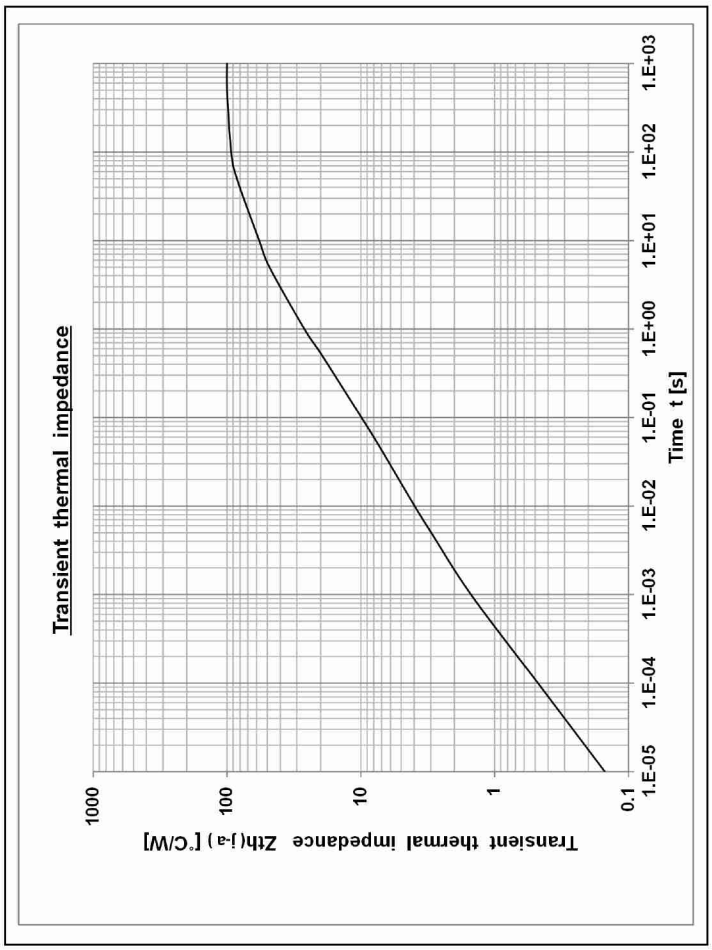


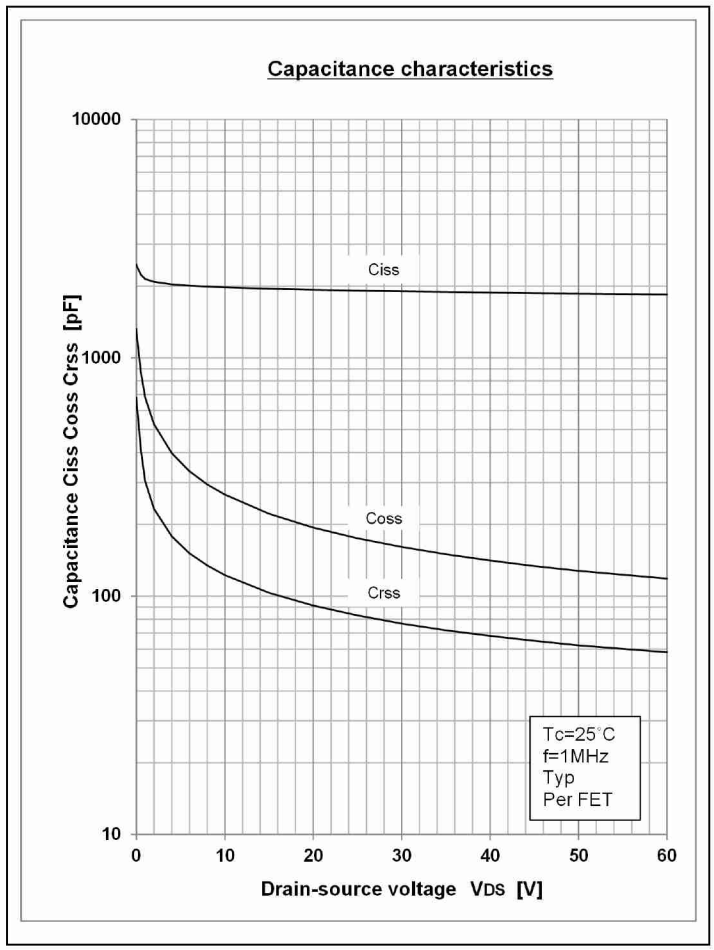
Safe operating area



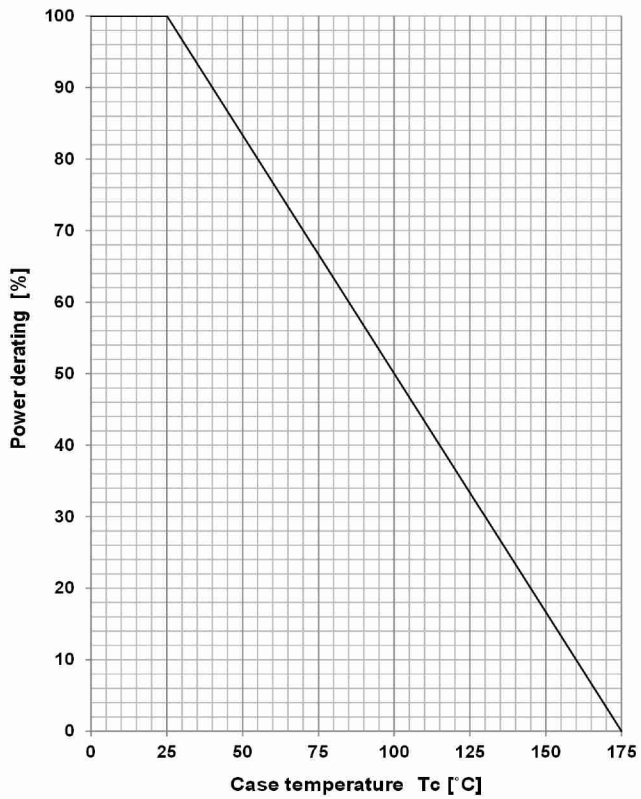

Transient thermal impedance
Transient thermal impedance Zth(j-c) [°C/W]
Time t [s]
10
1
0.1
0.01
0.001
1.E-05
1.E-04
1.E-03
1.E-02
1.E-01
1.E+00
1.E+01


Transient thermal impedance
Transient thermal impedance Zth(j-a) [°C/W]
Time t [s]
1000
100
10
1
0.1
1.E-05
1.E-04
1.E-03
1.E-02
1.E-01
1.E+00
1.E+01
1.E+02
1.E+03

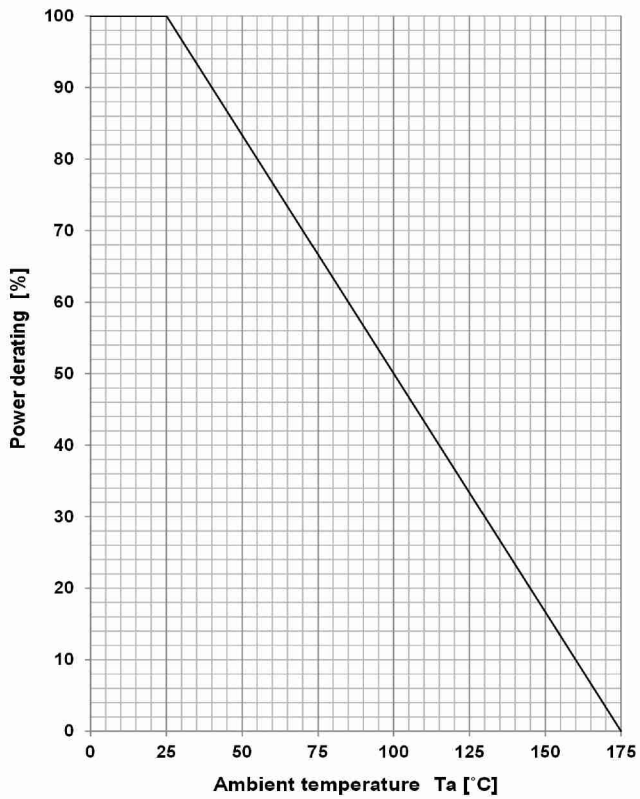

Transient thermal impedance
Transient thermal impedance Zth(j-a) [°C/W]
Time t [s]
1000
100
10
1
0.1
1.E-05
1.E-04
1.E-03
1.E-02
1.E-01
1.E+00
1.E+01
1.E+02
1.E+03


Capacitance characteristics
Capacitance Ciss Coss Crss [pF]
Drain-source voltage VDS [V]
Ciss
Coss
Crss
Tc=25°C
f=1MHz
Typ
Per FET
10000
1000
100
10
0
10
20
30
40
50
60

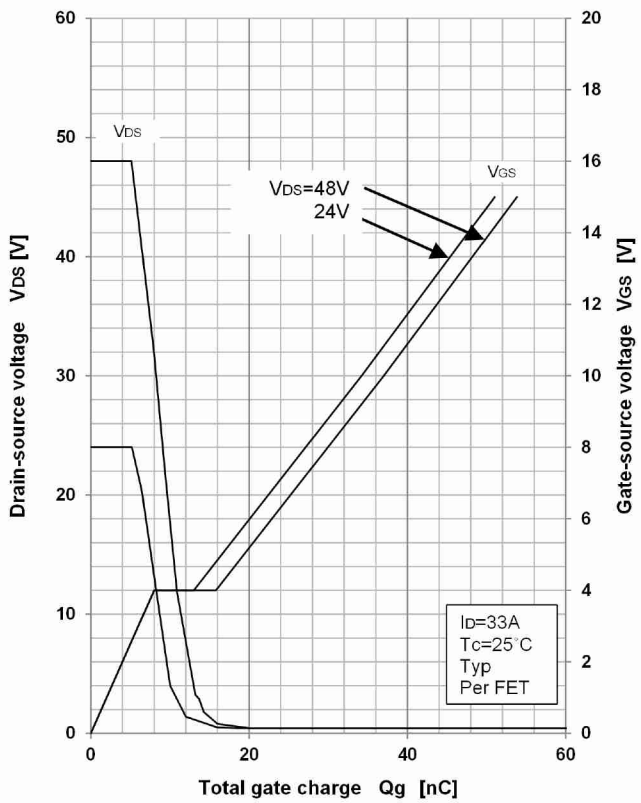
Power derating vs case temperature



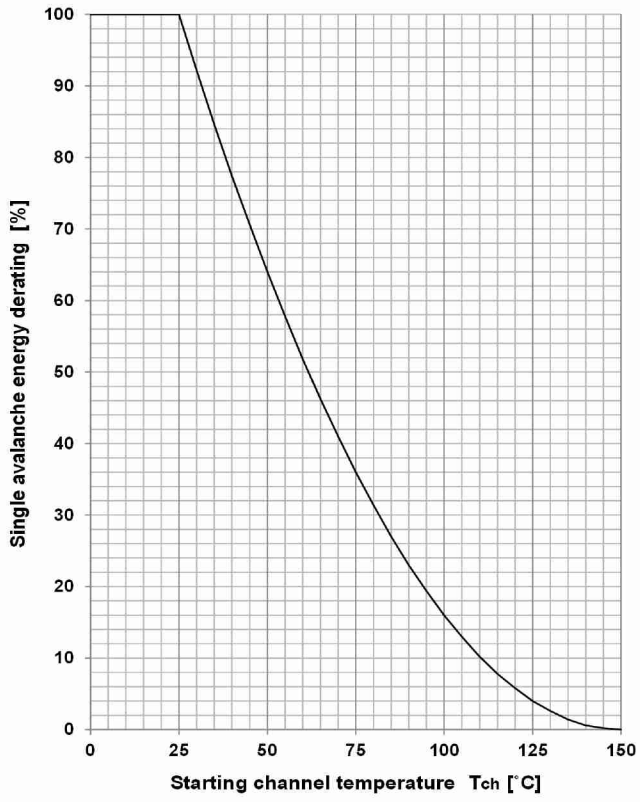
Power derating vs ambient temperature



Gate charge characteristics



Single avalanche energy derating vs starting channel temperature

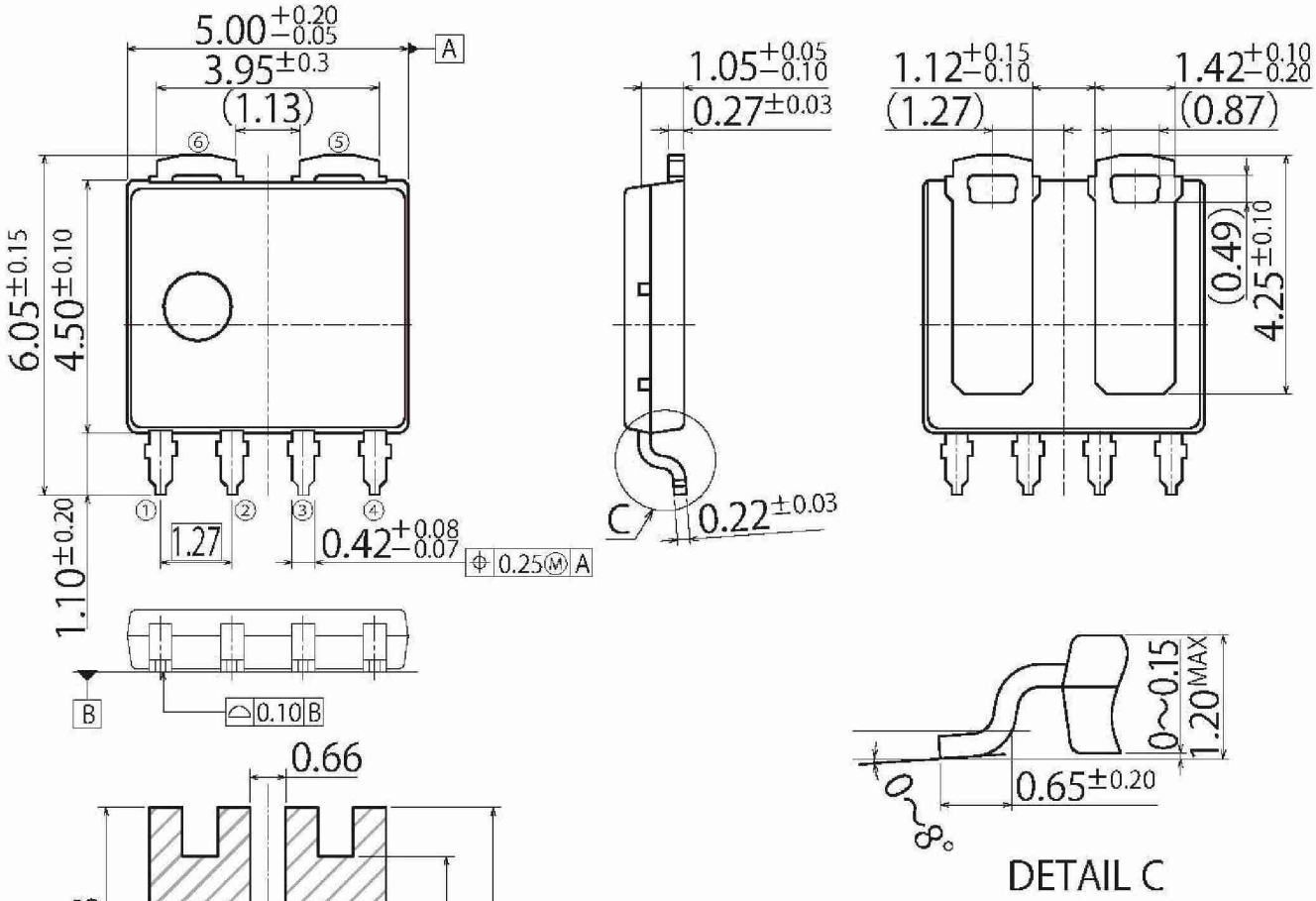


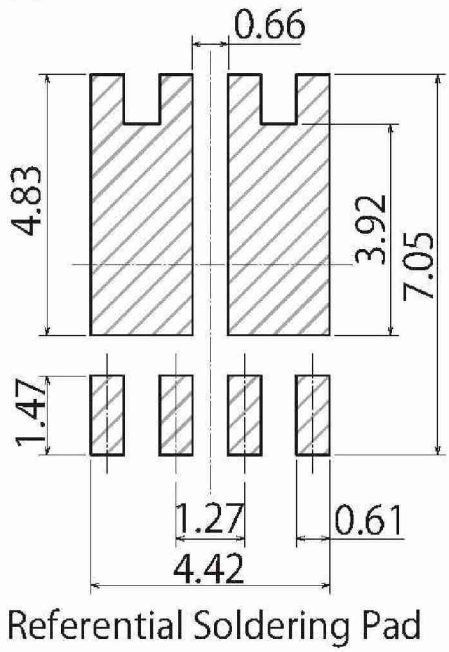
Outline Dimensions

unit:mm

G8

JEDEC Code	–
JEITA Code	–
House Name	LF_Dual





Referential Soldering Pad

Notes

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