

EEPROM Serial 64-Kb I²C - Automotive Grade 1

NV24C64LV

Description

The NV24C64LV is a EEPROM Serial 64-Kb I²C – Automotive Grade 1 device, organized internally as 256 pages of 32 bytes each. This device supports the Standard (100 kHz), Fast (400 kHz) and Fast-Plus (1 MHz) I²C protocol.

Data is written by providing a starting address, then loading 1 to 32 contiguous bytes into a Page Write Buffer, and then writing all data to non-volatile memory in one internal write cycle. Data is read by providing a starting address and then shifting out data serially while automatically incrementing the internal address count.

External address pins make it possible to address up to eight NV24C64LV devices on the same bus.

Features

- Automotive AEC-Q100 Grade 1 (–40°C to +125°C) Qualified
- Supports Standard, Fast and Fast-Plus I²C Protocol
- 1.7 V to 5.5 V Supply Voltage Range
- 32-Byte Page Write Buffer
- Fast Write Time (4 ms max)
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Automotive Grade 1 Temperature Range
- US-8, UDFN-8, SOIC-8 and TSSOP-8 Packages
- These Devices are Pb-Free, Halogen Free/BFR Free, and RoHS Compliant



ON Semiconductor®

www.onsemi.com



US8
U SUFFIX
CASE 493



UDFN-8
MUW3 SUFFIX
CASE 517DH

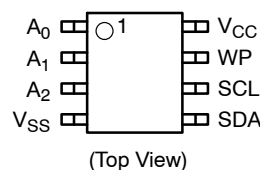


SOIC-8
DW SUFFIX
CASE 751BD



TSSOP-8
DT SUFFIX
CASE 948AL

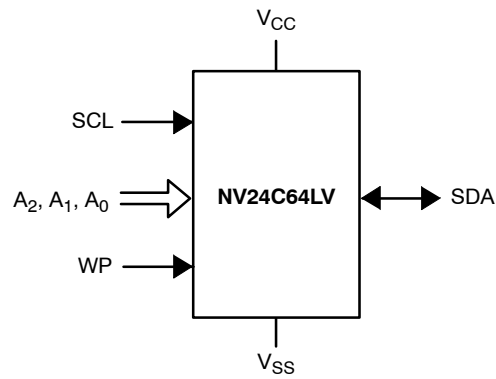
PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 9 of this data sheet.

NV24C64LV



PIN FUNCTION

Pin Name	Function
A ₀ , A ₁ , A ₂	Device Address
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V _{CC}	Power Supply
V _{SS}	Ground

Figure 1. Functional Symbols

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	-0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than -0.5 V or higher than $V_{CC} + 0.5$ V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than $V_{CC} + 1.5$ V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Max	Units
N _{END} (Note 2)	Endurance	1,000,000	Write Cycles (Note 3)
T _{DR} (Note 2)	Data Retention	100	Years

2. T_A = 25°C

3. A Write Cycle refers to writing a Byte or a Page.

NV24C64LV

Table 3. D.C. OPERATING CHARACTERISTICS ($V_{CC} = 1.7 \text{ V}$ to 5.5 V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CCR}	Read Current	Read, $f_{SCL} = 1 \text{ MHz}$		1	mA
I_{CCW}	Write Current	Write, $f_{SCL} = 1 \text{ MHz}$		1	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}		2	μA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}		2	μA
V_{IL}	Input Low Voltage	SCL, SDA	-0.5	$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage	SCL, SDA	$V_{CC} \times 0.7$	$V_{CC} + 0.5$	V
V_{ILA}	Input Low Voltage	A2, A1, A0 and WP	-0.5	$V_{CC} \times 0.3$	V
V_{IHA}	Input High Voltage	A2, A1, A0 and WP	$V_{CC} \times 0.8$	$V_{CC} + 0.5$	V
V_{OL1}	Output Low Voltage	$V_{CC} \geq 2.5 \text{ V}$, $I_{OL} = 3.0 \text{ mA}$		0.4	V
V_{OL2}	Output Low Voltage	$V_{CC} < 2.5 \text{ V}$, $I_{OL} = 1.0 \text{ mA}$		0.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. PIN IMPEDANCE CHARACTERISTICS ($V_{CC} = 1.7 \text{ V}$ to 5.5 V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Max	Units
C_{IN} (Note 4)	SDA I/O Pin Capacitance	$V_{IN} = 0 \text{ V}$		8	pF
C_{IN} (Note 4)	Input Capacitance (other pins)	$V_{IN} = 0 \text{ V}$		6	pF
R_{PD} (Note 5)	WP, A0, A1 or A2 On-Chip Pull-Down Resistor	$V_{IN} < V_{IHA}$	50		$k\Omega$
I_{PD} (Note 5)	WP, A0, A1 or A2 On-Chip Pull-Down Current	$V_{IN} > V_{IHA}$		2	μA

- These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
- For improved noise immunity (and to allow for floating input pins), the WP, A0, A1 & A2 inputs are pulled-down to GND by relatively strong on-chip resistors. When attempting to drive these inputs High, the external drivers must be able to supply sufficient current, until the input level at the pin exceeds V_{IHA} . Once the input level at the pin exceeds V_{IHA} , the resistive pull-down (R_{PD}) converts to a constant current pull-down (I_{PD}).

NV24C64LV

Table 5. A.C. CHARACTERISTICS ($V_{CC} = 1.7 \text{ V}$ to 5.5 V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ unless otherwise noted.) (Note 6)

Symbol	Parameter	Standard		Fast		Fast-Plus		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.25		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.45		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.40		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.25		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
t_R (Note 7)	SDA and SCL Rise Time		1,000		300		100	ns
t_F (Note 7)	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.40	μs
t_{DH} (Note 7)	Data Out Hold Time	100		100		50		ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		50		50		50	ns
$t_{SU:WP}$	WP Setup Time	0		0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		1		μs
t_{WR}	Write Cycle Time		4		4		4	ms
t_{PU} (Notes 7, 8)	Power-up to Ready Mode		0.35		0.35		0.35	ms

* $V_{CC(\min)} = 1.6 \text{ V}$ for Read operations, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$

6. Test conditions according to "A.C. Test Conditions" table.

7. Tested initially and after a design or process change that affects this parameter.

8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. A.C. TEST CONDITIONS

Input Levels	$0.2 \times V_{CC}$ to $0.8 \times V_{CC}$ for $V_{CC} \geq 2.2 \text{ V}$; $0.15 \times V_{CC}$ to $0.85 \times V_{CC}$ for $V_{CC} < 2.2 \text{ V}$
Input Rise and Fall Times	$\leq 50 \text{ ns}$
Input Reference Levels	$0.3 \times V_{CC}$, $0.7 \times V_{CC}$
Output Reference Levels	$0.3 \times V_{CC}$, $0.7 \times V_{CC}$
Output Load	Current Source: $I_{OL} = 6 \text{ mA}$ ($V_{CC} \geq 2.5 \text{ V}$); $I_{OL} = 2 \text{ mA}$ ($V_{CC} < 2.5 \text{ V}$); $C_L = 100 \text{ pF}$

Power-On Reset (POR)

Each NV24C64LV incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi-directional POR behavior protects the device against 'brown-out' failure following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the clock signal generated by the Master.

SDA: The Serial Data I/O pin accepts input data and delivers output data. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A₀, A₁ and A₂: The Address inputs set the device address that must be matched by the corresponding Slave address bits. The Address inputs are hard-wired HIGH or LOW allowing for up to eight devices to be used (cascaded) on the same bus. When left floating, these inputs are pulled LOW internally.

WP: When pulled HIGH, the Write Protect input pin inhibits all write operations. When left floating, this pin is pulled LOW internally.

Functional Description

The NV24C64LV supports the Inter-Integrated Circuit (I²C) Bus protocol. The protocol relies on the use of a Master device, which provides the clock and directs bus traffic, and Slave devices which execute requests. The NV24C64LV operates as a Slave device. Both Master and Slave can transmit or receive, but only the Master can assign those roles.

I²C Bus Protocol

The 2-wire I²C bus consists of two lines, SCL and SDA, connected to the V_{CC} supply via pull-up resistors. The Master provides the clock to the SCL line, and either the Master or the Slaves drive the SDA line. A '0' is transmitted by pulling a line LOW and a '1' by letting it stay HIGH. Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics). During data transfer, SDA must remain stable while SCL is HIGH.

START/STOP Condition

An SDA transition while SCL is HIGH creates a START or STOP condition (Figure 2). The START consists of a HIGH to LOW SDA transition, while SCL is HIGH. Absent the START, a Slave will not respond to the Master. The STOP completes all commands, and consists of a LOW to HIGH SDA transition, while SCL is HIGH.

Device Addressing

The Master addresses a Slave by creating a START condition and then broadcasting an 8-bit Slave address. For the NV24C64LV, the first four bits of the Slave address are set to 1010 (Ah); the next three bits, A₂, A₁ and A₀, must match the logic state of the similarly named input pins. The R/W bit tells the Slave whether the Master intends to read (1) or write (0) data (Figure 3).

Acknowledge

During the 9th clock cycle following every byte sent to the bus, the transmitter releases the SDA line, allowing the receiver to respond. The receiver then either acknowledges (ACK) by pulling SDA LOW, or does not acknowledge (NoACK) by letting SDA stay HIGH (Figure 4). Bus timing is illustrated in Figure 5.

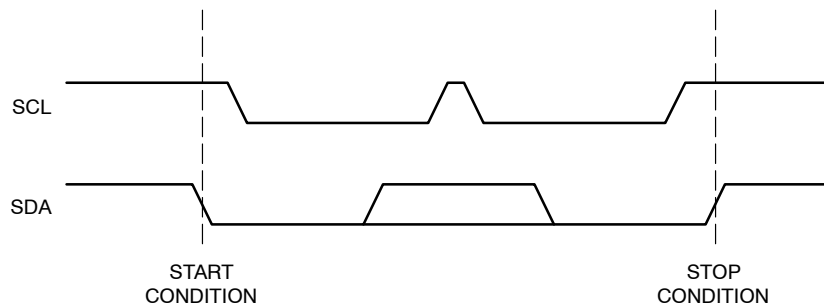


Figure 2. Start/Stop Timing

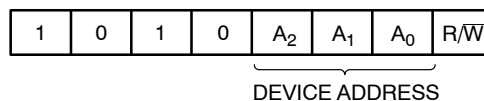


Figure 3. Slave Address Bits

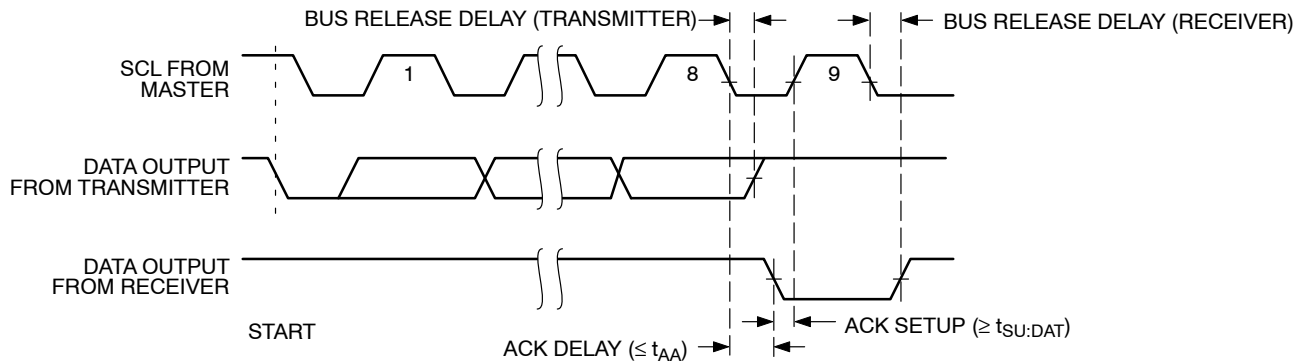


Figure 4. Acknowledge Timing

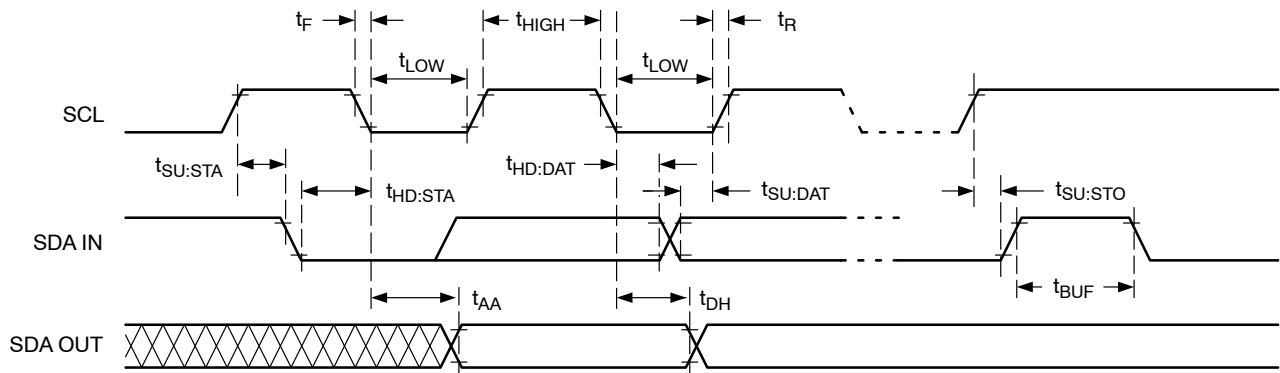


Figure 5. Bus Timing

WRITE OPERATIONS

Byte Write

To write data to memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the R/W bit set to '0'. The Master then sends two address bytes and a data byte and concludes the session by creating a STOP condition on the bus. The Slave responds with ACK after every byte sent by the Master (Figure 6). The STOP starts the internal Write cycle, and while this operation is in progress (t_{WR}), the SDA output is tri-stated and the Slave does not acknowledge the Master (Figure 7).

Page Write

The Byte Write operation can be expanded to Page Write, by sending more than one data byte to the Slave before issuing the STOP condition (Figure 8). Up to 32 distinct data bytes can be loaded into the internal Page Write Buffer starting at the address provided by the Master. The page address is latched, and as long as the Master keeps sending data, the internal byte address is incremented up to the end of page, where it then wraps around (within the page). New data can therefore replace data loaded earlier. Following the STOP, data loaded during the Page Write session will be written to memory in a single internal Write cycle (t_{WR}).

Acknowledge Polling

As soon (and as long) as internal Write is in progress, the Slave will not acknowledge the Master. This feature enables the Master to immediately follow-up with a new Read or Write request, rather than wait for the maximum specified Write time (t_{WR}) to elapse. Upon receiving a NoACK response from the Slave, the Master simply repeats the request until the Slave responds with ACK.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the Write operation. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the 1st data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the Slave will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The NV24C64LV is shipped erased, i.e., all bytes are FFh.

NV24C64LV

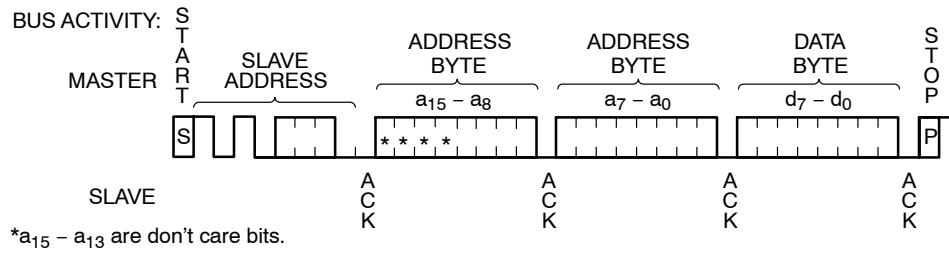


Figure 6. Byte Write Sequence

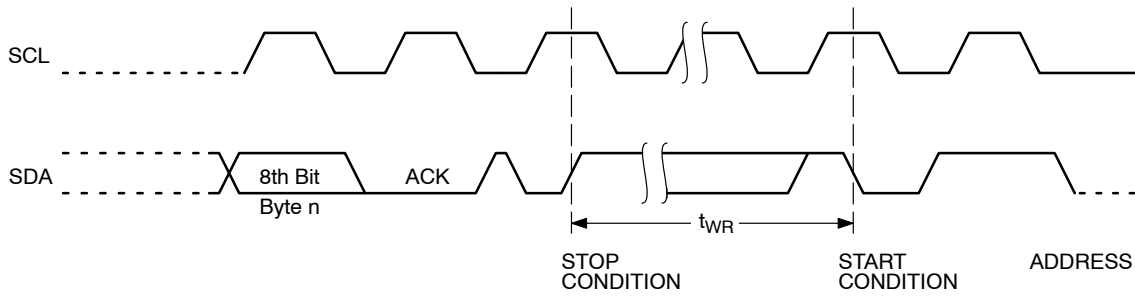


Figure 7. Write Cycle Timing

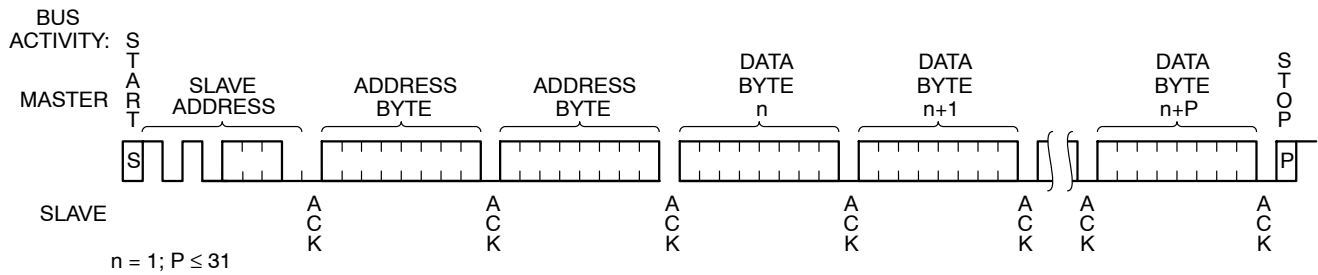


Figure 8. Page Write Sequence

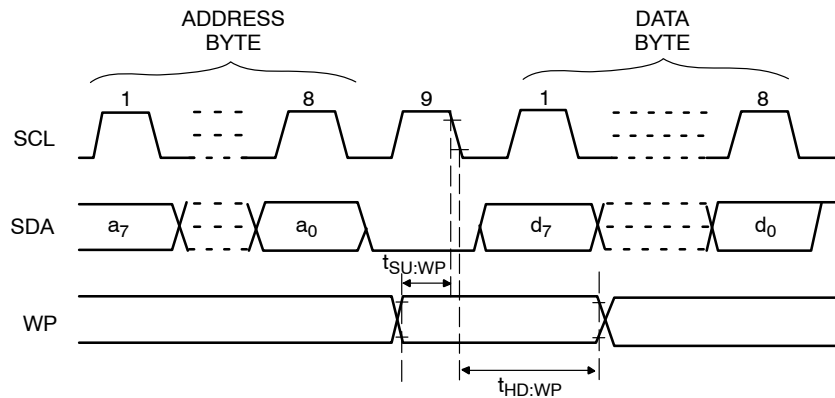


Figure 9. WP Timing

READ OPERATIONS

Immediate Read

To read data from memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the $R/\overline{W}$ bit set to '1'. The Slave responds with ACK and starts shifting out data residing at the current address. After receiving the data, the Master responds with NoACK and terminates the session by creating a STOP condition on the bus (Figure 10). The Slave then returns to Standby mode.

Selective Read

To read data residing at a specific address, the selected address must first be loaded into the internal address register. This is done by starting a Byte Write sequence, whereby the Master creates a START condition, then broadcasts a Slave address with the $R/\overline{W}$ bit set to '0' and then sends two address bytes to the Slave. Rather than completing the Byte

Write sequence by sending data, the Master then creates a START condition and broadcasts a Slave address with the $R/\overline{W}$ bit set to '1'. The Slave responds with ACK after every byte sent by the Master and then sends out data residing at the selected address. After receiving the data, the Master responds with NoACK and then terminates the session by creating a STOP condition on the bus (Figure 11).

Sequential Read

If, after receiving data sent by the Slave, the Master responds with ACK, then the Slave will continue transmitting until the Master responds with NoACK followed by STOP (Figure 12). During Sequential Read the internal byte address is automatically incremented up to the end of memory, where it then wraps around to the beginning of memory.

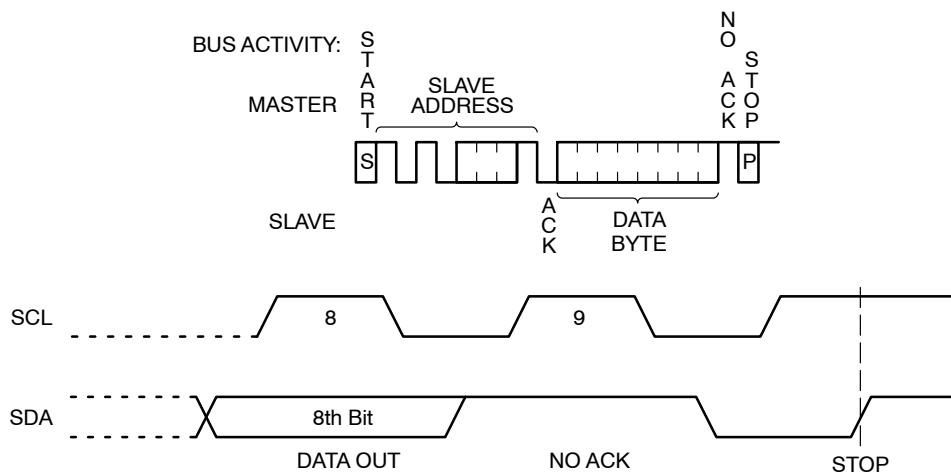


Figure 10. Immediate Read Sequence and Timing

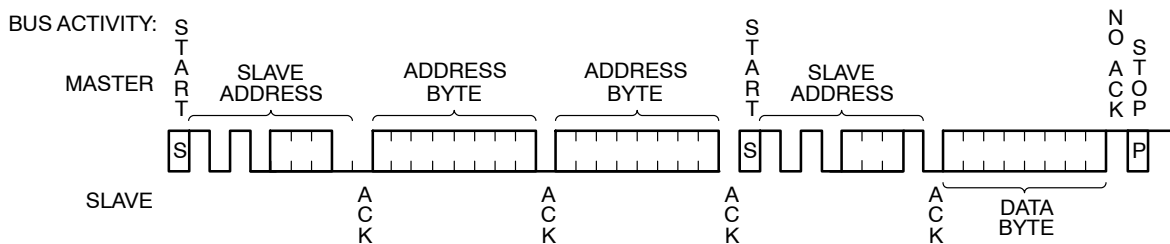


Figure 11. Selective Read Sequence

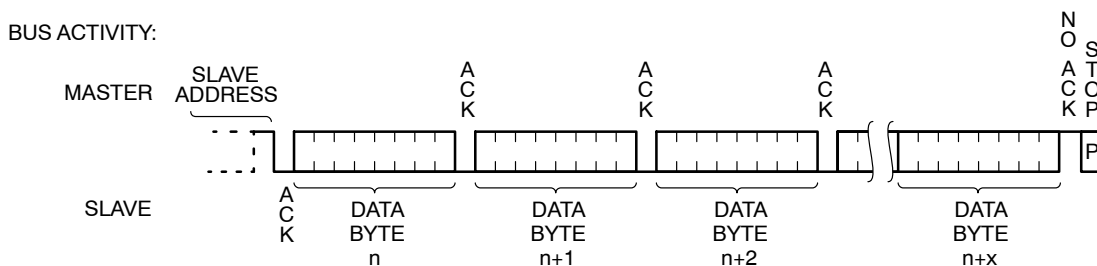


Figure 12. Sequential Read Sequence

NV24C64LV

ORDERING INFORMATION

Device Order Number	Density (Kb)	Package Type	Temperature Range	Shipping
NV24C64UVLT2G	64	US-8	V = Automotive Grade 1 (-40°C to +125°C)	Tape & Reel, 3,000 Units / Reel
NV24C64MUW3VLTBG	64	UDFN-8 Wettable Flank	V = Automotive Grade 1 (-40°C to +125°C)	Tape & Reel, 3,000 Units / Reel
NV24C64DWVLT3G	64	SOIC-8	V = Automotive Grade 1 (-40°C to +125°C)	Tape & Reel, 3,000 Units / Reel
NV24C64DTVLT3G	64	TSSOP-8	V = Automotive Grade 1 (-40°C to +125°C)	Tape & Reel, 3,000 Units / Reel

9. All packages are RoHS-compliant (Lead-free, Halogen-free).

10. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ON Semiconductor is licensed by the Philips Corporation to carry the I²C bus protocol.

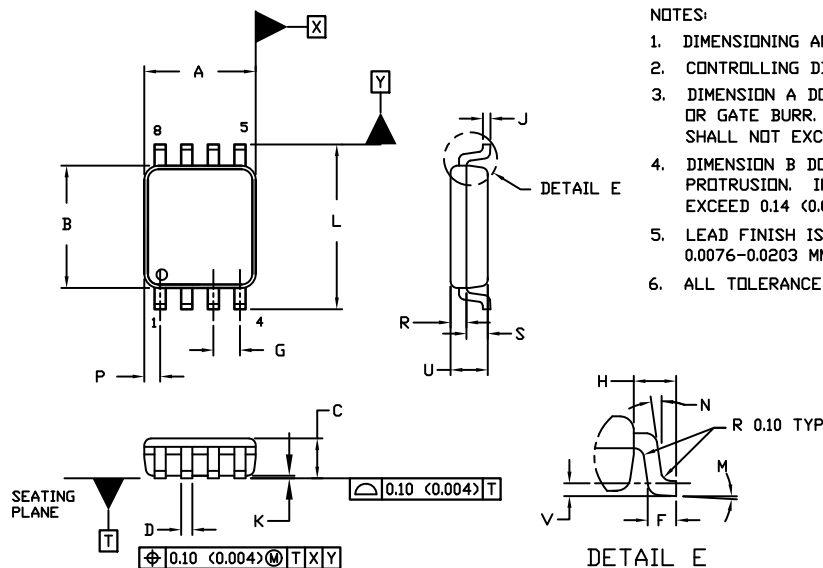
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

US8
CASE 493
ISSUE F

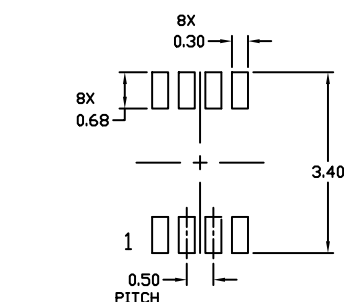
DATE 01 SEP 2021



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR. MOLD FLASH, PROTRUSION, OR GATE BURR SHALL NOT EXCEED 0.14 (0.0055") PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM (0.003-0.008").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 MM (0.002").

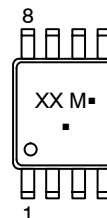
DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.25	0.118	0.128
M	0°	6°	0°	6°
N	0°	10°	0°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	



RECOMMENDED * MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the DFN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON04475D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	US8	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



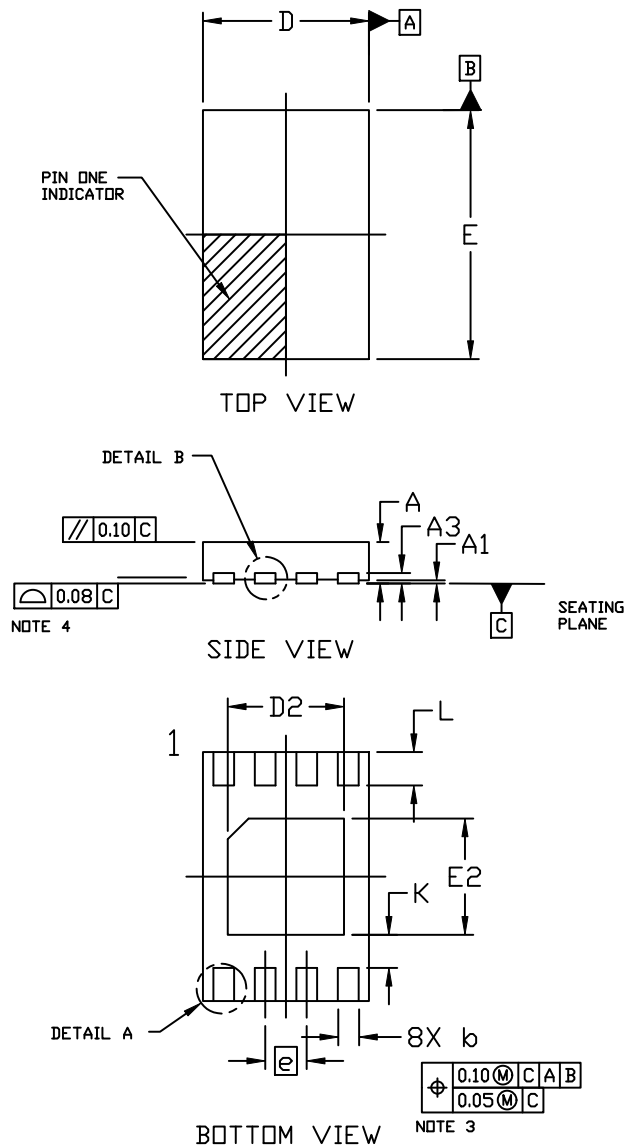
SCALE 2:1

UDFN8 2x3, 0.5P

CASE 517DH

ISSUE A

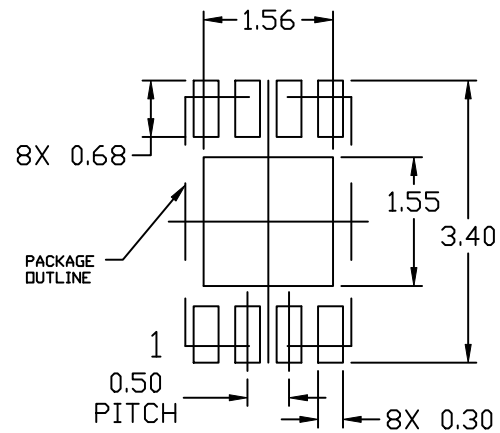
DATE 10 DEC 2020



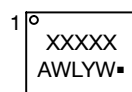
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
A1	0.00	---	0.05
A3	0.13 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.30	1.40	1.50
e	0.50 BSC		
K	0.40 REF		
L	0.30	0.40	0.50



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON06579G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	UDFN8 2X3, 0.5P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

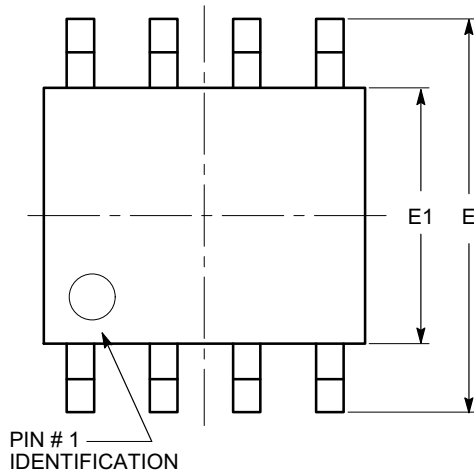
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



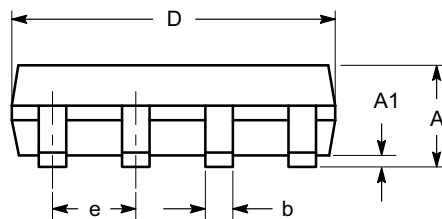
SOIC-8, 150 mils
CASE 751BD
ISSUE O

DATE 19 DEC 2008

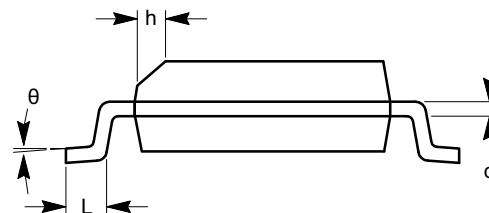


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



END VIEW

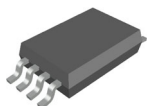
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

DOCUMENT NUMBER:	98AON34272E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC 8, 150 MILS	PAGE 1 OF 1

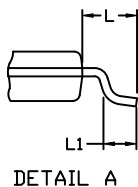
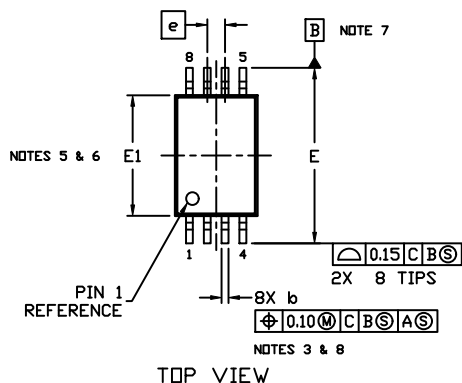
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



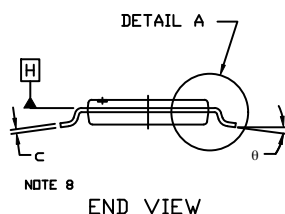
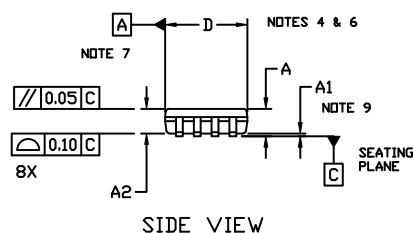
TSSOP8, 4.4x3.0, 0.65P CASE 948AL ISSUE A

DATE 20 MAY 2022



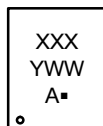
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009..
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL NOT BE 0.15 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
5. DIMENSION $E1$ DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND $E1$ ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM PLANE H.
7. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
8. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP..
9. A1 IS DEFINED AS THE LOWEST VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY..



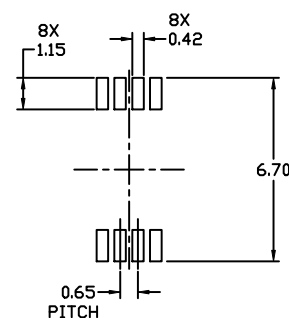
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.80	0.90	1.05
b	0.19	---	0.30
c	0.09	---	0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.70
θ	0°	---	8°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
 Y = Year
 WW = Work Week
 A = Assembly Location
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON34428E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP8, 4.4X3.0, 0.65P	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative