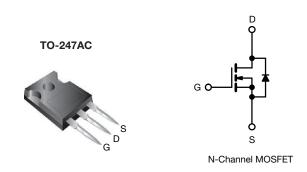


Power MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	V _{DS} (V) 600			
$R_{DS(on)}(\Omega)$	$V_{GS} = 10 \text{ V}$	0.60		
Q _g (max.) (nC)	140			
Q _{gs} (nC)	20			
Q _{gd} (nC)	69			
Configuration	Single			

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- · Isolated central mounting hole
- Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFPC50PbF

ABSOLUTE MAXIMUM RATINGS ($T_{\rm C}$	= 25 °C, unl	ess otherwis	se noted)		
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V _{DS}	600	V
Gate-source voltage			V_{GS}	± 20	v
Continuous drain current	V at 10 V	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$	L	11	
Continuous drain current	V _{GS} at 10 V	T _C = 100 °C	I _D	7.0	Α
Pulsed drain current ^a			I _{DM}	44	
Linear derating factor				1.4	W/°C
Single pulse avalanche energy b			E _{AS}	920	mJ
Repetitive avalanche current a			I _{AR}	10	Α
Repetitive avalanche energy a			E _{AR}	18	mJ
Maximum power dissipation	T _C = 25 °C		P_{D}	180	W
Peak diode recovery dV/dt ^c			dV/dt	3.0	V/ns
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) for 10 s				300 ^d	
Mounting torque 6-32 or M3 screw			10	lbf ⋅ in	
Mounting torque	0-32 OF IVIS	0-32 OF IVIS SCIEW		1.1	N⋅m

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 13 mH, R_g = 25 Ω , I_{AS} = 11 A (see fig. 12)
- c. $I_{SD} \le 11$ A, $dI/dt \le 100$ A/µs, $V_{DD} \le V_{DS}$, $T_{J} \le 150$ °C
- d. 1.6 mm from case



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THERMAL RESISTANCE					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	-	40	
Case-to-sink, flat, greased surface	R _{thCS}	-	0.24	-	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	-	0.65	

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D =$	= 250 μA	600	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference to	25 °C, I _D = 1 mA	-	0.78	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D}$	= 250 μΑ	2.0	-	4.0	V
Gate-source leakage	I _{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
7		$V_{DS} = 600 \text{ V}, \text{ V}$	$V_{GS} = 0 \text{ V}$	-	-	100	
Zero gate voltage drain current	I _{DSS}	$V_{DS} = 480 \text{ V}, \text{ V}$	V _{GS} = 0 V, T _J = 125 °C	-	-	500	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 6.0 A ^b	-	-	0.60	Ω
Forward transconductance	9 _{fs}	V _{DS} = 100 V, I	_D = 6.0 A ^b	5.7	-	-	S
Dynamic							
Input capacitance	C _{iss}	$V_{GS} = 0 V$		-	2700	-	
Output capacitance	C _{oss}	$V_{DS} = 25 \text{ V},$		-	300	-	рF
Reverse transfer capacitance	C _{rss}	f = 1.0 MHz, s	ee fig. 5	-	61	-	
Output capacitance	Q _g	V _{GS} = 10 V	-	-	140		
	Q_{gs}		-	-	20	nC	
Effective output capacitance	Q _{gd}	. See lig. 6 and 13 -		-	-	69	
Total gate charge	t _{d(on)}	$V_{DD} = 300 \text{ V}, I_{D} = 11 \text{ A},$ $R_{g} = 6.2 \Omega, R_{D} = 30 \Omega, \text{ see fig. } 10^{\text{ b}}$		-	18	-	ns
Gate-source charge	t _r			-	37	-	
Gate-drain charge	t _{d(off)}			-	88	-	
Turn-on delay time	t _f		1		36	-	
Internal drain inductance	L _D	Between lead		-	5.0	-	
Internal source inductance	L _S	6 mm (0.25") from package and center of die contact		-	13	-	nH
Drain-Source Body Diode Characteristic	cs						
Continuous source-drain diode current	I _S	MOSFET sym	bol	-	-	11	
Pulsed diode forward current ^a	I _{SM}	showing the integral revers p - n junction		-	-	44	А
Body diode voltage	V_{SD}	T _J = 25 °C, I _S	= 11 A, V _{GS} = 0 V ^b	-	-	1.4	V
Body diode reverse recovery time	t _{rr}	T 05 %C 1	44 A -11/-14 400 A / - b	-	550	830	ns
Body diode reverse recovery charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 11 \text{A}, \text{dI/dt} = 100 \text{A/}\mu\text{s}^{\text{b}}$		-	3.9	5.9	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)			<u> </u>		

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 μ s; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

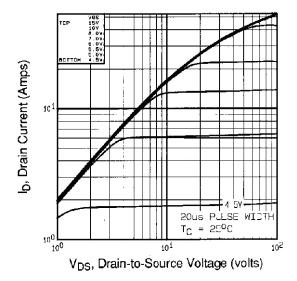


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

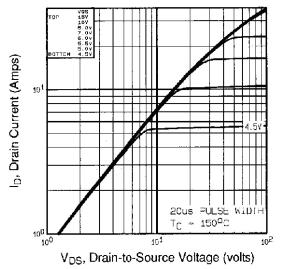


Fig. 2 - Typical Output Characteristics, T_C = 150 $^{\circ}$ C

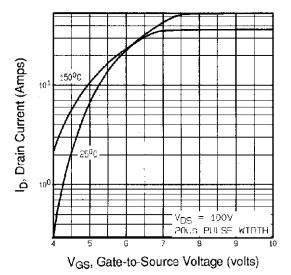


Fig. 3 - Typical Transfer Characteristics

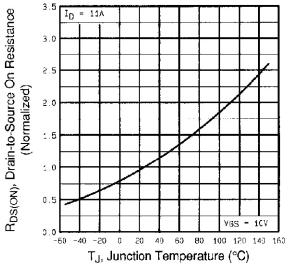


Fig. 4 - Normalized On-Resistance vs. Temperature



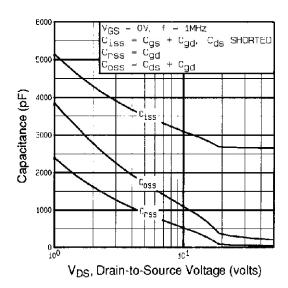


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

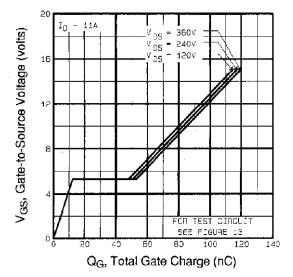


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

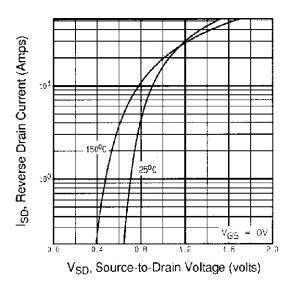


Fig. 7 - Typical Source-Drain Diode Forward Voltage

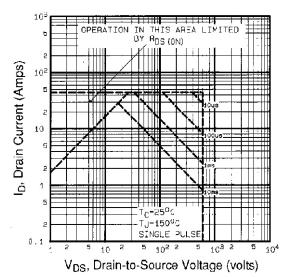


Fig. 8 - Maximum Safe Operating Area



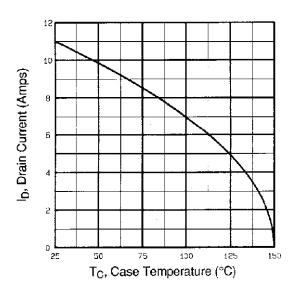


Fig. 9 - Maximum Drain Current vs. Case Temperature

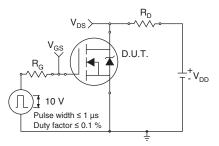


Fig. 10 - Switching Time Test Circuit

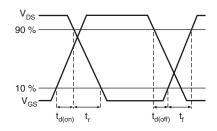


Fig. 11 - Switching Time Waveforms

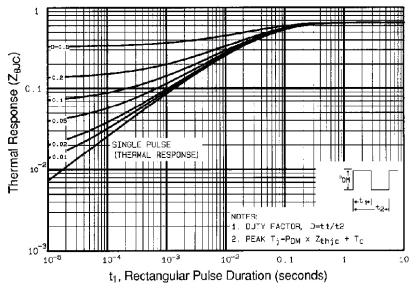


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



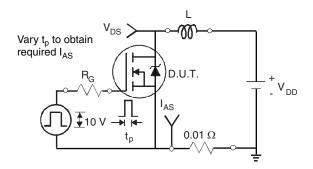


Fig. 13 - Unclamped Inductive Test Circuit

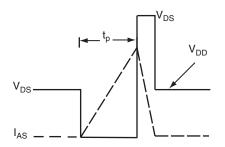


Fig. 14 - Unclamped Inductive Waveforms

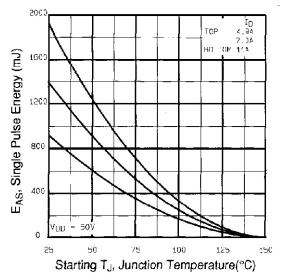


Fig. 15 - Maximum Avalanche Energy vs. Drain Current

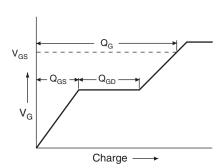


Fig. 16 - Basic Gate Charge Waveform

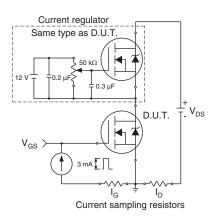
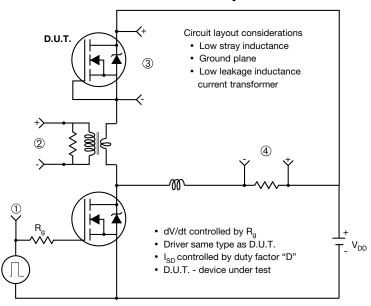


Fig. 17 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



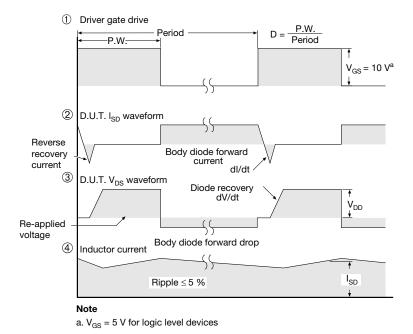


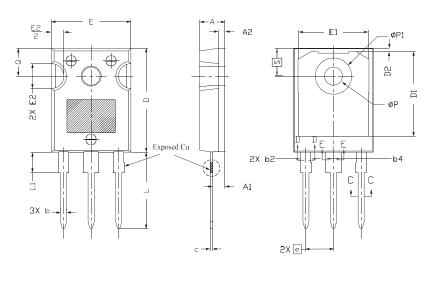
Fig. 18 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91243.



TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9







Section C--C,D-D,E-E

	MILLIMETERS				
DIM.	MIN.	NOM.	MAX.	NOTES	
Α	4.83	5.02	5.21		
A1	2.29	2.41	2.55		
A2	1.17	1.27	1.37		
b	1.12	1.20	1.33		
b1	1.12	1.20	1.28		
b2	1.91	2.00	2.39	6	
b3	1.91	2.00	2.34		
b4	2.87	3.00	3.22	6, 8	
b5	2.87	3.00	3.18		
С	0.40	0.50	0.60	6	
c1	0.40	0.50	0.56		
D	20.40	20.55	20.70	4	

	MILLIMETERS				
DIM.	MIN.	NOM.	MAX.	NOTES	
D1	16.46	16.76	17.06	5	
D2	0.56	0.66	0.76		
Е	15.50	15.70	15.87	4	
E1	13.46	14.02	14.16	5	
E2	4.52	4.91	5.49	3	
е		5.46 BSC			
L	14.90	15.15	15.40		
L1	3.96	4.06	4.16	6	
ØΡ	3.56	3.61	3.65	7	
Ø P1	7.19 ref.				
Q	5.31	5.50	5.69		
S	5.51 BSC				

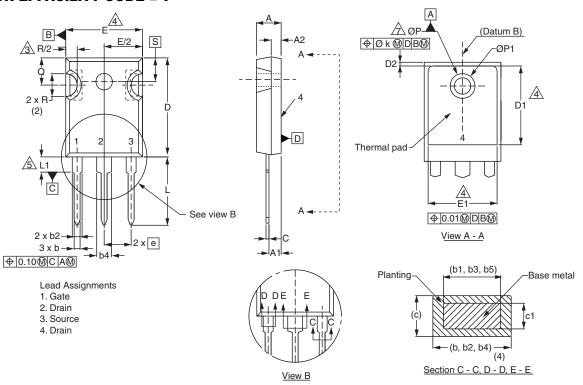
- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- $^{(7)}$ Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



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VERSION 2: FACILITY CODE = Y



	MILLIM		
DIM.	MIN.	MAX.	NOTES
Α	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
С	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

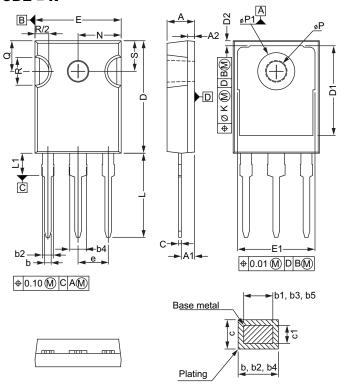
	MILLIN		
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
Е	15.29	15.87	
E1	13.72	-	
е	5.46	BSC	
Øk	0.2	254	
L	14.20	16.25	
L1	3.71	4.29	
ØР	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c

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VERSION 3: FACILITY CODE = N



	MILLIMETERS		
DIM.	MIN.	MAX.	
Α	4.65	5.31	
A1	2.21	2.59	
A2	1.17	1.37	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.65	2.39	
b3	1.65	2.34	
b4	2.59	3.43	
b5	2.59	3.38	
С	0.38	0.89	
c1	0.38	0.84	
D	19.71	20.70	
D1	13.08	-	

	MILLIMETERS		
DIM.	MIN.	MAX.	
D2	0.51	1.35	
E	15.29	15.87	
E1	13.46	-	
е	5.46 BSC		
k	0.254		
L	14.20	16.10	
L1	3.71	4.29	
N	7.62	BSC	
Р	3.56	3.66	
P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

ECN: E22-0452-Rev. G, 31-Oct-2022

DWG: 5971

- ⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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Vishay

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