NHD-3.12-25664UCB2

Graphic OLED Display Module

NHD-	Newhaven Display
3.12-	3.12” Diagonal Size
25664-	256 x 64 Pixel Resolution
UC-	Model
B-	Emitting Color: Blue

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Document Revision History

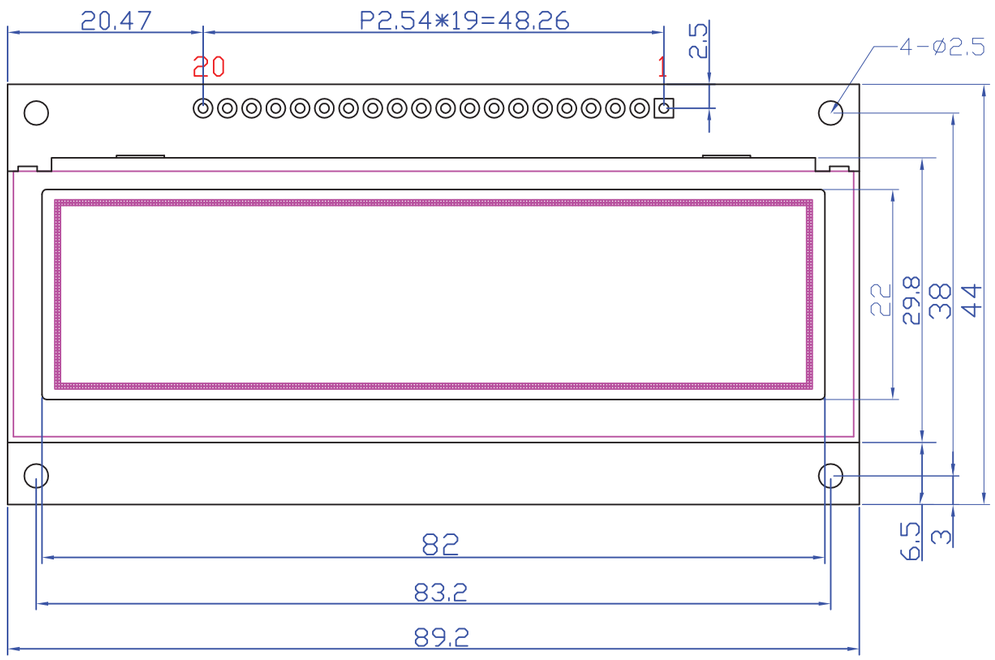
Revision	Date	Description	Changed by
0	5/1/2011	Initial Product Release	-
1	2/22/2013	Electrical characteristics and mechanical drawing updated	JN
2	5/2/16	Supply Current Updated	SB
3	8/23/19	Electrical Characteristics & Mechanical Drawing Updated	SB
4	8/4/20	Updated Pixel Memory Mapping Figure	AS

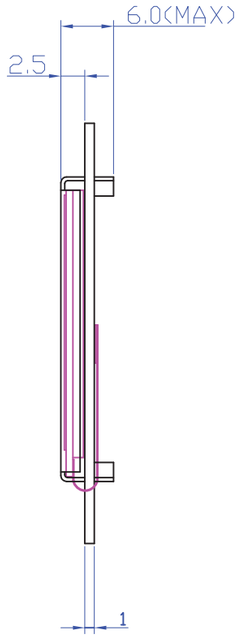
Functions and Features

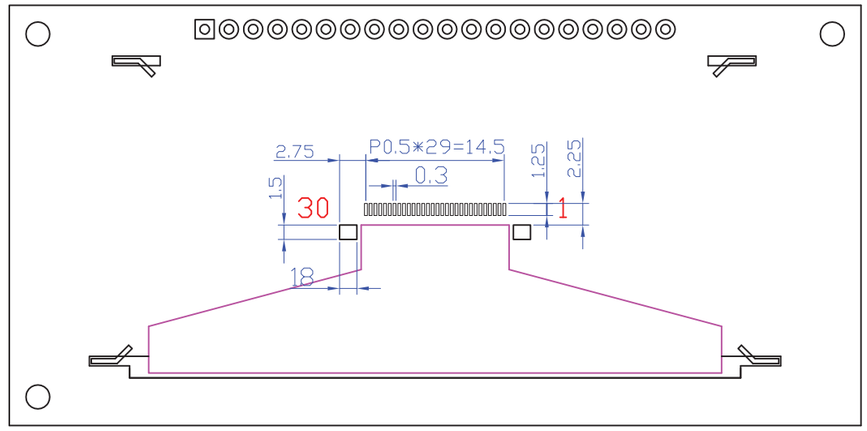
- **256 x 64 Pixel resolution**
- **Built-in SSD1322 controller**
- **Parallel or serial MPU interface**
- **Single, low voltage power supply**
- **RoHS compliant**

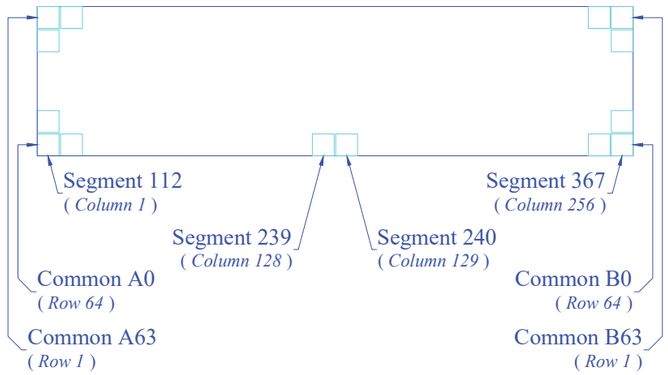
2D Mechanical Drawing

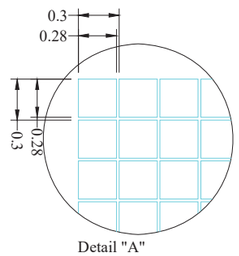
SYMBOL	REVISION	DATE











Pin Assignment

Pin No.	Symbol
1	VSS
2	VDD
3	NC
4	D/C
5	R/W or /WR
6	E or /RD
7-14	DB0 – DB7
15	NC
16	/RES
17	/CS
18	NC
19	BS1
20	BS0

Notes:

1. Display Color: Blue
2. Supply: 3.0V
3. Driver IC: SSD1322
4. Interface: Parallel (8080 or 6800) or SPI (3 or 4 Wire)
5. Luminance: 80 cd/m²

STANDARD TOLERANCE:
(UNLESS OTHERWISE SPECIFIED)
LINEAR: ±0.3mm

NEWHAVEN DISPLAY INTERNATIONAL

DRAWING/PART NUMBER: NHD-3.12-25664UCB2
REVISION: 1.0
SIZE: A3
SCALE: NS

UNLESS OTHERWISE SPECIFIED:
- DIMENSIONS ARE IN MILLIMETERS
- THIRD ANGLE PROJECTION

DRAWN BY: A. Shah
APPROVED BY: A. Shah
DRAWN DATE: 8/4/20
APPROVED DATE: 8/4/20

DO NOT SCALE DRAWING
SHEET 1 OF 2

Interface Description

Parallel Interface:

Pin No.	Symbol	External Connection	Function Description
1	V_{SS}	Power Supply	Ground
2	V_{DD}	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	D/C	MPU	Register select signal. D/C=0: Command, D/C=1: Data
5	R/W or /WR	MPU	**6800-interface:** Read/Write select signal, R/W=1: Read; R/W: =0: Write **8080-interface:** Active LOW Write signal.
6	E or /RD	MPU	**6800-interface:** Operation enable signal. Falling edge triggered. **8080-interface:** Active LOW Read signal.
7-14	DB0 – DB7	MPU	8-bit Bi-directional data bus lines.
15	NC	-	No Connect
16	/RES	MPU	Active LOW Reset signal.
17	/CS	MPU	Active LOW Chip Select signal.
18	NC	-	No Connect
19	BS1	MPU	MPU Interface Select signal.
20	BS0	MPU	MPU Interface Select signal.

Serial Interface:

Pin No.	Symbol	External Connection	Function Description
1	V_{SS}	Power Supply	Ground
2	V_{DD}	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	D/C	MPU	Register select signal. D/C=0: Command, D/C=1: Data Tie LOW for 3-wire Serial Interface.
5-6	VSS	Power Supply	Ground
7	SCLK	MPU	Serial Clock signal.
8	SDIN	MPU	Serial Data Input signal.
9	NC	-	No Connect
10-14	VSS	Power Supply	Ground
15	NC	-	No Connect
16	/RES	MPU	Active LOW Reset signal.
17	/CS	MPU	Active LOW Chip Select signal.
18	NC	-	No Connect
19	BS1	MPU	MPU Interface Select signal.
20	BS0	MPU	MPU Interface Select signal.

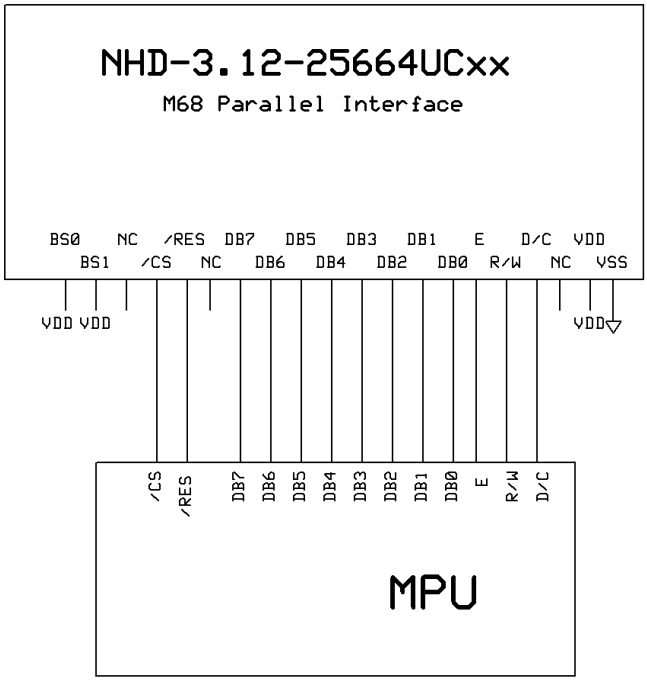
MPU Interface Pin Selections

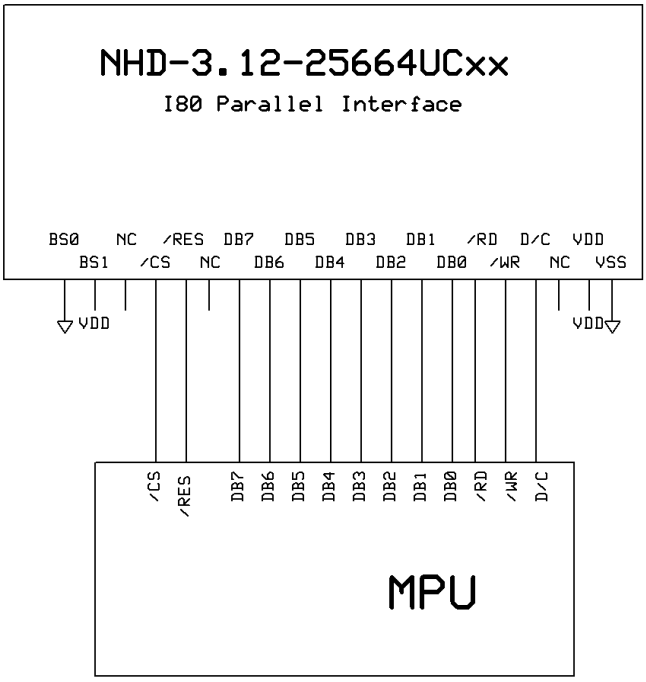
Pin Name	6800 Parallel 8-bit interface	8080 Parallel 8-bit interface	3-wire Serial Interface	4-wire Serial Interface
BS1	1	1	0	0
BS0	1	0	1	0

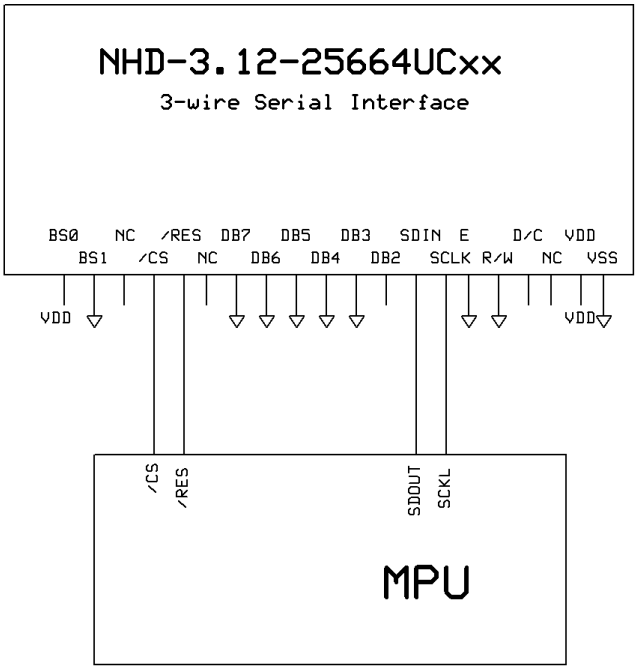
MPU Interface Pin Assignment Summery

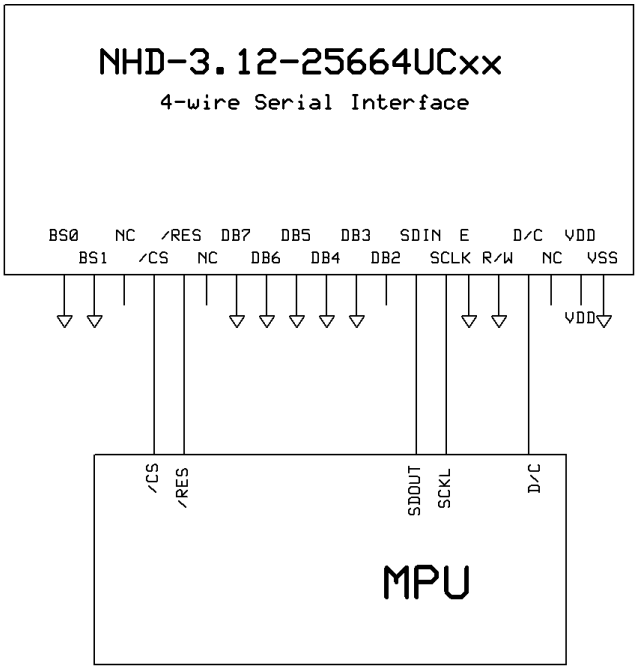
Bus Interface	Data/Command Interface								Control Signals				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	/CS	D/C	/RES
8-bit 6800	D[7:0]								E	R/W	/CS	D/C	/RES
8-bit 8080	D[7:0]								/RD	/WR	/CS	D/C	/RES
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		/CS	Tie LOW	/RES
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		/CS	D/C	/RES

Wiring Diagrams









Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T_{OP}	Absolute Max	-40	-	+85	°C
Storage Temperature Range	T_{ST}	Absolute Max	-40	-	+90	°C
Supply Voltage	V_{DD}	-	2.8	3.0	3.3	V
Supply Current (logic)	I_{DD}	T_{OP}=25°C, V_{DD}=3.0V	1	5	6	mA
Supply Current (display)	I_{CC}	50% ON, V_{DD}=3.0V	100	155	165	mA
		100% ON, V_{DD}=3.0V	150	250	265	mA
Sleep Mode Current	$I_{DD}+I_{CC\_SLEEP}$	-	-	-	110	µA
"H" Level input	V_{IH}	-	0.8 * V_{DD}	-	V_{DD}	V
"L" Level input	V_{IL}	-	V_{SS}	-	0.2 * V_{DD}	V
"H" Level output	V_{OH}	-	0.9 * V_{DD}	-	V_{DD}	V
"L" Level output	V_{OL}	-	V_{SS}	-	0.1 * V_{DD}	V

Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Optimal Viewing Angles	Top	φY+		80	-	-	º
	Bottom	φY-		80	-	-	º
	Left	θX-		80	-	-	º
	Right	θX+		80	-	-	º
Contrast Ratio		CR	-	2000:1	-	-	-
Response Time	Rise	T_R	-	-	10	-	us
	Fall	T_F	-	-	10	-	us
Brightness[2]		L_V	T_{OP}=25°C 50% Checkerboard	60	80	-	cd/m^2
Lifetime[1]		-		10,000	-	-	Hrs.

Note:

1) Lifetime at typical temperature is based on accelerated high-temperature operation. Lifetime is tested at average 50% pixels on and is rated as hours until half-brightness. The Display OFF command can be used to extend the lifetime of the display.

2) Luminance of active pixels will degrade faster than inactive pixels. Residual (burn-in) images may occur. To avoid this, every pixel should be illuminated uniformly. Using a screensaver is highly recommended.

Built-in SSD1322 controller
Instruction Table

Instruction	Code										Description	RESET value
	D/C	HEX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Enable Grayscale Table	0	**00**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	Enable the Grayscale table settings. (see command 0xB8)	
Set Column Address	0 1 1	**15** **A[6:0]** **B[6:0]**	**0** * *	**0** **A6** **B6**	**0** **A5** **B5**	**1** **A4** **B4**	**0** **A3** **B3**	**1** **A2** **B2**	**0** **A1** **B1**	**1** **A0** **B0**	Set column start and end address A[6:0]: Column start address. Range: 0-119d B[6:0]: Column end address. Range: 0-119d	 0 119d
Write RAM Command	0	**5C**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	Enable MCU to write Data into RAM	
Read RAM Command	0	**5D**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**1**	Enable MCU to read Data from RAM	
Set Row Address	0 1 1	**75** **A[6:0]** **B[6:0]**	**0** * *	**1** **A6** **B6**	**1** **A5** **B5**	**1** **A4** **B4**	**0** **A3** **B3**	**1** **A2** **B2**	**0** **A1** **B1**	**1** **A0** **B0**	Set row start and end address A[6:0]: Row start address. Range: 0-127d B[6:0]: Row end address. Range: 0-127d	 0 127d
Set Remap	0 1 1	**A0** **A[5:0]** **B[4]**	**1** **0** *	**0** **0** *	**1** **A5** **0**	**0** **A4** **B4**	**0** **0** **0**	**0** **A2** **0**	**0** **A1** **0**	**0** **A0** **1**	A[0] = 0; Horizontal Address Increment A[0] = 1; Vertical Address Increment A[1] = 0; Disable Column Address remap A[1] = 1; Enable Column Address remap A[2] = 0; Disable Nibble remap A[2] = 1; Enable Nibble remap A[4] = 0; Scan from COM0 to COM[N-1] A[4] = 1; Scan from COM[N-1] to COM0 A[5] = 0; Disable COM split Odd/Even A[5] = 1; Enable COM split Odd/Even B[4] = 0; Disable Dual COM mode B[4] = 1; Enable Dual COM mode Note: A[5] must be 0 if B[4] is 1.	0 0 0 0 0 0
Set Display Start Line	0 1	**A1** **A[6:0]**	**1** *	**0** **A6**	**1** **A5**	**0** **A4**	**0** **A3**	**0** **A2**	**0** **A1**	**1** **A0**	Set display RAM display start line register from 0-127.	0
Set Display Offset	0 1	**A2** **A[6:0]**	**1** *	**0** **A6**	**1** **A5**	**0** **A4**	**0** **A3**	**0** **A2**	**1** **A1**	**0** **A0**	Set vertical shift by COM from 0~127.	0
Display Mode	0	**A4/A7**	**1**	**0**	**1**	**0**	**0**	**X2**	**X1**	**X0**	0xA4 = Entire display OFF 0xA5 = Entire display ON, all pixels Grayscale level 15 0xA6 = Normal display 0xA7 = Inverse display	0xA6
Enable Partial Display	0 1 1	**A8** **A[6:0]** **B[6:0]**	**1** **0** **0**	**0** **A6** **B6**	**1** **A5** **B5**	**0** **A4** **B4**	**1** **A3** **B3**	**0** **A2** **B2**	**0** **A1** **B1**	**0** **A0** **B0**	Turns ON partial mode. A[6:0] = Address of start row B[6:0] = Address of end row (B[6:0] > A[6:0])	

Exit Partial Display	0	**A9**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	Exit Partial Display mode	
Function Selection	0 1	**AB** **A[0]**	**1** **0**	**0** **0**	**1** **0**	**0** **0**	**1** **0**	**0** **0**	**1** **0**	**1** **A0**	A[0] = 0; External VDD A[0] = 1; Internal VDD regulator	 1
Set Sleep Mode ON/OFF	0	**AE~AF**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**X0**	0xAE = Sleep Mode ON (display OFF) 0xAF = Sleep Mode OFF (display ON)	
Set Phase Length	0 1	**B1** **A[7:0]**	**1** **A7**	**0** **A6**	**1** **A5**	**1** **A4**	**0** **A3**	**0** **A2**	**0** **A1**	**1** **A0**	A[3:0] = P1. Phase 1 period of 5-31 DCLK clocks A[7:4] = P2. Phase 2 period of 3-15 DCLK clocks	9 7
Set Display Clock Divide Ratio / Oscillator Frequency	0 1	**B3** **A[7:0]**	**1** **A7**	**0** **A6**	**1** **A5**	**1** **A4**	**0** **A3**	**0** **A2**	**1** **A1**	**1** **A0**	A[3:0] = 0000; divide by 1 A[3:0] = 0001; divide by 2 A[3:0] = 0010; divide by 4 A[3:0] = 0011; divide by 8 A[3:0] = 0100; divide by 16 A[3:0] = 0101; divide by 32 A[3:0] = 0110; divide by 64 A[3:0] = 0111; divide by 128 A[3:0] = 1000; divide by 256 A[3:0] = 1001; divide by 512 A[3:0] = 1010; divide by 1024 A[3:0] >= 1011; invalid A[7:4] = Set the Oscillator Frequency. Frequency increases with the value of A[7:4]. Range 0000b~1111b.	0 1100b
Set GPIO	0 1	**B5** **A[3:0]**	**1** *	**0** *	**1** *	**1** *	**0** **A3**	**1** **A2**	**0** **A1**	**1** **A0**	A[1:0] = 00; GPIO0 input disabled A[1:0] = 01; GPIO0 input enabled A[1:0] = 10; GPIO0 output LOW A[1:0] = 11; GPIO0 output HIGH A[3:2] = 00; GPIO1 input disabled A[3:2] = 01; GPIO1 input enabled A[3:2] = 10; GPIO1 output LOW A[3:2] = 11; GPIO1 output HIGH	 10b 10b
Set Second Precharge Period	0 1	**B6** **A[3:0]**	**1** *	**0** *	**1** *	**1** *	**0** **A3**	**1** **A2**	**1** **A1**	**0** **A0**	Sets the second precharge period A[3:0] = DCLKs	1000b
Set Grayscale Table	0 1 1 1 1 1 1	**B8** **A1[7:0]** **A2[7:0]** **.** **.** **.** **A14[7:0]** **A15[7:0]**	**1** $A1_7$ $A2_7$ . . . $A14_7$ $A15_7$	**0** $A1_6$ $A2_6$ . . . $A14_6$ $A15_6$	**1** $A1_5$ $A2_5$ . . . $A14_5$ $A15_5$	**1** $A1_4$ $A2_4$ . . . $A14_4$ $A15_4$	**1** $A1_3$ $A2_3$ . . . $A14_3$ $A15_3$	**0** $A1_2$ $A2_2$ . . . $A14_2$ $A15_2$	**0** $A1_1$ $A2_1$ . . . $A14_1$ $A15_1$	**0** $A1_0$ $A2_0$ . . . $A14_0$ $A15_0$	Sets the gray scale pulse width in units of DCLK. Range 0-180d. A1[7:0] = Gamma Setting for GS1 A2[7:0] = Gamma Setting for GS2 . . . A14[7:0] = Gamma Setting for GS14 A15[7:0] = Gamma Setting for GS15 Note: 0 < GS1 < GS2 < GS3 … < GS14 < GS15 The setting must be followed by command 0x00.	
Select Default	0	**B9**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	Sets Linear Grayscale table	

Linear Gray Scale Table											GS0 pulse width = 0 GS0 pulse width = 0 GS0 pulse width = 8 GS0 pulse width = 16 . . . GS0 pulse width = 104 GS0 pulse width = 112	
Set Precharge Voltage	0 1	**BB** **A[4:0]**	**1** *	**0** *	**1** *	**1** **A4**	**1** **A3**	**0** **A2**	**1** **A1**	**1** **A0**	Set precharge voltage level. A[4:0] = 0x00; 0.20*VCC . . A[4:0] = 0x3E; 0.60*VCC	0x17
Set VCOMH Voltage	0 1	**BE** **A[3:0]**	**1** *	**0** *	**1** *	**1** *	**1** **A3**	**1** **A2**	**1** **A1**	**0** **A0**	Sets the VCOMH voltage level A[3:0] = 0x00; 0.72*VCC . . A[3:0] = 0x04; 0.8*VCC . . A[3:0] = 0x07; 0.86*VCC	0x04
Set Contrast Control	0 1	**C1** **A[7:0]**	**1** **A7**	**1** **A6**	**0** **A5**	**0** **A4**	**0** **A3**	**0** **A2**	**0** **A1**	**1** **A0**	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases.	0x7F
Master Contrast Control	0 1	**C7** **A[3:0]**	**1** *	**1** *	**0** *	**0** *	**0** **A3**	**1** **A2**	**1** **A1**	**1** **A0**	A[3:0] = 0x00; Reduce output for all colors to 1/16 A[3:0] = 0x01; Reduce output for all colors to 2/16 . . A[3:0] = 0x0E; Reduce output for all colors to 15/16 A[3:0] = 0x0F; no change	0x0f
Set Multiplex Ratio	0 1	**CA** **A[6:0]**	**1** *	**1** **A6**	**0** **A5**	**0** **A4**	**1** **A3**	**0** **A2**	**1** **A1**	**0** **A0**	Set MUX ratio to N+1 MUX N=A[6:0]; from 16MUX to 128MUX (0 to 14 are invalid)	127d
Set Command Lock	0 1	**FD** **A[2]**	**1** **0**	**1** **0**	**1** **0**	**1** **1**	**1** **0**	**1** **A2**	**0** **1**	**1** **0**	A[2] = 0; Unlock OLED to enable commands A[2] = 1; Lock OLED from entering commands	0x12

For detailed instruction information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1322.pdf

MPU Interface

For detailed timing information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1322.pdf

6800-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, R/W, D/C, E, and /CS.
A LOW on R/W indicates write operation, and HIGH on R/W indicates read operation.
A LOW on D/C indicates "Command" read or write, and HIGH on D/C indicates "Data" read or write.
The E input serves as data latch signal, while /CS is LOW. Data is latched at the falling edge of E signal.

Function	E	R/W	/CS	D/C
Write Command	↓	0	0	0
Read Status	↓	1	0	0
Write Data	↓	0	0	1
Read Data	↓	1	0	1

8080-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, /RD, /WR, D/C, and /CS.
A LOW on D/C indicates "Command" read or write, and HIGH on D/C indicates "Data" read or write.
A rising edge of /RS input serves as a data read latch signal while /CS is LOW.
A rising edge of /WR input serves as a data/command write latch signal while /CS is LOW.

Function	/RD	/WR	/CS	D/C
Write Command	1	↑	0	0
Read Status	↑	1	0	0
Write Data	1	↑	0	1
Read Data	↑	1	0	1

Alternatively, /RD and /WR can be kept stable while /CS serves as the data/command latch signal.

Function	/RD	/WR	/CS	D/C
Write Command	1	0	↑	0
Read Status	0	1	↑	0
Write Data	1	0	↑	1
Read Data	0	1	↑	1

Serial Interface (4-wire)

The 4-wire serial interface consists of serial clock SCLK, serial data SDIN, D/C, and /CS.
D0 acts as SCLK and D1 acts as SDIN. D2 should be left open. D3~D7, E, and R/W should be connected to GND.

Function	/RD	/WR	/CS	D/C	D0
Write Command	Tie LOW	Tie LOW	0	0	↑
Write Data	Tie LOW	Tie LOW	0	1	↑

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6,…D0.
D/C is sampled on every eighth clock and the data byte in the shift register is written to the GDRAM or command register in the same clock.
Note: Read is not available in serial mode.

Serial Interface (3-wire)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN, and /CS.
D0 acts as SCLK and D1 acts as SDIN. D2 should be left open. D3~D7, E, R/W, and D/C should be connected to GND.

Function	/RD	/WR	/CS	D/C	D0
Write Command	Tie LOW	Tie LOW	0	Tie LOW	↑
Write Data	Tie LOW	Tie LOW	0	Tie LOW	↑

SDIN is shifted into an 9-bit shift register on every rising edge of SCLK in the order of D/C, D7, D6,…D0.
D/C (first bit of the sequential data) will determine if the following data byte is written to the Display Data RAM (D/C = 1) or the command register (D/C = 0).
Note: Read is not available in serial mode.

For detailed protocol information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1322.pdf

Example Initialization Sequence:

```
Set_Command_Lock(0x12);                 // Unlock Basic Commands (0x12/0x16)
Set_Display_On_Off(0x00);               // Display Off (0x00/0x01)
Set_Column_Address(0x1C,0x5B);
Set_Row_Address(0x00,0x3F);
Set_Display_Clock(0x91);                // Set Clock as 80 Frames/Sec
Set_Multiplex_Ratio(0x3F);              // 1/64 Duty (0x0F~0x3F)
Set_Display_Offset(0x00);               // Shift Mapping RAM Counter (0x00~0x3F)
Set_Start_Line(0x00);                   // Set Mapping RAM Display Start Line (0x00~0x7F)
Set_Remap_Format(0x14);                 // Set Horizontal Address Increment
                                        //    Column Address 0 Mapped to SEG0
                                        //    Disable Nibble Remap
                                        //    Scan from COM[N-1] to COM0
                                        //    Disable COM Split Odd Even
                                        //    Enable Dual COM Line Mode
Set_GPIO(0x00);                         // Disable GPIO Pins Input
Set_Function_Selection(0x01);           // Enable Internal VDD Regulator
Set_Display_Enhancement_A(0xA0,0xFD);       // Enable External VSL
Set_Contrast_Current(0x9F);             // Set Segment Output Current
Set_Master_Current(0x0F);               // Set Scale Factor of Segment Output Current Control
//Set_Gray_Scale_Table();               // Set Pulse Width for Gray Scale Table
Set_Linear_Gray_Scale_Table();          //set default linear gray scale table
Set_Phase_Length(0xE2);                 // Set Phase 1 as 5 Clocks & Phase 2 as 14 Clocks
Set_Display_Enhancement_B(0x20);        // Enhance Driving Scheme Capability (0x00/0x20)
Set_Precharge_Voltage(0x1F);            // Set Pre-Charge Voltage Level as 0.60*VCC
Set_Precharge_Period(0x08);             // Set Second Pre-Charge Period as 8 Clocks
Set_VCOMH(0x07);                        // Set Common Pins Deselect Voltage Level as 0.86*VCC
Set_Display_Mode(0x02);                 // Normal Display Mode (0x00/0x01/0x02/0x03)
Set_Partial_Display(0x01,0x00,0x00);    // Disable Partial Display
Set_Display_On_Off(0x01);
```

Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Test the endurance of the display at high storage temperature.	+90°C, 240hrs	2
Low Temperature storage	Test the endurance of the display at low storage temperature.	-40°C, 240hrs	1,2
High Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature.	+85°C, 240hrs	2
Low Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at low temperature.	-40°C, 240hrs	1,2
High Temperature / Humidity Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature with high humidity.	+60°C, 90% RH, 240hrs	1,2
Thermal Shock resistance	Test the endurance of the display by applying electric stress (voltage & current) during a cycle of low and high temperatures.	-40°C,30min -> 25°C,5min -> 85°C,30min = 1 cycle 100 cycles	
Vibration test	Test the endurance of the display by applying vibration to simulate transportation and use.	10-22Hz, 15mm amplitude. 22-500Hz, 1.5G 30min in each of 3 directions X, Y, Z	3
Atmospheric Pressure test	Test the endurance of the display by applying atmospheric pressure to simulate transportation by air.	115mbar, 40hrs	3
Static electricity test	Test the endurance of the display by applying electric static discharge.	VS=800V, RS=1.5kΩ, CS=100pF One time	

Note 1: No condensation to be observed.
Note 2: Conducted after 2 hours of storage at 25°C, 0%RH.
Note 3: Test performed on product itself, not inside a container.
Evaluation Criteria:
1: Display is fully functional during operational tests and after all tests, at room temperature.
2: No observable defects.
3: Luminance >50% of initial value.
4: Current consumption within 50% of initial value

Precautions for using OLEDs/LCDs/LCMs

See Precautions at www.newhavendisplay.com/specs/precautions.pdf

Warranty Information and Terms & Conditions

http://www.newhavendisplay.com/index.php?main_page=terms