TFT DISPLAY SPECIFICATION

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RFE430W-EYW-DSG

SPECIFICATION

CUSTOMER:

APPROVED BY	
PCB VERSION	
DATE	

FOR CUSTOMER USE ONLY

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

Release DATE:

TFT Display Inspection Specification: https://www.raystar-optronics.com/download/products.htm
Precaution in use of TFT module: https://www.raystar-optronics.com/download/declaration.htm

Revision History

VERSION	DATE	REVISED PAGE NO.	Note
0 A B	2021/12/16 2022/02/23 2022/04/18		First issue Modify Initial Code Modify Contour Drawing

Contents

1.Module Classification Information

R	F	E	43	0W	-	E	Y	W	-	D	S	G
1	2	3	4	5	-	6	7	8	-	9	10	11

Item	Description		
1	R：Raystar Optronics Inc.		
2	Display Type：F→TFT Type, J→ Custom TFT		
3	Solution: A: 128x160 B:320x234 C:320x240 D:480x234 E:480x272 F:800x480 G:640x480 H:1024x600 I:320x480 J:240x320 K:1280x800 L:240x400 M:1024x768 N:128x128 O:480x800 P:640x320 Q:800x600 S:480x128 T:800x320 Y: 1920 x 720		
4	Display Size：4.3” TFT		
5	Version Code.		
6	Model Type: A：TFT LCD E：TFT+FR+CONTROL BOARD J：TFT+FR+A/D BOARD N：TFT+FR+A/D BOARD+CONTROL BOARD S：TFT+FR+POWER BOARD (DC TO DC) 1：TFT+CONTROL BOARD	6：TFT+FR H：TFT+D/V BOARD I：TFT+FR+D/V BOARD B：TFT+POWER BD	
7	Polarizer Type, Temperature range, View direction	I→Transmissive, W. T, 6:00 ; C→Transmissive, N. T, 6:00 L→Transmissive, W.T,12:00 ; F→Transmissive, N.T,12:00 Y→Transmissive,W.T, IPS TFT ; W→Transmissive, Super W.T, IPS TFT A→Transmissive, N.T, IPS TFT Z→Transmissive, W.T, O-TFT R→Transmissive, Super W.T, O-TFT N→Transmissive, Super W.T, 6:00; Q→Transmissive, Super W.T, 12:00 V→Transmissive, Super W.T, VA TFT	
8	Backlight	W：LED, White	H：LED, High Light White
		F：CCFL, White	
9	Driver Method	D: Digital A: Analog L：LVDS M:MIPI	
10	Interface	N：without control board A：8Bit B：16Bit S:SPI Interface R: RS232 U:USB I: I2C	
11	TS	N：Without TS S：resistive touch panel C：capacitive touch panel capacitive touch panel (G-F-F) G：capacitive touch panel(G-G)	

2.Summary

TFT 4.3” is a IPS transmissive type color active matrix TFT liquid crystal display that use amorphous silicon TFT as switching devices. This module is a composed of a TFT_LCD module, It is usually designed for industrial application and this module follows RoHs,

3.General Specifications

- Size: 4.3 inch
- Dot Matrix: 480 x RGBx272(TFT) dots
- Module dimension: 123.5 (W) x 67.2 (H) x 14.73(D)(MAX) mm
- Active area: 95.04 x 53.856 mm
- Pixel pitch: 0.198(H) x 0.198(V) mm
- LCD type: TFT, Normally Black, Transmissive
- Viewing Angle: 80/80/80/80
- Aspect Ratio: 16:9
- Backlight Type: LED,Normally White
- TFT Controller IC: BT815
- TFT Interface: SPI/QSPI
- CTP FW Version: 0x07.0x00.0x00.0x00.0x01.0x0C.0x11.0x43
- CTP IC: ILI2130 or equivalent
- CTP Interface: I2C
- CTP Resolution: 16384*16384
- With /Without TP: With CTP
- Surface: Glare

*Color tone slight changed by temperature and driving voltage

4.Interface

4.1. LCM PIN Definition (CON 5)

Pin	Symbol	I/O	Function
1	VDD	P	3.3V power supply input
2	GND	P	Ground
3	SCK	I	SPI clock input
4	MISO	O	SPI Single mode: SPI MISO output SPI Dual/Quad mode: SPI data line 1
5	MOSI	I	SPI Single mode: SPI MOSI input SPI Dual/Quad mode: SPI data line 0
6	CS	I	SPI slave select input
7	INT	OD/O	Interrupt to host, open drain output(default) or push-pull output, active low
8	PD_N	I	Chip power down mode control input, active low. Connect to MCU GPIO for power management or hardware reset function
9	GPIO2	I/O	General purpose IO 2
10	GPIO3	I/O	General purpose IO 3
11	IO2	I/O	SPI Single/Dual mode: General purpose IO 0 SPI Quad mode: SPI data line 2
12	IO3	I/O	SPI Single/Dual mode: General purpose IO 1 SPI Quad mode: SPI data line 3
13	CSCL	I	Connect to I2C SCL pin of the CTP(ILI2130)
14	CSDA	I/O	Connect to I2C SDA pin of the CTP(ILI2130)
15	CRST	I	Connect to reset pin of the CTP(ILI2130)
16	CINT	O	Connect to interrupt pin of the CTP(ILI2130)
17	VLED	P	5V power supply input
18	VLED	P	5V power supply input
19	GND	P	Ground
20	GND	P	Ground

4.2. QSPI Interface

The QSPI slave interface operates up to 30MHz. Only SPI mode 0 is supported.
The QSPI can be configured as a SPI slave in SINGLE, DUAL or QUAD channel modes.
By default the SPI slave operates in the SINGLE channel mode with MOSI as input from the master and MISO as output to the master. DUAL and QUAD channel modes can be configured through the SPI slave itself. To change the channel modes, write to register REG_SPI_WIDTH. The table below depicts the setting.

REG_SPI_WIDTH[1:0]	Channel Mode	Data pins	Max bus speed
00	SINGLE – default mode	MISO, MOSI	30 MHz
01	DUAL	MOSI, MISO	30 MHz
10	QUAD	MOSI, MISO, IO2, IO3	30 MHz
11	Reserved	-	-

Table 1 QSPI Channel Selection

With DUAL/QUAD channel modes, the SPI data ports are now unidirectional. In these modes, each SPI transaction (signified by CS going active low) will begin with the data ports set as inputs.
Hence, for writing to the BT815/6, the protocol will operate as in FT800, with “WR-Command/Addr2, Addr1, Addr0, DataX, DataY, DataZ …” The write operation is considered complete when CS goes inactive high.
For reading from the BT815/6, the protocol will still operate as in FT800, with “RD-Command/Addr2, Addr1, Addr0, Dummy-Byte, DataX, DataY, DataZ”. However as the data ports are now unidirectional, a change of port direction will occur before DataX is clocked out of the BT815/6. Therefore it is important that the firmware controlling the SPI master changes the SPI master data port direction to “input” after transmitting Addr0. The BT815/6 will not change the port direction till it starts to clock out DataX. Hence, the Dummy-Byte cycles will be used as a change-over period when neither the SPI master nor slave will be driving the bus; the data paths thus must have pull-ups/pull-downs. The SPI slave from the BT815/6 will reset all its data ports’ direction to input once CS goes inactive high (i.e. at the end of the current SPI master transaction).
The diagram depicts the behaviour of both the SPI master and slave in the master read case.

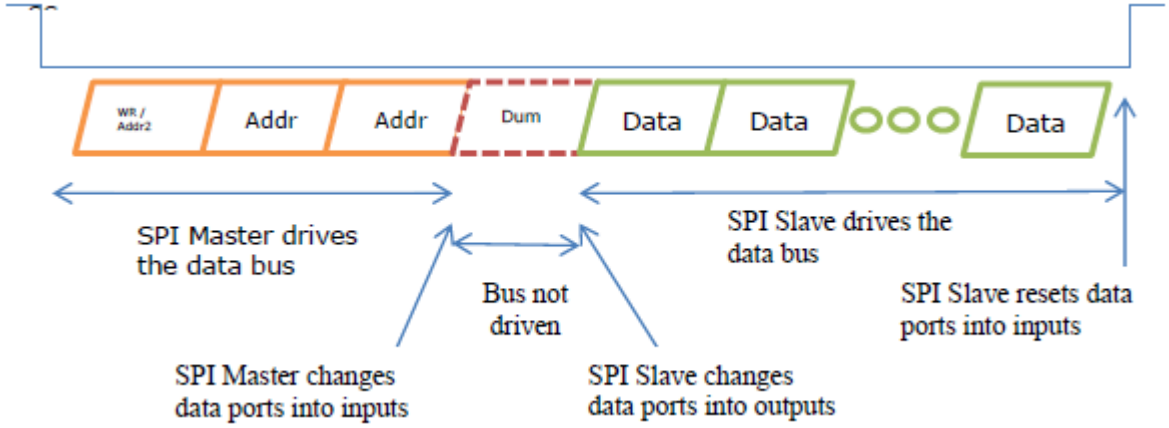


Figure 1 SPI Master and Slave in the Master Read Case

In the DUAL channel mode, MISO (MSB) and MOSI are used while in the QUAD channel mode. IO3 (MSB), IO2, MISO and MOSI are used.

Figure 2 illustrates a direct connection to a 3.3V IO MPU/MCU with single or dual SPI interface.

Figure 3 illustrates a direct connection to a 3.3V IO MPU/MCU with Quad SPI interface.

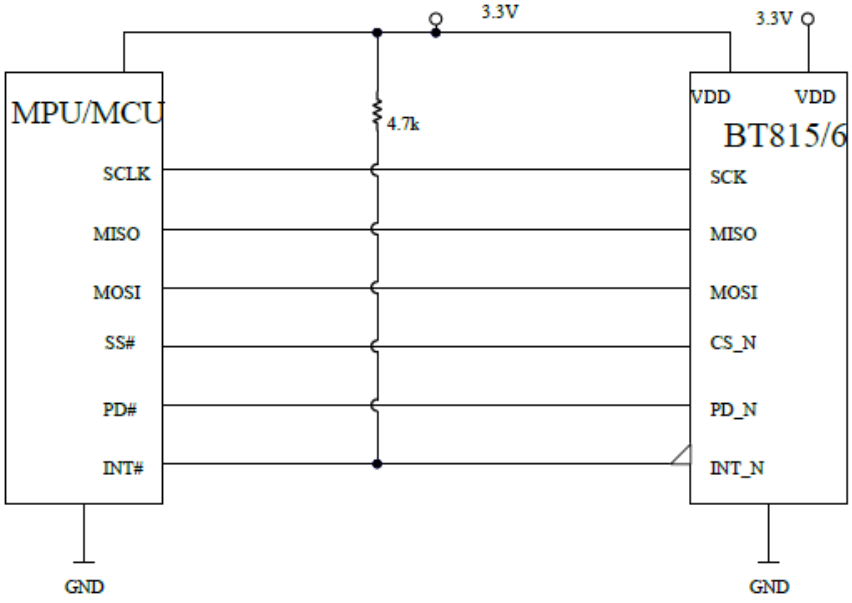


Figure 2 Single/Dual SPI Interface connection

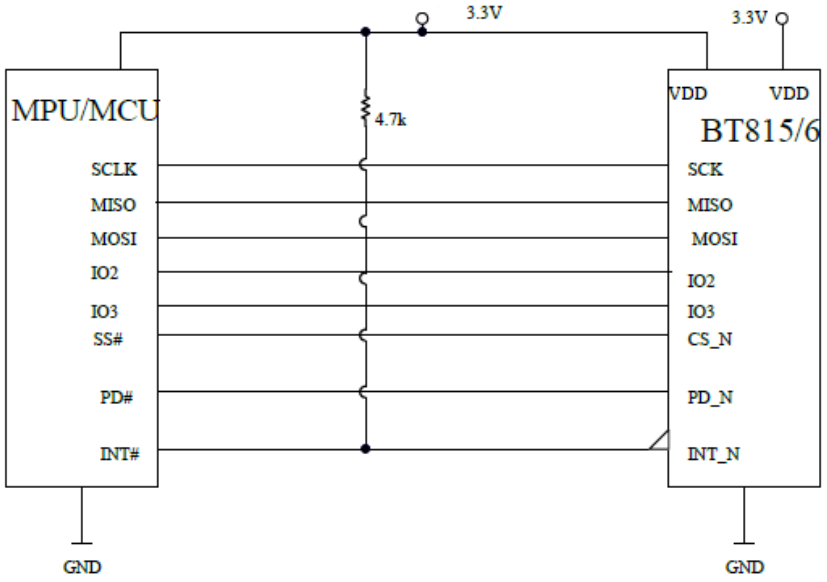
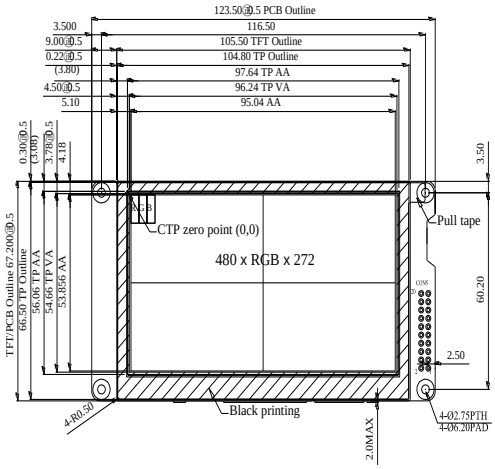
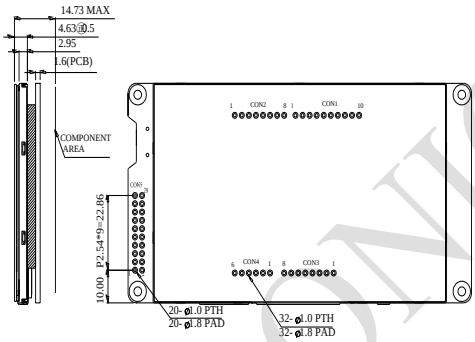


Figure 3 Quad SPI Interface connection

5.Contour Drawing





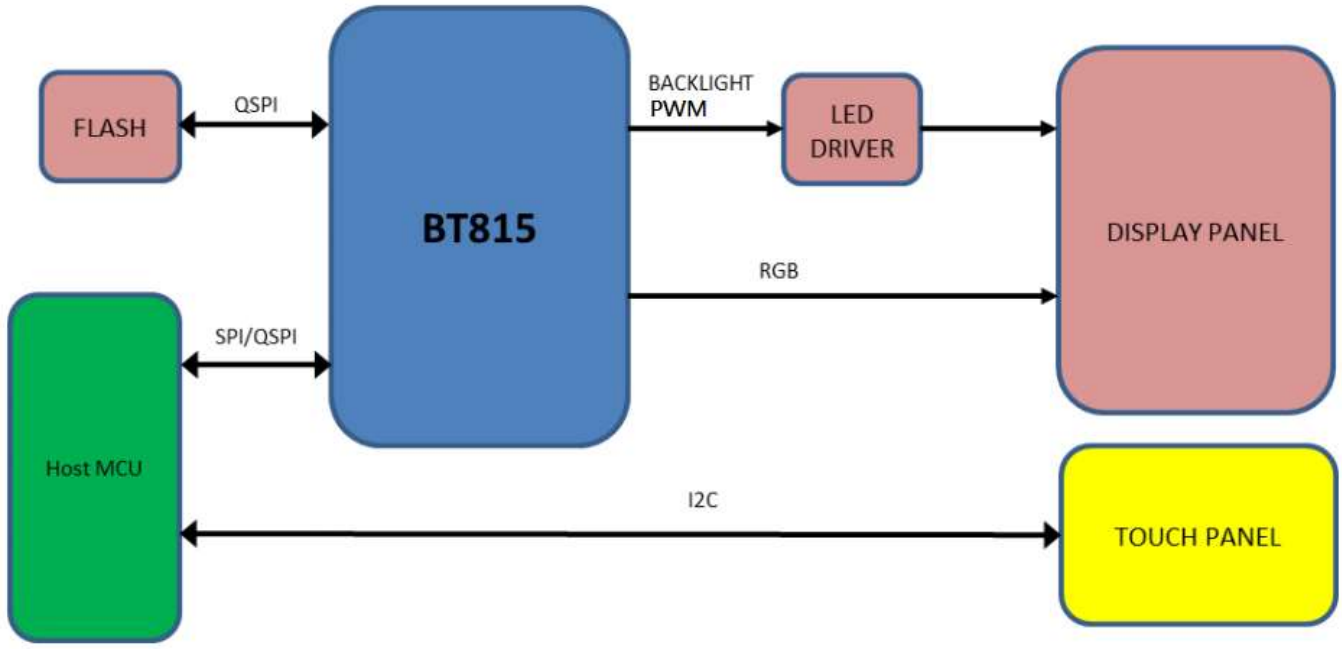
CON5			
PIN	SYMBOL	PIN	SYMBOL
1	VDD	2	GND
3	SCK	4	MISO
5	MOSI	6	CS
7	INT	8	PD_N
9	GPIO2	10	GPIO3
11	IO2	12	IO3
13	CSCL	14	CSDA
15	CRST	16	CINT
17	VLED	18	VLED
19	GND	20	GND

Note.

380nm transmittance(UV Cut at 380nm)<1.0%

The non-specified tolerance of dimension is ±0.3 mm .

6.Block Diagram



7.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-20	—	+70	□
Storage Temperature	TST	-30	—	+80	□

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. □60□, 90% RH MAX. Temp.＞60□, Absolute humidity shall be less than 90% RH at 60□

8.Electrical Characteristics

8.1. Operating conditions:

Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
Supply Voltage For VDD	VDD	—	3.1	3.3	3.5	V	—
Supply Current For VDD	IDD	VDD=3.3V	—	100	150	mA	Note1,2
Supply Voltage For VLED	VLED	—	4.5	5	5.5	V	—
Supply Current For VLED	ILED	VLED=+5V	—	200	300	mA	Note1

Note 1 : This(Typ) value is test for VDD=3.3V ,VLED=+5V , Ta=25 ℃ only

Note 2 : VDD Power consumption is include CTP driver system

8.2. Backlight PWM conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
PWM Control Duty Ratio	-	0	-	100	%	Note 4,5,6
PWM Control Frequency	-	250	-	10K	Hz	
LED Life Time	-	-	50,000	-	Hr	Note 1,2,3

Note 1 : Ta = 25 ℃

Note 2 : Brightness to be decreased to 50% of the initial value

Note 3 : The single LED lamp case

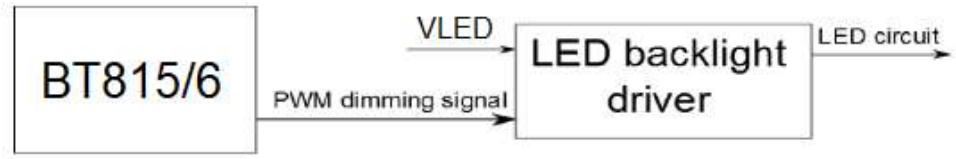
Note 4 : Turn ON the backlight when PWM =Low, Turn OFF when PWM =High

Note 5 : PWM Low Active Control from lowest brightness to highest brightness

Note 6 : Backlight PWM signal is internally connected to BT815/6 backlight control pin, This pin is controlled by BT815/6 registers

Note 7: The backlight dimming control pin (BACKLIGHT) is a pulse width modulated (PWM) signal controlled by two registers: REG_PWM_HZ and REG_PWM_DUTY. REG_PWM_HZ specifies the PWM output frequency, the range is 250-10000 Hz. REG_PWM_DUTY specifies the duty cycle; the range is 0-128. A value of 0 means that the PWM is completely off and 128 means completely on.

The BACKLIGHT pin will output low when the DISP pin is not enabled (i.e. logic 0).



8.3. SPI / CTP Operating conditions

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
Low level input voltage	VIL	0	-	0.3VDD	V	VDD=3.3V
High level input voltage	VIH	0.7VDD	-	VDD	V	

9.AC Characteristics

9.1. SPI Interface Timing

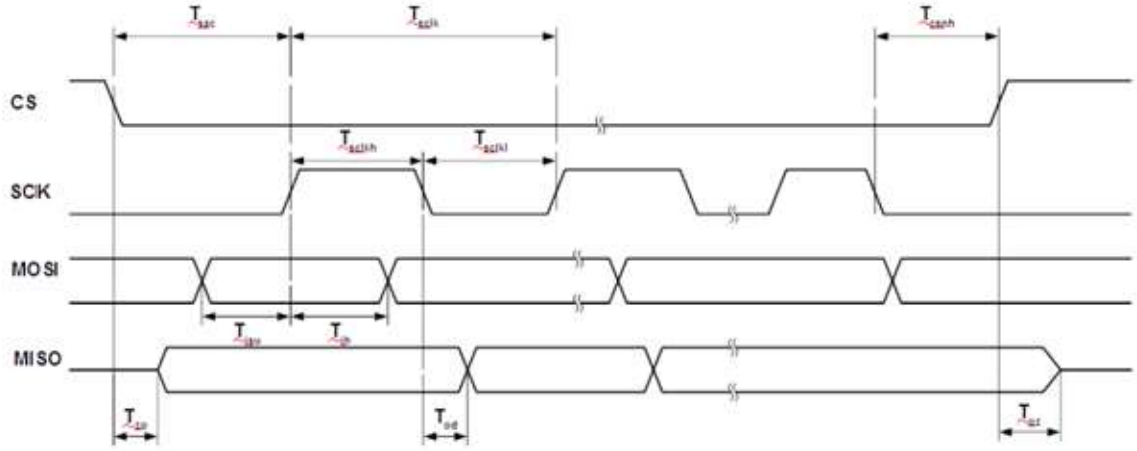


Figure 1 SPI Interface Timing

Parameter	Description	VDD=3.3V		Units
		Min	Max	
Tsclk	SPI clock period (SINGLE/DUAL mode)	33.3		ns
Tsclk	SPI clock period (QUAD mode)	33.3		ns
Tsclkl	SPI clock low duration	13		ns
Tsclkh	SPI clock high duration	13		ns
Tsac	SPI access time	3		ns
Tisu	Input Setup	3		ns
Tih	Input Hold	0		ns
Tzo	Output enable delay		11	ns
Toz	Output disable delay		10	ns
Tod	Output data delay		11	ns
Tcsnh	CSN hold time	0		ns

Table 1 SPI Interface Timing Specifications

For more information about BT816Q controller please go to official BT81x website.
https://brtchip.com/bt81x

9.2.

Internal Regulator and POR(Power-On-Reset)

The internal regulator will generate a Power-On-Reset (POR) pulse when the output voltage rises above the POR threshold. The POR will reset all the core digital circuits；It is possible to use the PD_N pin as an asynchronous hardware reset input. Drive PD_N low for at least 5ms and then drive it high will reset the BT815/6 chip.

9.3. Power Modes

When the supply to VDD is applied, the internal regulator is powered by VDD. An internal POR pulse will be generated during the regulator power up until it is stable. After the initial power up, the BT815/6 will stay in the SLEEP state. When needed, the host can set the BT815/6 to the ACTIVE state by performing a SPI ACTIVE command. The graphics engine, and the touch engine are only functional in the ACTIVE state. To save power the host can send a command to put the BT815/6 into any of the low power modes: STANDBY, SLEEP and POWERDOWN. In addition, the host is allowed to put the BT815/6 in POWERDOWN mode by driving the PD_N pin to low, regardless of what state it is currently in. Refer to Figure 2 for the power state transitions.

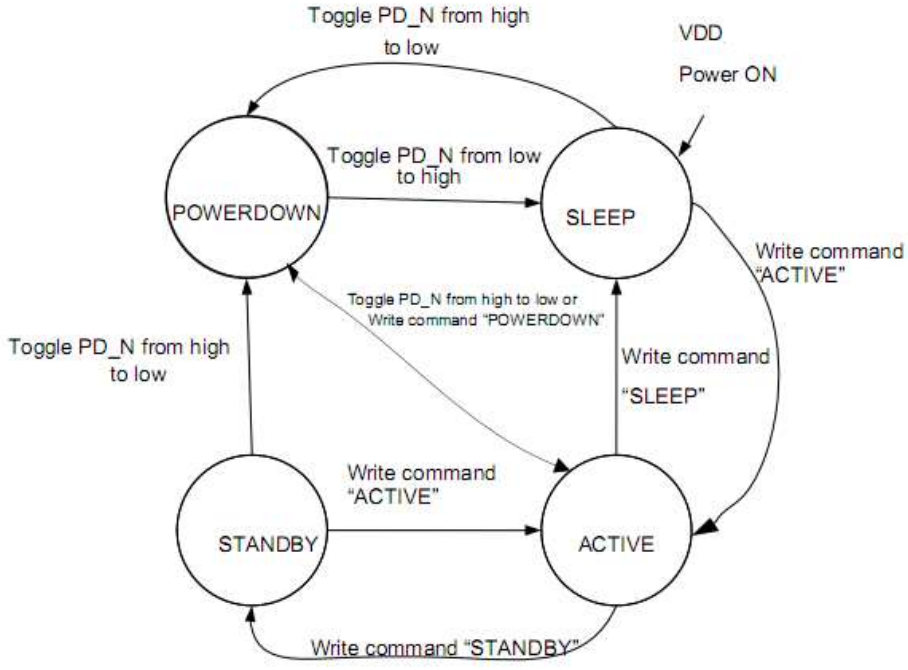
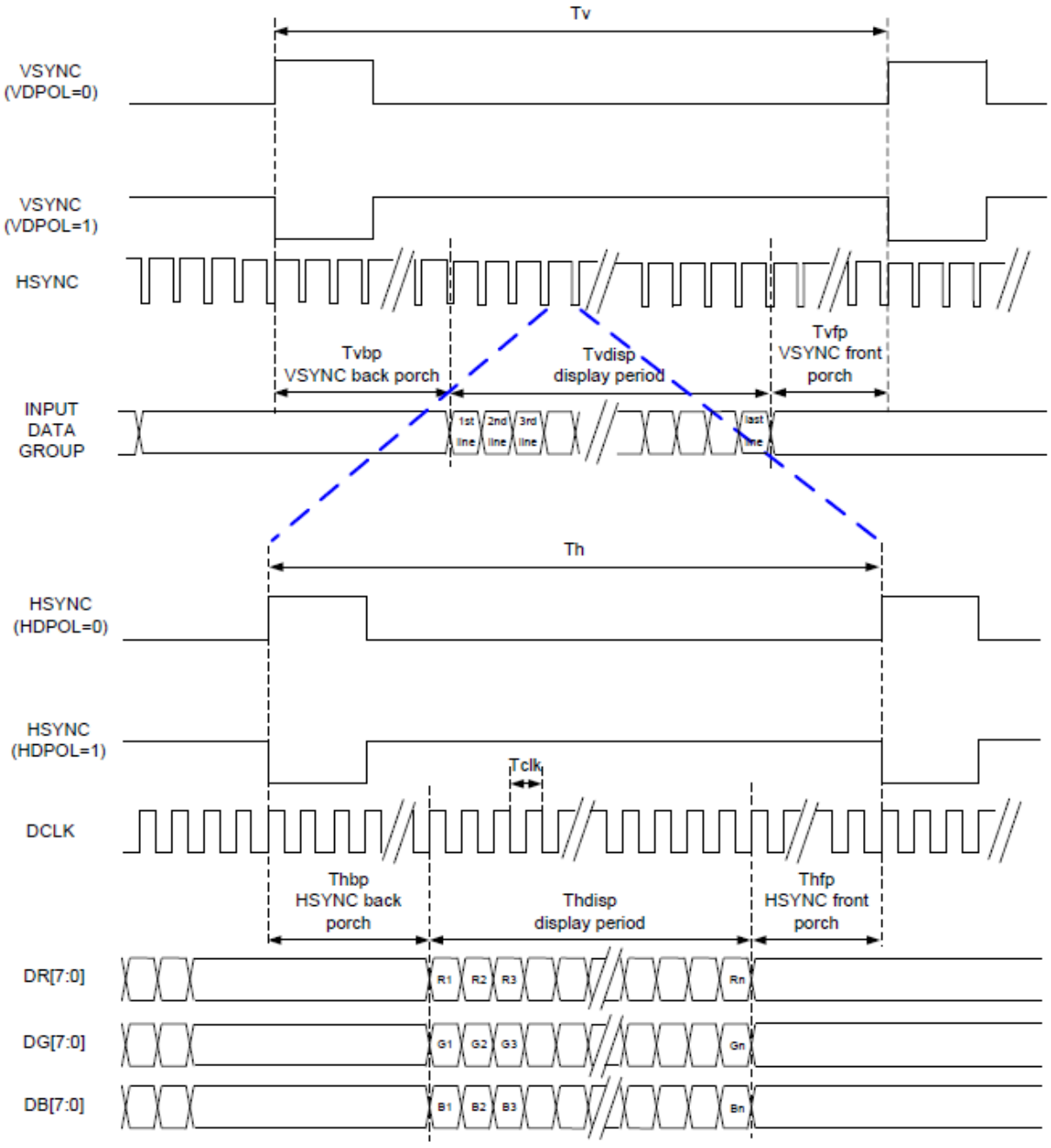


Figure 2 Power State Transition

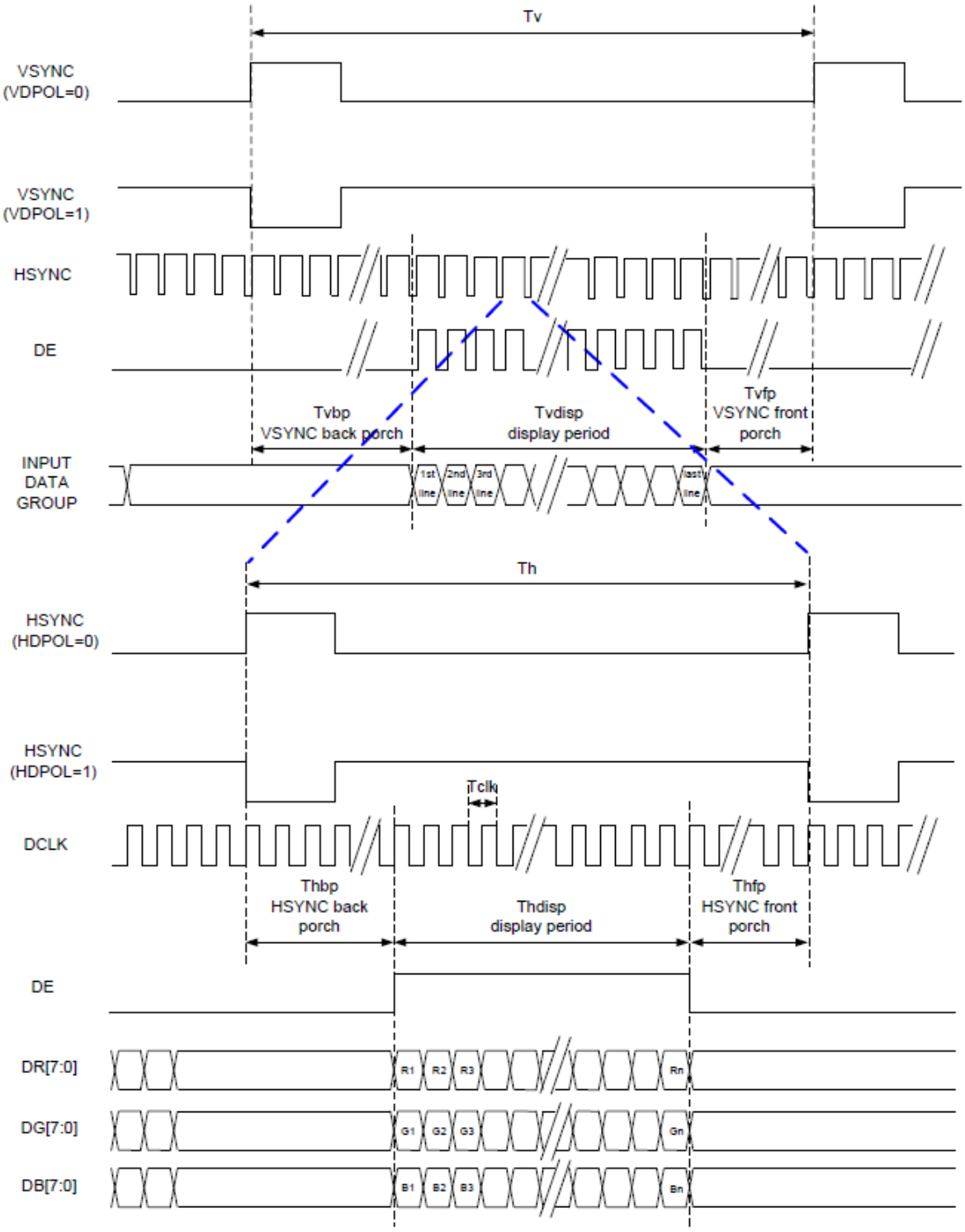
10.Timing Characteristics

10.1. RGB Interface

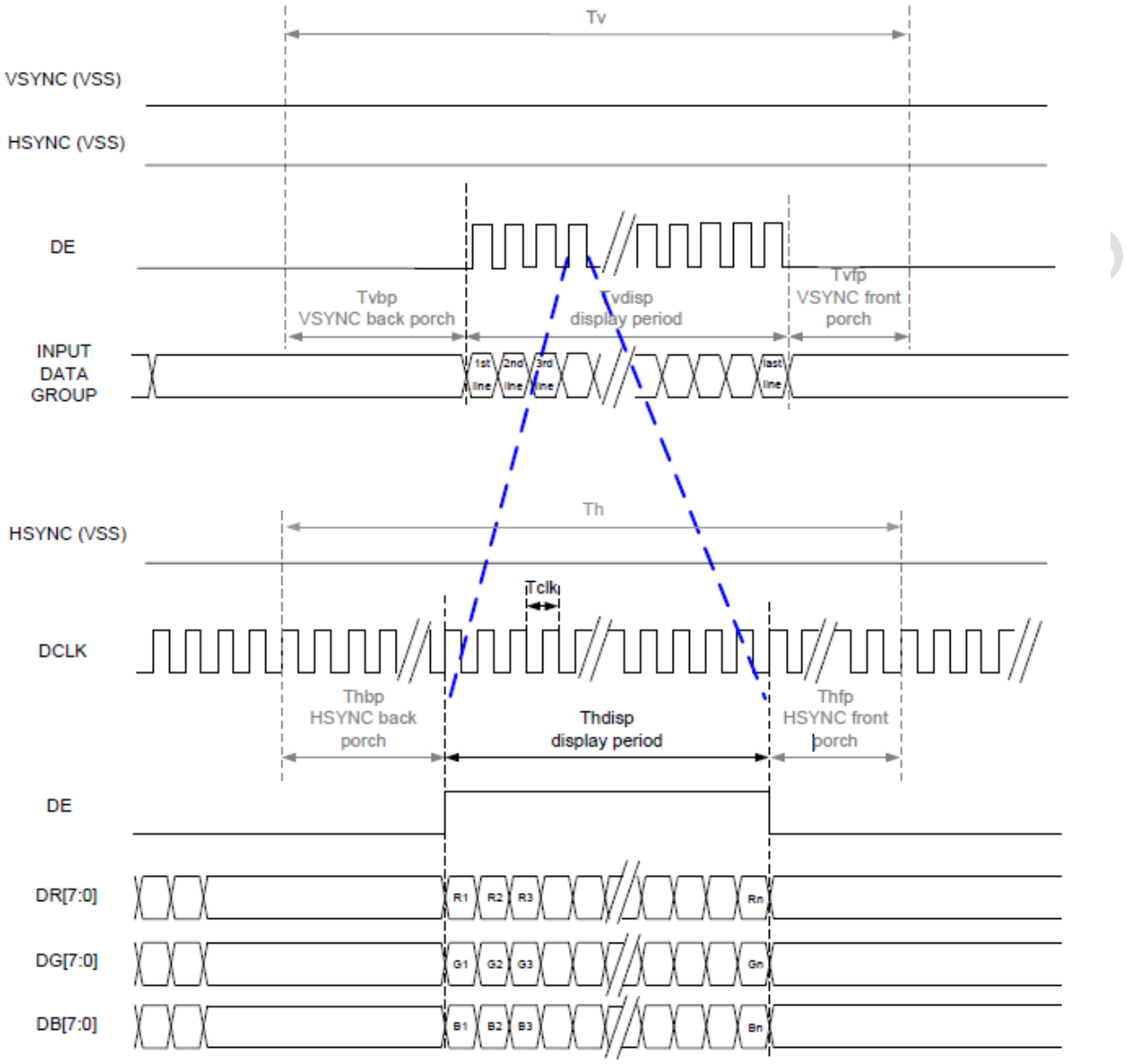
1. SYNC Mode



2. SYNC-DE Mode



3. DE Mode



RGB Mode Selection Table	DCLK	HSYNC	VSYNC	DE
SYNC - DE Mode	Input	Input	Input	Input
SYNC Mode	Input	Input	Input	GND
DE Mode	Input	GND	GND	Input

Note: "Input" means these signals are driven by host side.

10.2. Parallel 24 bit RGB Input Timing Table

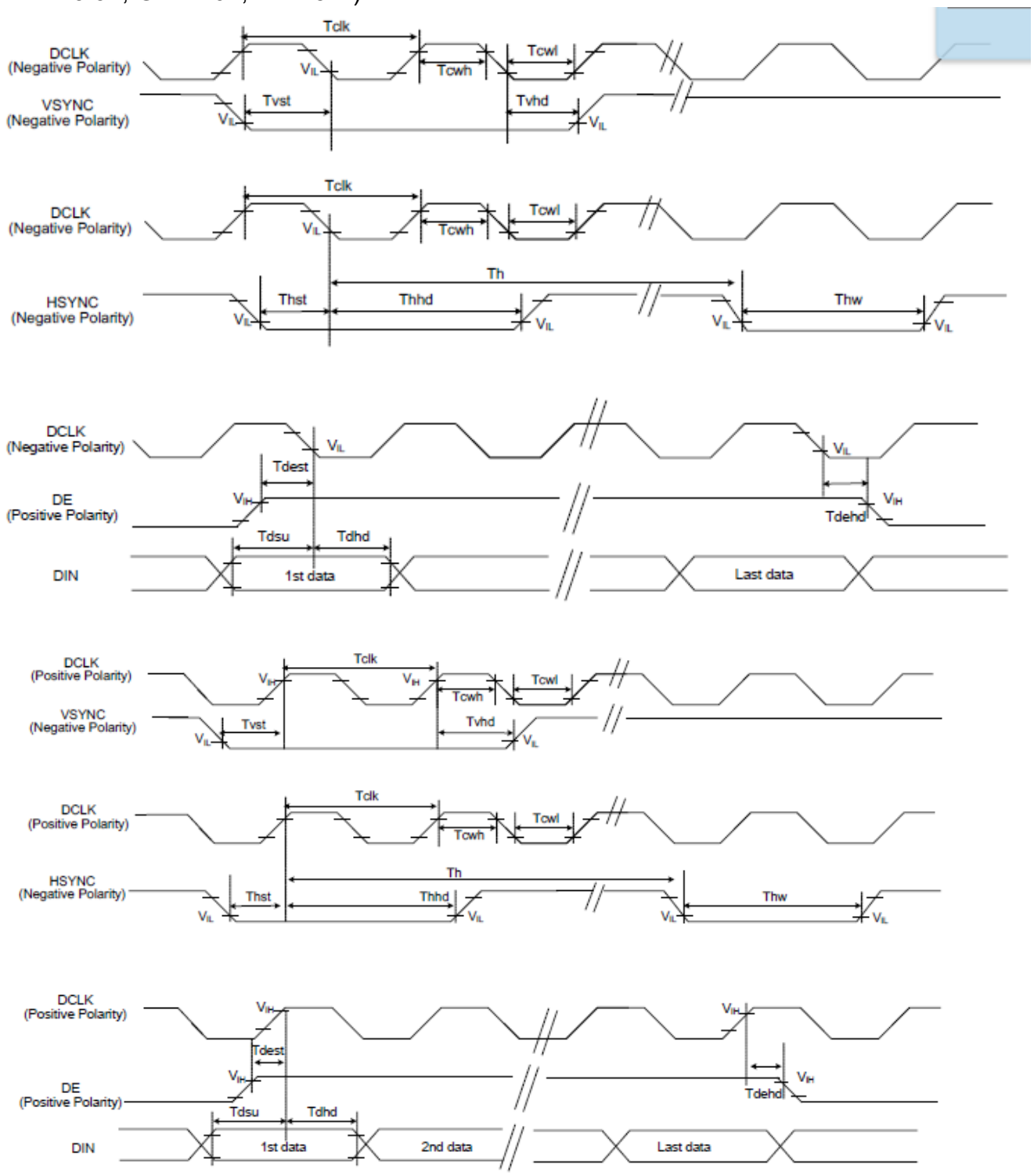
(Parallel 24-bit RGB Input Timing (VDD= 3.3V, GND= 0V, TA=25℃)

480RGB X 272 Resolution Timing Table							
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	8	9	12	MHz	
DCLK Period		Tclk	83	111	125	ns	
HSYNC	Period Time	Th	485	531	598	DCLK	
	Display Period	Thdisp		480		DCLK	
	Back Porch	Thbp	3	43	43	DCLK	Thbp of SYNC mode set by H_BLANKING[7:0]
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	43	DCLK	
VSYNC	Period Time	Tv	276	292	321	HSYNC	
	Display Period	Tvdisp		272		HSYNC	
	Back Porch	Tvbp	2	12	12	HSYNC	Tvbp of SYNC mode set by V_BLANKING[7:0]
	Front Porch	Tvfp	2	8	37	HSYNC	
	Pulse Width	Tvw	2	4	12	HSYNC	

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

10.3. System Bus Timing for RGB Interface

(VDD= 3.3V, GND= 0V, TA=25℃)



Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK Pulse Duty	Tcw	40	50	60	%	
HSYNC Width	Thw	2	-	-	DCLK	
VSYNC Setup Time	Tvst	12	-	-	ns	
VSYNC Hold Time	Tvhd	12	-	-	ns	
HSYNC Setup Time	Thst	12	-	-	ns	
HSYNC Hold Time	Thhd	12	-	-	ns	
Data Setup Time	Tdsu	12	-	-	ns	
Data Hold Time	Tdhd	12	-	-	ns	
DE Setup Time	Tdest	12	-	-	ns	
DE Hold Time	Tdehd	12	-	-	ns	

11.Optical Characteristics

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response time		Tr+ Tf	θ=0°、Φ=0°	-	30	40	ms	Note 3
Contrast ratio		CR	At optimized viewing angle	640	800	-	-	Note 4
Color Chromaticity	White	Wx	θ=0°、Φ=0	0.27	0.32	0.37	-	Note 2,6,7
		Wy		0.295	0.345	0.395	-	
Viewing angle	Hor.	ΘR	CR≧10	70	80	-	Deg.	Note 1
		ΘL		70	80	-		
	Ver.	ΦT		70	80	-		
		ΦB		70	80	-		
Brightness		-	-	300	400	-	cd/m²	Center of display
Uniformity		(U)	-	75	-	-	%	Note 5

Ta=25±2℃, IL=200mA

Note 1: Definition of viewing angle range

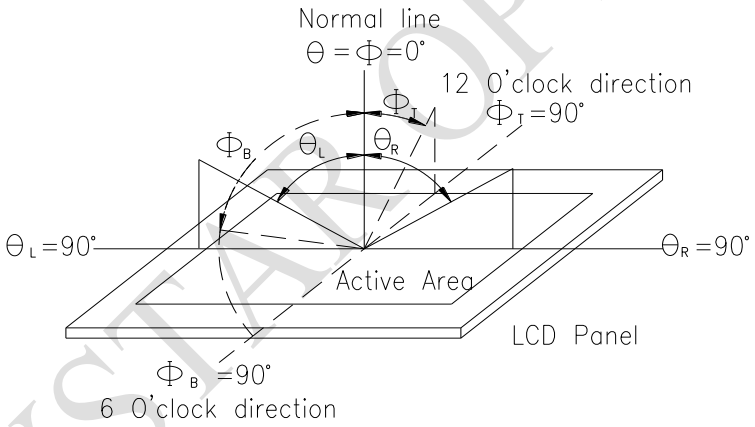


Fig. 11.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

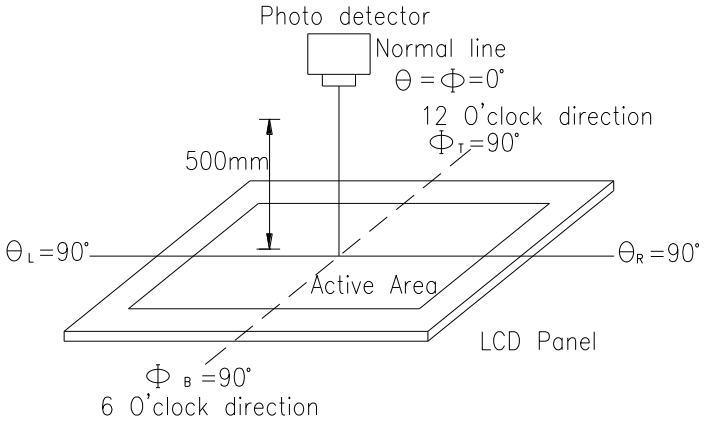
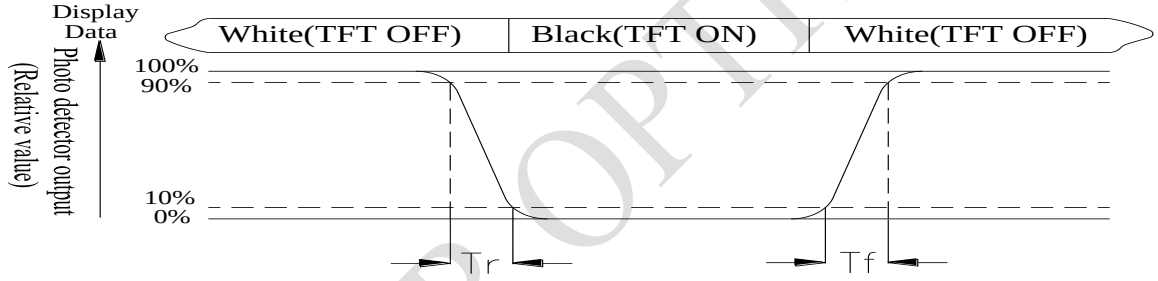


Fig. 11.2. Optical measurement system setup

Note 3: Definition of Response time:
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%



Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.
Luminance Uniformity (U) = Lmin/Lmax x100%
L = Active area length
W = Active area width

Fig 11.3. Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

12.Reliability

Content of Reliability Test (Wide temperature, -20□~70□)

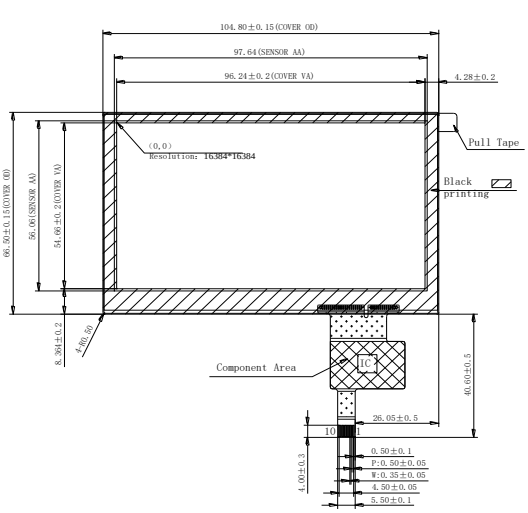
Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80□ 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30□ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70□ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20□ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60□,90%RH max	60□,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -20□ 25□ 70□ 30min 5min 30min 1 cycle	-20□/70□ 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact) ,±800v(air), RS=330Ω CS=150pF 10 times	——

Note1: No dew condensation to be observed.

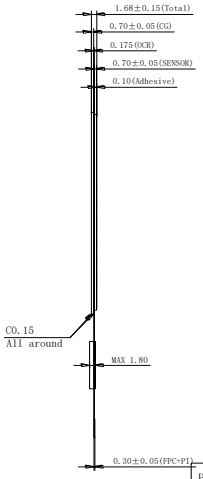
Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: The packing have to including into the vibration testing.

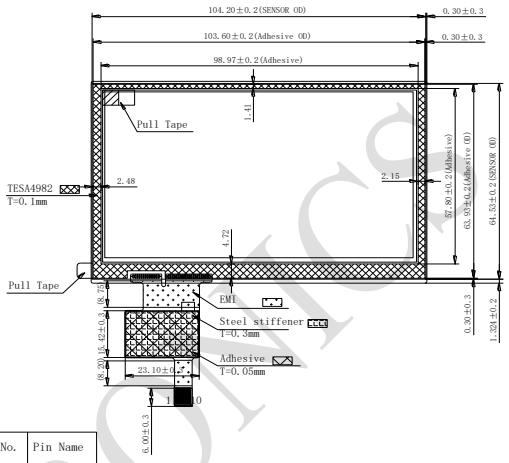
13.Touch Panel Information



Front view



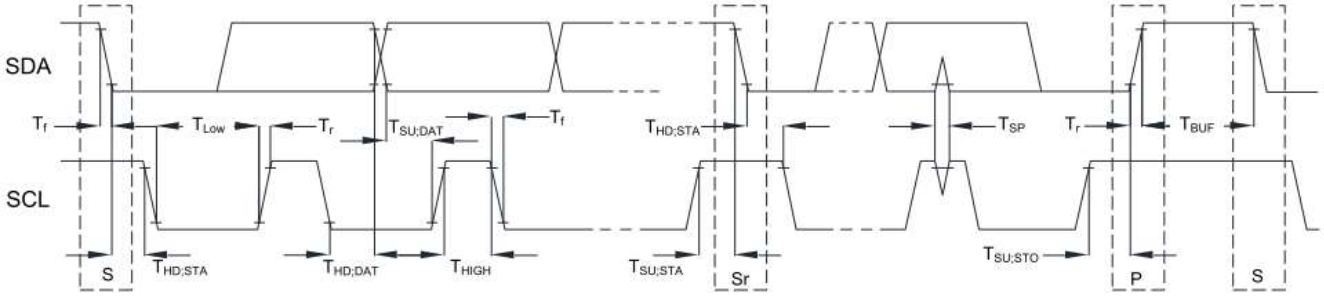
Side view



Back view

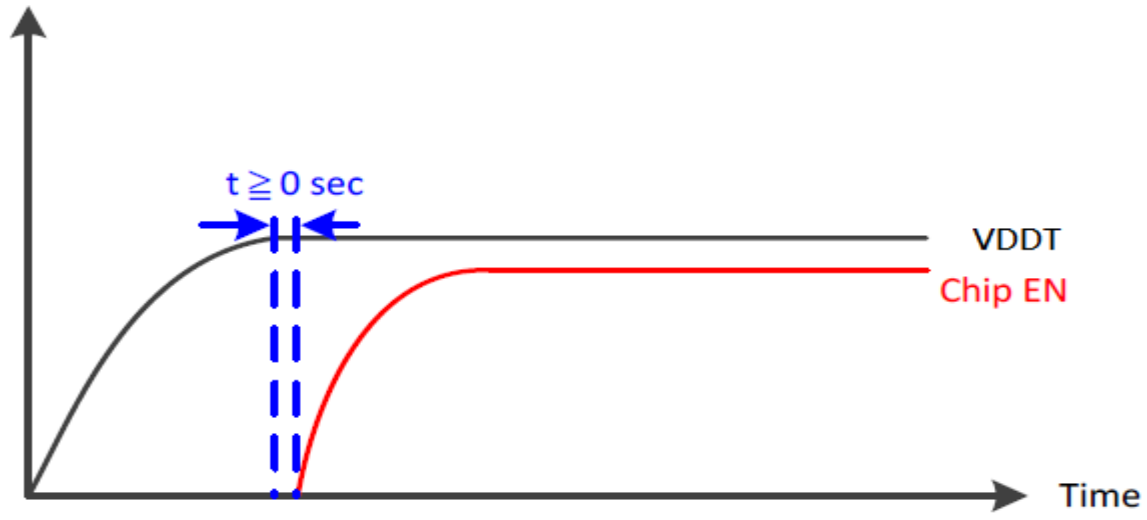
PIN No.	Pin Name
1	VSS
2	VDDT
3	SCL
4	NC
5	SDA
6	NC
7	RST
8	NC
9	INT
10	VSS

13.1. I2C AC Characteristics

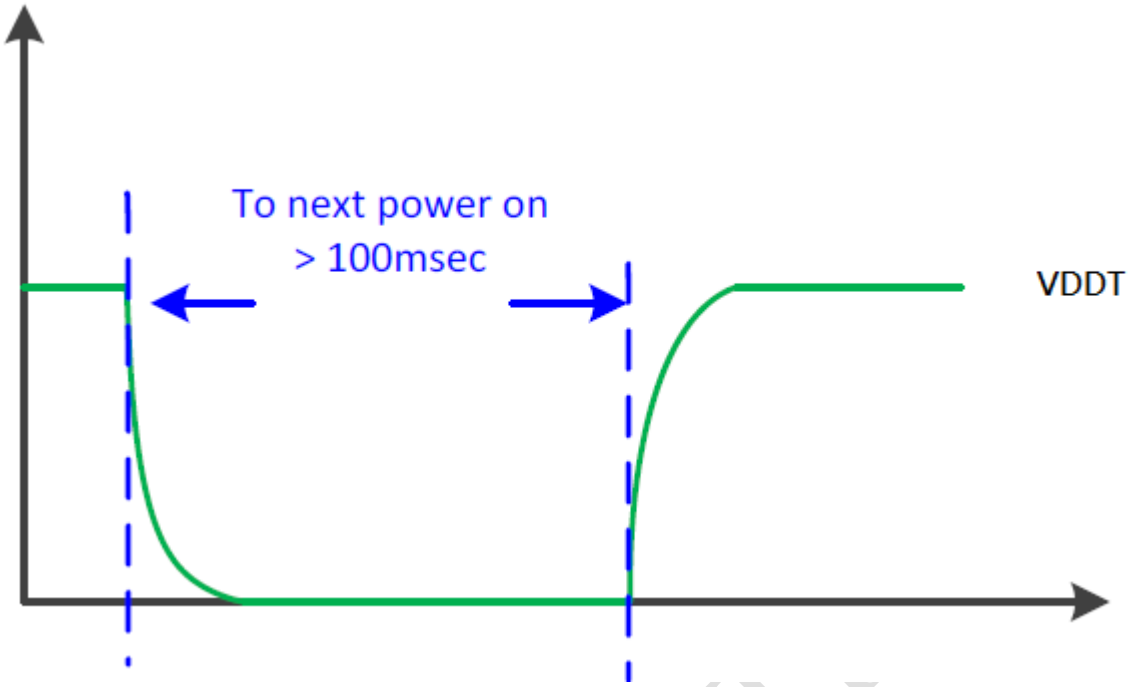


Item	Symbol	100kHz		400kHz		Unit
		Min.	Max.	Min.	Max.	
SCL standard mode clock frequency	FSCL	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock is generated.	THD;STA	4	--	0.6	--	us
LOW period of the SCL clock	TLOW	4.7	--	1.3	--	us
HIGH period of the SCL clock	THIGH	4	--	0.6	--	us
Setup time for a repeat START condition.	TSU;STA	4.7	--	0.6	--	us
Data hold time	THD;DAT	0	3.45	0	0.9	us
Data setup time	TSU;DAT	250	--	100	--	ns
Rising time of both SDA and SCL signals	Tr	--	1000	--	300	ns
Falling time of both SDA and SCL signals	Tf	--	300	--	300	ns
Setup time for STOP condition.	TSU;STO	4	--	0.6	--	us
Free time between STOP and START condition	TBUF	4.7	--	1.3	--	us
Pulse width of spikes which must be suppressed by input filter	TSP	--	--	0	50	ns

13.2. Power On Sequence



13.3. Power Off to Power On Sequence



14.Initial Code For Reference

1. REGISTER VALUES:

REG_HSIZE 480

REG_VSIZE 272

REG_HCYCLE 548

REG_HOFFSET 43

REG_HSYNC0 0

REG_HSYNC1 41

REG_VCYCLE 292

REG_VOFFSET 12

REG_VSYNC0 0

REG_VSYNC1 10

REG_SWIZZLE 0

REG_PCLK_POL 1

REG_CSPREAD 1

LCM Sample Estimate Feedback Sheet		
Module Number：_____		
1、Panel Specification：		
1. Panel Type：	□ Pass	□ NG ,_____
2. View Direction：	□ Pass	□ NG ,_____
3. Numbers of Dots：	□ Pass	□ NG ,_____
4. View Area：	□ Pass	□ NG ,_____
5. Active Area：	□ Pass	□ NG ,_____
6.Operating Temperature：	□ Pass	□ NG ,_____
7.Storage Temperature：	□ Pass	□ NG ,_____
8.Others：_____		
2、Mechanical Specification：		
1. PCB Size：	□ Pass	□ NG ,_____
2.Frame Size：	□ Pass	□ NG ,_____
3.Materal of Frame：	□ Pass	□ NG ,_____
4.Connector Position：	□ Pass	□ NG ,_____
5.Fix Hole Position：	□ Pass	□ NG ,_____
6.Backlight Position：	□ Pass	□ NG ,_____
7. Thickness of PCB：	□ Pass	□ NG ,_____
8. Height of Frame to PCB：	□ Pass	□ NG ,_____
9.Height of Module：	□ Pass	□ NG ,_____
10.Others：	□ Pass	□ NG ,_____
3、Relative Hole Size：		
1.Pitch of Connector：	□ Pass	□ NG ,_____
2.Hole size of Connector：	□ Pass	□ NG ,_____
3.Mounting Hole size：	□ Pass	□ NG ,_____
4.Mounting Hole Type：	□ Pass	□ NG ,_____
5.Others：	□ Pass	□ NG ,_____
4、Backlight Specification：		
1.B/L Type：	□ Pass	□ NG ,_____
2.B/L Color：	□ Pass	□ NG ,_____
3.B/L Driving Voltage (Reference for LED Type)：□ Pass □ NG ,_____		
4.B/L Driving Current：	□ Pass	□ NG ,_____
5.Brightness of B/L：	□ Pass	□ NG ,_____
6.B/L Solder Method：	□ Pass	□ NG ,_____
7.Others：	□ Pass	□ NG ,_____

>> **Go to page 2** <<

Module Number：_____		
5、Electronic Characteristics of Module：		
1.Input Voltage：	□ Pass	□ NG ,_____
2.Supply Current：	□ Pass	□ NG ,_____
3.Driving Voltage for LCD：	□ Pass	□ NG ,_____
4.Contrast for LCD：	□ Pass	□ NG ,_____
5.B/L Driving Method：	□ Pass	□ NG ,_____
6.Negative Voltage Output：	□ Pass	□ NG ,_____
7.Interface Function：	□ Pass	□ NG ,_____
8.LCD Uniformity：	□ Pass	□ NG ,_____
9.ESD test：	□ Pass	□ NG ,_____
10.Others：	□ Pass	□ NG ,_____

6、Summary：

Sales signature：_____

Customer Signature：_____ **Date**：__/__/__