100V COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	BV_{DSS}	$R_{DS(ON)}$ (Ω)max	I_D (A)max T_A = +25°C
Q1	100V	0.230 @ V_{GS} = 10V	2.1
		0.300 @ V_{GS} = 4.5V	1.9
Q2	-100V	0.235 @ V_{GS} = -10V	-2.2
		0.320 @ V_{GS} = -4.5V	-1.9

Features

- 100V Complementary in SO-8 Package
- Low On-Resistance
- Fast Switching Speed
- Low Voltage (V_{GS} = 4.5V) Gate Drive
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Description

This new generation complementary dual MOSFET features low on-resistance achievable with low gate drive.

Mechanical Data

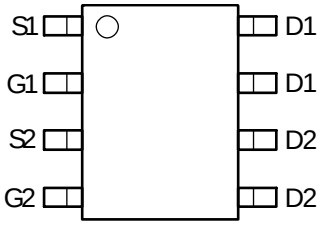
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin Annealed over Copper Lead Frame. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.074 grams (Approximate)

Applications

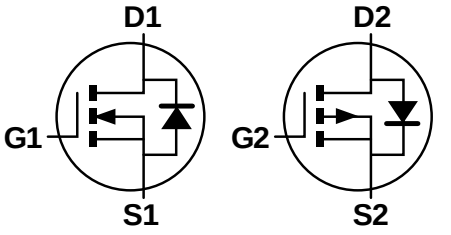
- DC Motor Control
- Backlighting

SO-8

Top View



Top View



Q1 N-Channel Q2 P-Channel

Equivalent Circuit

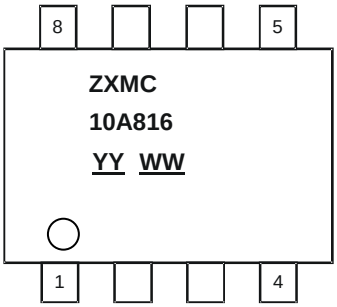
Ordering Information (Note 4)

Part Number	Reel Size (inches)	Tape Width (mm)	Quantity Per Reel
ZXMC10A816N8TA	7	12	500
ZXMC10A816N8TC	13	12	2,500

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

Top View



ZXMC10A816 = Product Type Marking Code
YY WW = Date Code Marking
YY = Year (ex: 17 = 2017)
WW = Week (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

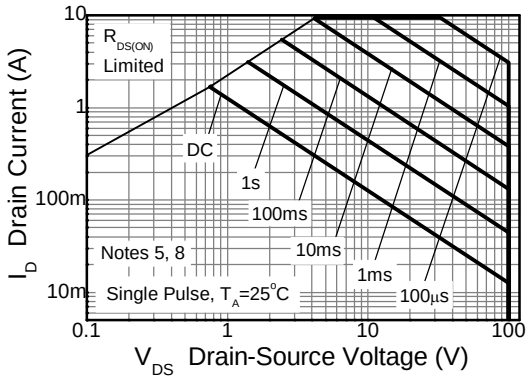
Parameter	Symbol	N-channel Q1	P-channel Q2	Unit
Drain-Source Voltage	V_{DSS}	100	-100	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current @ V_{GS}= 10V; T_A= +25°C (Notes 6, 8) @ V_{GS}= 10V; T_A= +70°C (Notes 6, 8) @ V_{GS}= 10V; T_A= +25°C (Notes 5, 8) @ V_{GS}= 10V; T_A= +25°C (Notes 5, 9) @ V_{GS}= 10V; T_L= +25°C (Notes 8, 10)	I_D	2.1 1.7 1.7 2.0 2.3	-2.2 -1.8 -1.7 -2.0 -2.4	A
Pulsed Drain Current @ V_{GS} = 10V; T_A = +25°C (Notes 7, 8)	I_{DM}	9.4	-10.5	A
Continuous Source Current (Body Diode) at T_A = +25°C (Notes 6, 8)	I_S	3.0	-3.1	A
Pulsed Source Current (Body Diode) at T_A = +25°C (Notes 7, 8)	I_{SM}	9.4	-10.5	A
Avalanche Current (Note 11) L = 0.1mH	I_{AS}	1.2	-12	A
Power Dissipation at T_A = +25°C (Notes 5, 8) Linear Derating Factor	P_D	1.3 10.0		W mW/°C
Power Dissipation at T_A = +25°C (Notes 5, 9) Linear Derating Factor	P_D	1.8 14.2		W mW/°C
Power Dissipation at T_A = +25°C (Notes 6, 8) Linear Derating Factor	P_D	2.1 16.7		W mW/°C
Power Dissipation at T_L = +25°C (Notes 8, 10) Linear Derating Factor	P_D	2.4 18.9	2.6 20.4	W mW/°C
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150		°C

Thermal Characteristics

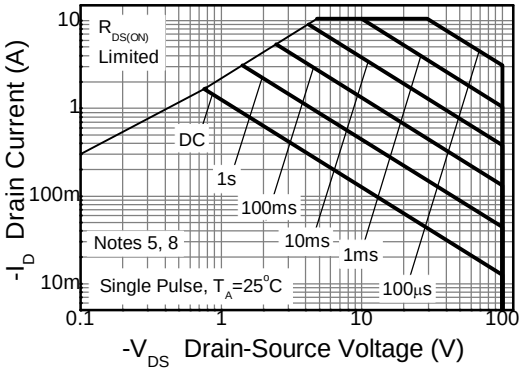
Parameter	Symbol	Value		Unit
Junction to Ambient (Notes 5, 8)	$R_{\theta JA}$	100		°C/W
Junction to Ambient (Notes 5, 9)	$R_{\theta JA}$	70		°C/W
Junction to Ambient (Notes 6, 8)	$R_{\theta JA}$	60		°C/W
Junction to Lead (Notes 8, 10)	$R_{\theta JL}$	53	49	°C/W

Notes:
5. For a device surface mounted on 25mm x 25mm x 1.6mm FR-4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
6. Same as note (5), except the device is measured at t ≤ 10 sec.
7. Same as note (5), except the device is pulsed with D = 0.02 and pulse width 300µs. The pulse current is limited by the maximum junction temperature.
8. For a dual device with one active die.
9. For a device with two active die running at equal power.
10. Thermal resistance from junction to solder-point (at the end of the drain lead); the device is operating in a steady-state condition.
11. I_{AS} rating is based on low frequency and duty cycles to keep T_J = +25°C.

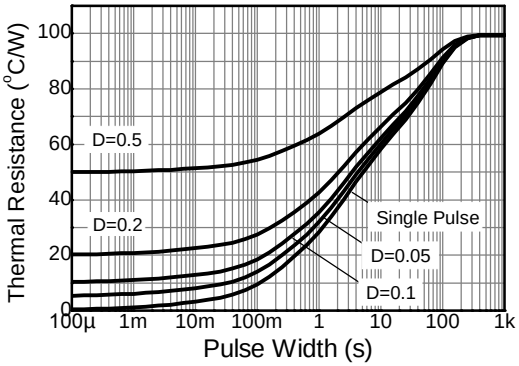
Thermal Characteristics



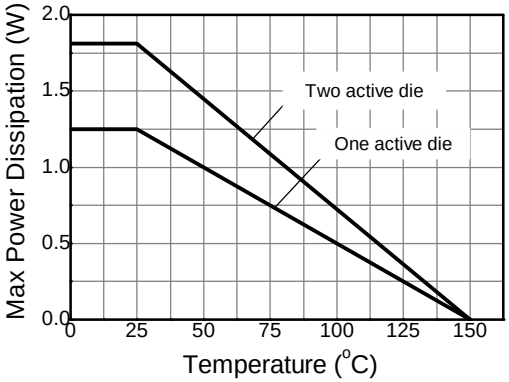
N-channel Safe Operating Area



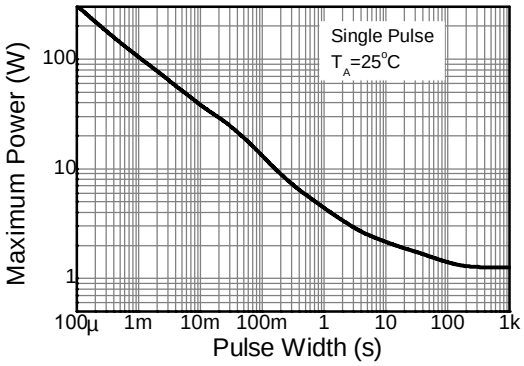
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



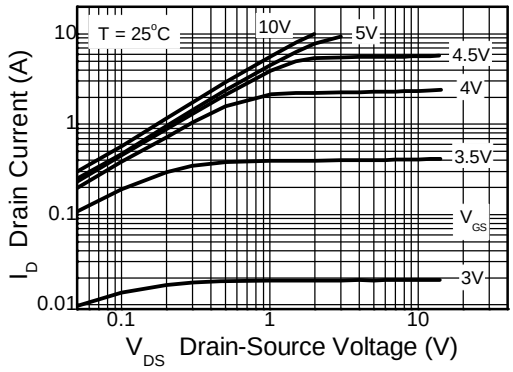
Pulse Power Dissipation

Electrical Characteristics Q1 N-Channel (@T_A = +25°C, unless otherwise specified.)

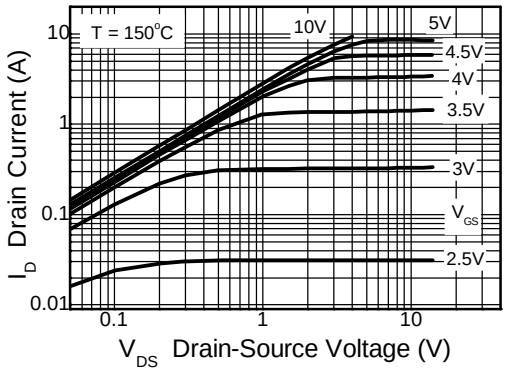
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	100	—	—	V	I_D = 250µA, V_{GS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	—	—	0.5	µA	V_{DS} = 100V, V_{GS} = 0V
Gate-Body Leakage	I_{GSS}	—	—	100	nA	V_{GS} = ±20V, V_{DS} = 0V
Gate-Source Threshold Voltage	$V_{GS(TH)}$	1.7	—	2.4	V	I_D = 250µA, V_{DS} = V_{GS}
Static Drain-Source On-State Resistance (Note 12)	$R_{DS(ON)}$	—	0.170 0.210	0.230 0.300	Ω	V_{GS} = 10V, I_D = 1.0A V_{GS} = 4.5V, I_D = 0.5A
Forward Transconductance (Notes 12, 14)	g_{fs}	—	4.8	—	S	V_{DS} = 15V, I_D = 1.6A
Dynamic Capacitance (Note 14)						
Input Capacitance	C_{iss}	—	497	—	pF	V_{DS} = 50V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	29	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	18	—	pF	
Switching (Notes 13, 14)						
Turn-On-Delay Time	$t_{D(ON)}$	—	2.9	—	ns	V_{DD} = 50V, V_{GS} = 10V I_D = 1.0A $R_G \cong$ 6.0Ω
Rise Time	t_R	—	2.1	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	12.1	—	ns	
Fall Time	t_F	—	5.0	—	ns	
Gate Charge (Note 14)						
Total Gate Charge	Q_g	—	9.2	—	nC	V_{DS} = 50V, V_{GS} = 10V I_D = 1.6A
Gate-Source Charge	Q_{gs}	—	1.7	—	nC	
Gate-Drain Charge	Q_{gd}	—	2.5	—	nC	
Source–Drain Diode						
Diode Forward Voltage (Note 12)	V_{SD}	—	0.85	0.95	V	I_S = 1.7A, V_{GS} = 0V
Reverse Recovery Time (Note 14)	t_{RR}	—	32	—	ns	I_S = 1.7A, di/dt = 100A/µs
Reverse Recovery Charge (Note 14)	Q_{RR}	—	40	—	nC	
Gate Resistance						
Gate Resistance	R_G	0	—	3	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz

Notes: 12. Measured under pulsed conditions. Pulse width ≤ 300µs; duty cycle ≤ 2%.
13. Switching characteristics are independent of operating junction temperature.
14. For design aid only, not subject to production testing.

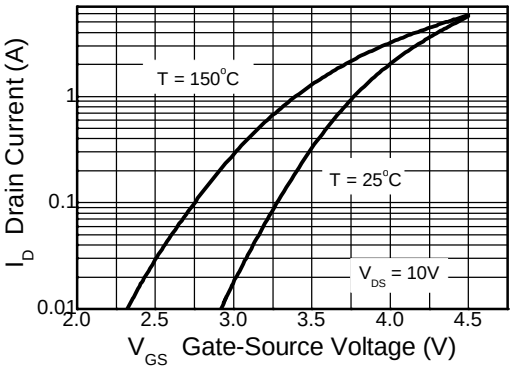
Typical Characteristics Q1 N-Channel



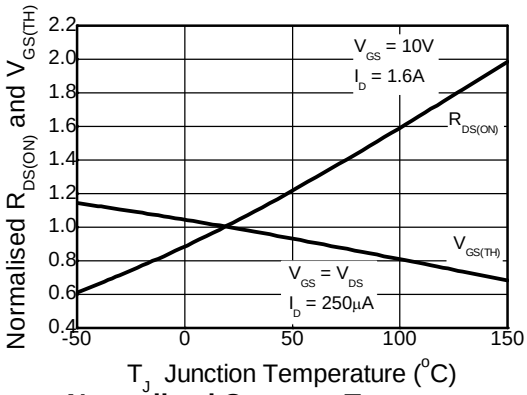
Output Characteristics



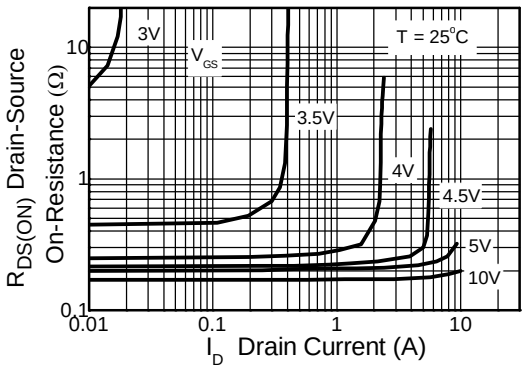
Output Characteristics



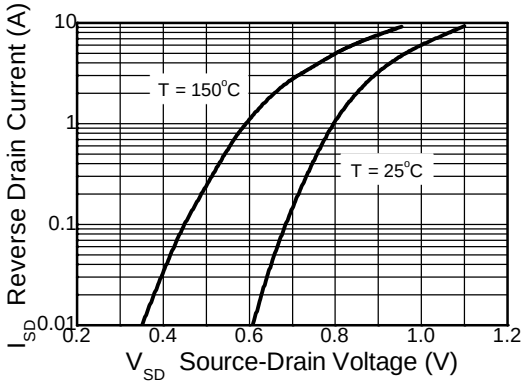
Typical Transfer Characteristics



Normalised Curves v Temperature

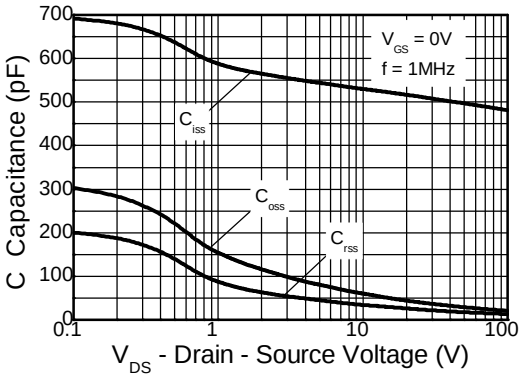


On-Resistance v Drain Current

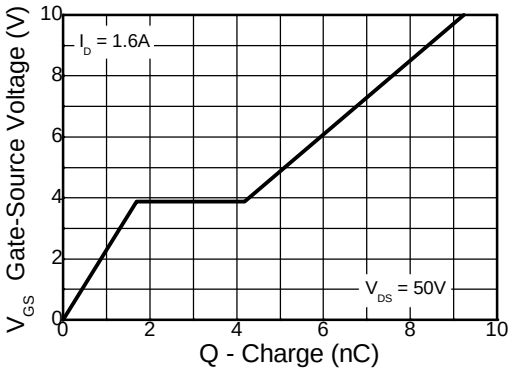


Source-Drain Diode Forward Voltage

Typical Characteristics Q1 N-Channel (Cont.)

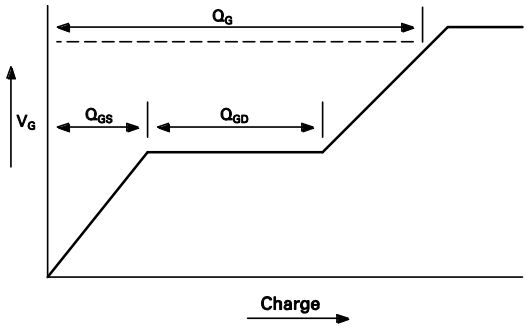


Capacitance v Drain-Source Voltage

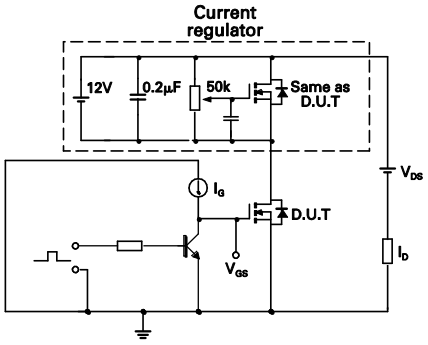


Gate-Source Voltage v Gate Charge

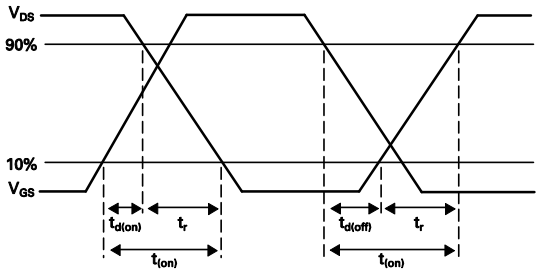
Test Circuits



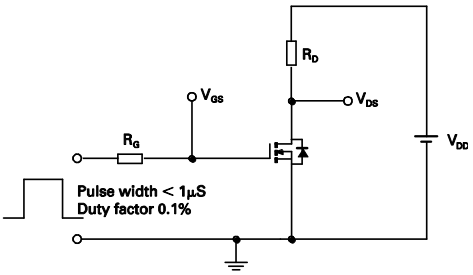
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



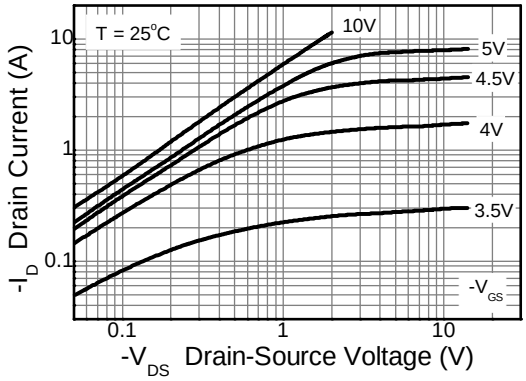
Switching time test circuit

Electrical Characteristics Q2 P-Channel (@T_A = +25°C, unless otherwise specified.)

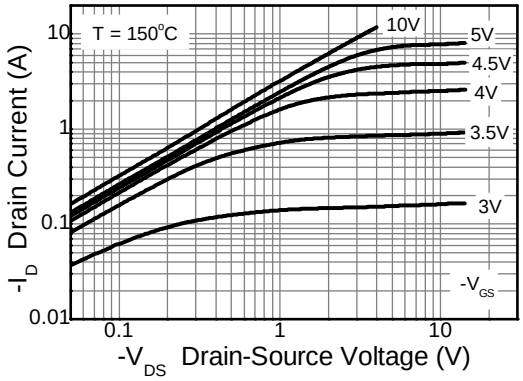
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	-100	—	—	V	I_D = -250µA, V_{GS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-0.5	µA	V_{DS} = -100V, V_{GS} = 0V
Gate-Body Leakage	I_{GSS}	—	—	-100	nA	V_{GS} = ±20V, V_{DS} = 0V
Gate-Source Threshold Voltage	$V_{GS(TH)}$	-2.0	—	-3.0	V	I_D = -250µA, V_{DS} = V_{GS}
Static Drain-Source On-State Resistance (Note 12)	$R_{DS(ON)}$	—	0.170 0.250	0.235 0.320	Ω	V_{GS} = -10V, I_D = -1.0A V_{GS} = -4.5V, I_D = -0.5A
Forward Transconductance (Notes 12, 14)	g_{fs}	—	4.7	—	S	V_{DS} = -15V, I_D = -2.1A
Dynamic Capacitance (Note 14)						
Input Capacitance	C_{iss}	—	717	—	pF	V_{DS} = -50V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	55	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	46	—	pF	
Switching (Notes 13, 14)						
Turn-On-Delay Time	$t_{D(ON)}$	—	4.3	—	ns	V_{DD} = -50V, V_{GS} = -10V I_D = -1A $R_G \cong$ 6.0Ω
Rise Time	t_R	—	5.2	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	20	—	ns	
Fall Time	t_F	—	12	—	ns	
Gate Charge (Note 14)						
Total Gate Charge	Q_g	—	16.5	—	nC	V_{DS} = -50V, V_{GS} = -10V I_D = -2.1A
Gate-Source Charge	Q_{gs}	—	2.5	—	nC	
Gate-Drain Charge	Q_{gd}	—	5.4	—	nC	
Source-Drain Diode						
Diode Forward Voltage (Note 12)	V_{SD}	—	-0.85	-0.95	V	I_S = -1.7A, V_{GS} = 0V
Reverse Recovery Time (Note 14)	t_{RR}	—	43	—	ns	I_S = -1.7A, di/dt = 100A/µs
Reverse Recovery Charge (Note 14)	Q_{RR}	—	77	—	nC	
Gate Resistance						
Gate Resistance	R_G	0	—	100	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz

Notes: 12. Measured under pulsed conditions. Pulse width ≤ 300µs; duty cycle ≤ 2%.
13. Switching characteristics are independent of operating junction temperature.
14. For design aid only, not subject to production testing.

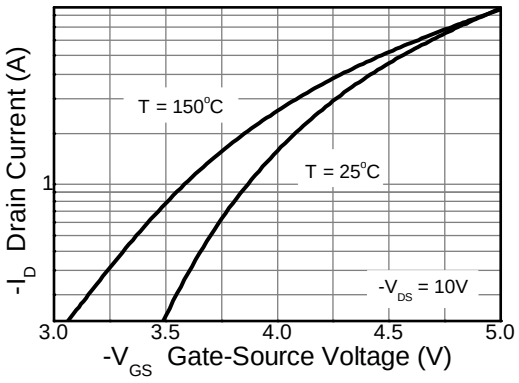
Typical Characteristics Q2 P-Channel



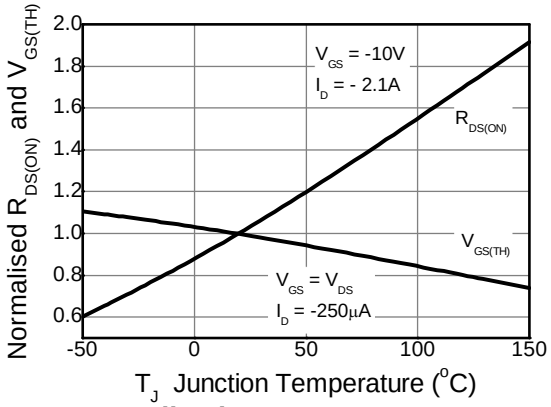
Output Characteristics



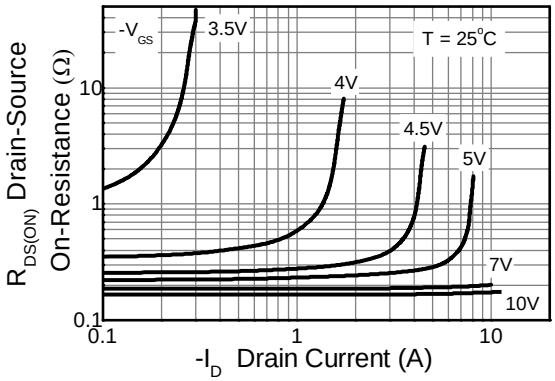
Output Characteristics



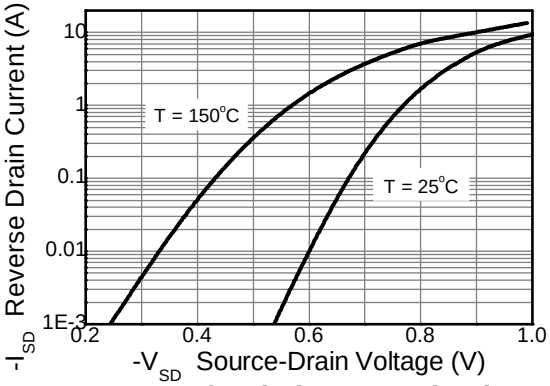
Typical Transfer Characteristics



Normalised Curves v Temperature

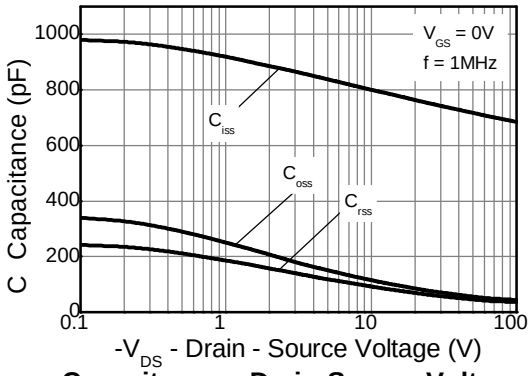


On-Resistance v Drain Current

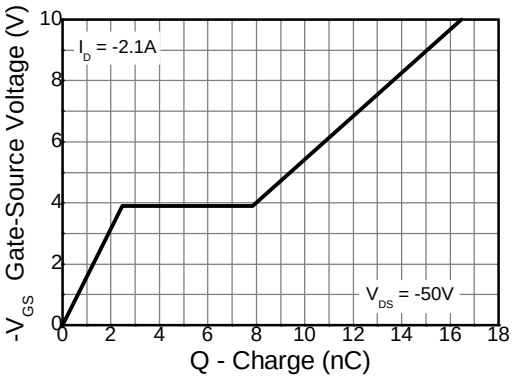


Source-Drain Diode Forward Voltage

Typical Characteristics Q2 P-Channel (Cont.)

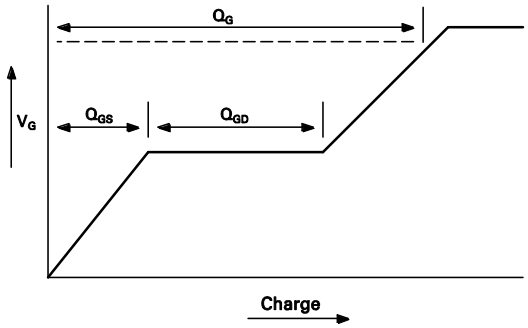


Capacitance v Drain-Source Voltage

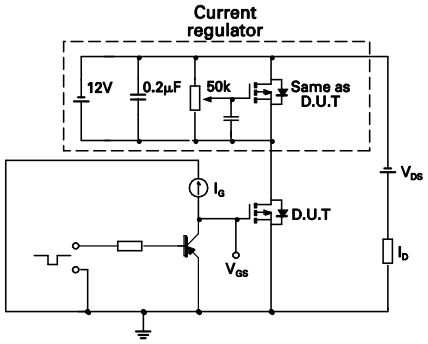


Gate-Source Voltage v Gate Charge

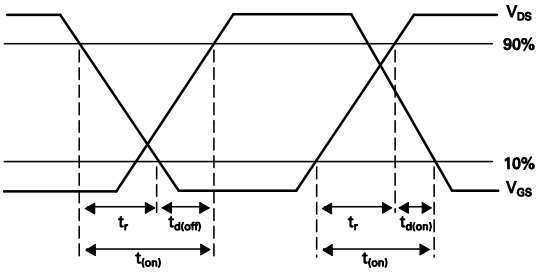
Test Circuits



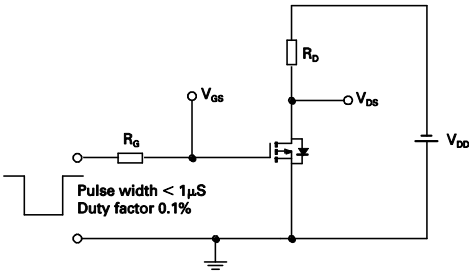
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms

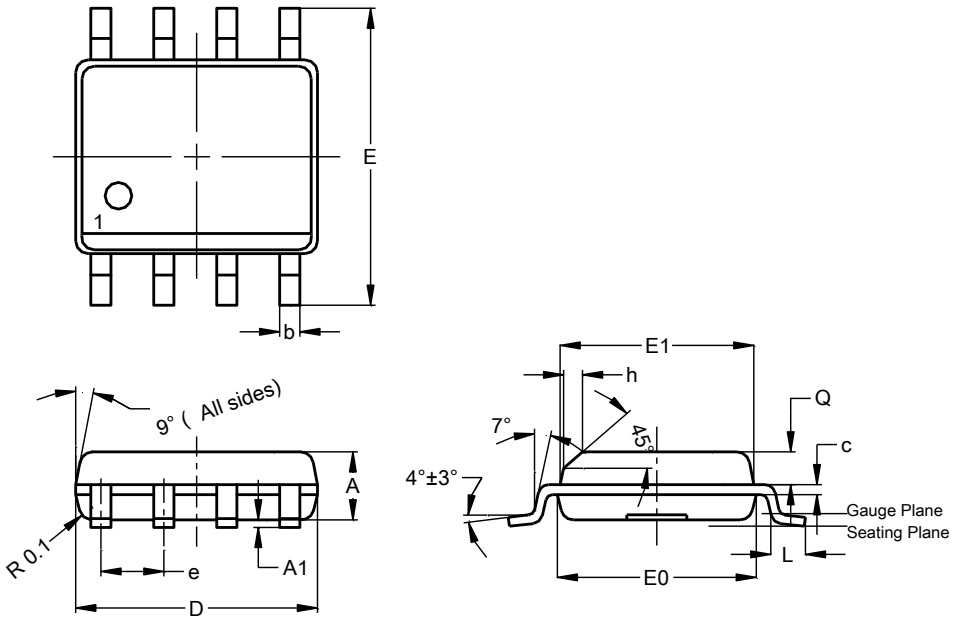


Switching time test circuit

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8

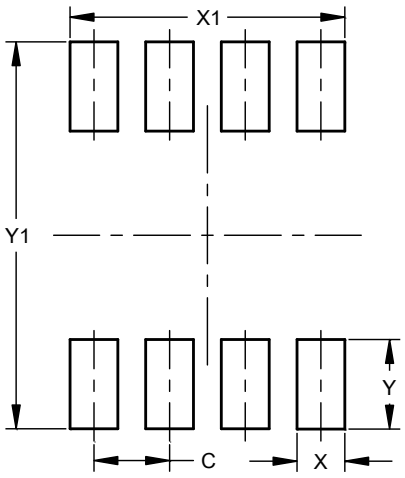


SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

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